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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	31775
Number of Logic Elements/Cells	406720
Total RAM Bits	29306880
Number of I/O	500
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	900-BBGA, FCBGA
Supplier Device Package	900-FCBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7k410t-2ffg900i

Table 3: DC Characteristics Over Recommended Operating Conditions (Cont'd)

Symbol	Description	Min	Typ ⁽¹⁾	Max	Units
$R_{IN_TERM}^{(4)}$	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_40) for commercial (C), industrial (I), and extended (E) temperature devices	28	40	55	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_50) for commercial (C), industrial (I), and extended (E) temperature devices	35	50	65	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_60) for commercial (C), industrial (I), and extended (E) temperature devices	44	60	83	Ω
n	Temperature diode ideality factor	—	1.010	—	—
r	Temperature diode series resistance	—	2	—	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a $V_{CCO}/2$ level.

Table 4: Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks⁽¹⁾

AC Voltage Overshoot	% of UI @–40°C to 100°C	AC Voltage Undershoot	% of UI @–40°C to 100°C
$V_{CCO} + 0.40$	100	–0.40	100
$V_{CCO} + 0.45$	100	–0.45	61.7
$V_{CCO} + 0.50$	100	–0.50	25.8
$V_{CCO} + 0.55$	100	–0.55	11.0
$V_{CCO} + 0.60$	46.6	–0.60	4.77
$V_{CCO} + 0.65$	21.2	–0.65	2.10
$V_{CCO} + 0.70$	9.75	–0.70	0.94
$V_{CCO} + 0.75$	4.55	–0.75	0.43
$V_{CCO} + 0.80$	2.15	–0.80	0.20
$V_{CCO} + 0.85$	1.02	–0.85	0.09
$V_{CCO} + 0.90$	0.49	–0.90	0.04
$V_{CCO} + 0.95$	0.24	–0.95	0.02

Notes:

1. A total of 200 mA per bank should not be exceeded.

Table 5: Maximum Allowed AC Voltage Overshoot and Undershoot for 1.8V HP I/O Banks⁽¹⁾⁽²⁾

AC Voltage Overshoot	% of UI @–40°C to 100°C	AC Voltage Undershoot	% of UI @–40°C to 100°C
$V_{CCO} + 0.40$	100	–0.40	100
$V_{CCO} + 0.45$	100	–0.45	100
$V_{CCO} + 0.50$	100	–0.50	100
$V_{CCO} + 0.55$	100	–0.55	100
$V_{CCO} + 0.60$	50.0	–0.60	50.0
$V_{CCO} + 0.65$	50.0	–0.65	50.0
$V_{CCO} + 0.70$	47.0	–0.70	50.0
$V_{CCO} + 0.75$	21.2	–0.75	50.0

Table 5: Maximum Allowed AC Voltage Overshoot and Undershoot for 1.8V HP I/O Banks⁽¹⁾⁽²⁾ (Cont'd)

AC Voltage Overshoot	% of UI @-40°C to 100°C	AC Voltage Undershoot	% of UI @-40°C to 100°C
$V_{CCO} + 0.80$	9.71	-0.80	50.0
$V_{CCO} + 0.85$	4.51	-0.85	28.4
$V_{CCO} + 0.90$	2.12	-0.90	12.7
$V_{CCO} + 0.95$	1.01	-0.95	5.79

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 μ s.

Table 6: Typical Quiescent Supply Current

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC7K70T	241	241	241	187	mA
		XC7K160T	474	474	474	368	mA
		XC7K325T	810	810	810	629	mA
		XC7K355T	993	993	993	771	mA
		XC7K410T	1080	1080	1080	838	mA
		XC7K420T	1313	1313	1313	1019	mA
		XC7K480T	1313	1313	1313	1019	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC7K70T	1	1	1	1	mA
		XC7K160T	1	1	1	1	mA
		XC7K325T	1	1	1	1	mA
		XC7K355T	1	1	1	1	mA
		XC7K410T	1	1	1	1	mA
		XC7K420T	1	1	1	1	mA
		XC7K480T	1	1	1	1	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC7K70T	21	21	21	21	mA
		XC7K160T	40	40	40	40	mA
		XC7K325T	68	68	68	68	mA
		XC7K355T	75	75	75	75	mA
		XC7K410T	85	85	85	85	mA
		XC7K420T	99	99	99	99	mA
		XC7K480T	99	99	99	99	mA
$I_{CCAUX_{IO}Q}$	Quiescent $V_{CCAUX_{IO}}$ supply current	XC7K70T	N/A	N/A	N/A	N/A	mA
		XC7K160T	2	2	2	2	mA
		XC7K325T	2	2	2	2	mA
		XC7K355T	N/A	N/A	N/A	N/A	mA
		XC7K410T	2	2	2	2	mA
		XC7K420T	N/A	N/A	N/A	N/A	mA
		XC7K480T	N/A	N/A	N/A	N/A	mA

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 9: SelectIO DC Input and Output Levels (1)(2)

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	8	-8
HSTL_I_12	-0.300	$V_{REF} - 0.080$	$V_{REF} + 0.080$	$V_{CCO} + 0.300$	25% V_{CCO}	75% V_{CCO}	6.3	-6.3
HSTL_I_18	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	8	-8
HSTL_II	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	16	-16
HSTL_II_18	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	16	-16
HSUL_12	-0.300	$V_{REF} - 0.130$	$V_{REF} + 0.130$	$V_{CCO} + 0.300$	20% V_{CCO}	80% V_{CCO}	0.1	-0.1
LVC MOS12	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 3	Note 3
LVC MOS15, LVDCI_15	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	25% V_{CCO}	75% V_{CCO}	Note 4	Note 4
LVC MOS18, LVDCI_18	-0.300	35% V_{CCO}	65% V_{CCO}	$V_{CCO} + 0.300$	0.450	$V_{CCO} - 0.450$	Note 5	Note 5
LVC MOS25	-0.300	0.700	1.700	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 6	Note 6
LVC MOS33	-0.300	0.800	2.000	3.450	0.400	$V_{CCO} - 0.400$	Note 6	Note 6
LV TTL	-0.300	0.800	2.000	3.450	0.400	2.400	Note 7	Note 7
MOBILE_DDR	-0.300	20% V_{CCO}	80% V_{CCO}	$V_{CCO} + 0.300$	10% V_{CCO}	90% V_{CCO}	0.1	-0.1
PCI33_3	-0.500	30% V_{CCO}	50% V_{CCO}	$V_{CCO} + 0.500$	10% V_{CCO}	90% V_{CCO}	1.5	-0.5
SSTL12	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	14.25	-14.25
SSTL135	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	13.0	-13.0
SSTL135_R	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	8.9	-8.9
SSTL15	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.175$	$V_{CCO}/2 + 0.175$	13.0	-13.0
SSTL15_R	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.175$	$V_{CCO}/2 + 0.175$	8.9	-8.9
SSTL18_I	-0.300	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.470$	$V_{CCO}/2 + 0.470$	8	-8
SSTL18_II	-0.300	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.600$	$V_{CCO}/2 + 0.600$	13.4	-13.4

Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in 3.3V I/O banks.
3. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks and 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. Supported drive strengths of 4, 8, 12, or 16 mA
7. Supported drive strengths of 4, 8, 12, 16, or 24 mA
8. For detailed interface specific DC voltage levels, see [UG471: 7 Series FPGAs SelectIO Resources User Guide](#).

Table 18: Maximum Physical Interface (PHY) Rate for Memory Interfaces (FBG Packages)⁽¹⁾⁽²⁾

Memory Standard	I/O Bank Type	V _{CCAUX_IO} ⁽³⁾	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
4:1 Memory Controllers							
DDR3	HP	N/A	1333	1066	800	800	Mb/s
	HR	N/A	1066	800	800	800	Mb/s
DDR3L	HP	N/A	1066	800	667	667	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	N/A	800	800	800	800	Mb/s
	HR	N/A	800	667	667	667	Mb/s
RLDRAM III ⁽⁴⁾	HP	N/A	550	500	450	450	MHz
	HR	N/A	N/A				
2:1 Memory Controllers							
DDR3	HP	N/A	1066	1066	800	800	Mb/s
	HR	N/A	1066	800	800	800	Mb/s
DDR3L	HP	N/A	1066	800	667	667	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	N/A	800	800	800	800	Mb/s
	HR	N/A	800	667	667	667	Mb/s
QDR II+ ⁽⁵⁾	HP	N/A	550	500	450	450	MHz
	HR	N/A	450	400	350	350	MHz
RLDRAM II	HP	N/A	533	500	450	450	MHz
	HR	N/A					
LPDDR2 ⁽⁴⁾	HP	N/A	667	667	667	667	Mb/s
	HR	N/A	667	667	533	533	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see [UG586](#), *7 Series FPGAs Memory Interface Solutions User Guide*.
2. When using the internal V_{REF} the maximum data rate is 800 Mb/s (400 MHz).
3. FBG packages do not have separate V_{CCAUX_IO} supply pins to adjust the pre-driver voltage of the HP I/O banks.
4. RLDRAM III (BL = 4, BL = 8) and LPDDR2 specifications have not been validated with memory IP.
5. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

Table 19: 3.3V IOB High Range (HR) Switching Characteristics (Cont'd)

I/O Standard	T _{IOP1}				T _{IOP0}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
HSTL_I_F	0.61	0.64	0.73	0.79	1.10	1.19	1.23	1.41	1.86	2.05	2.22	1.92	ns
HSTL_II_F	0.61	0.64	0.73	0.78	1.05	1.18	1.28	1.42	1.81	2.04	2.27	1.94	ns
HSTL_I_18_F	0.64	0.67	0.76	0.79	1.05	1.18	1.28	1.44	1.81	2.04	2.27	1.95	ns
HSTL_II_18_F	0.64	0.67	0.76	0.79	1.03	1.14	1.23	1.42	1.79	2.00	2.22	1.94	ns
DIFF_HSTL_I_F	0.63	0.67	0.77	0.78	1.09	1.18	1.22	1.48	1.85	2.04	2.21	2.00	ns
DIFF_HSTL_II_F	0.63	0.67	0.77	0.79	1.02	1.11	1.14	1.48	1.78	1.97	2.13	2.00	ns
DIFF_HSTL_I_18_F	0.65	0.69	0.78	0.79	1.08	1.17	1.21	1.48	1.84	2.03	2.20	2.00	ns
DIFF_HSTL_II_18_F	0.65	0.69	0.78	0.81	1.01	1.10	1.13	1.48	1.77	1.96	2.12	2.00	ns
LVC MOS33_S4	1.31	1.40	1.60	1.54	5.23	5.61	6.09	4.13	5.99	6.47	7.08	4.64	ns
LVC MOS33_S8	1.31	1.40	1.60	1.54	4.46	4.85	5.33	3.84	5.22	5.71	6.32	4.36	ns
LVC MOS33_S12	1.31	1.40	1.60	1.54	3.46	3.89	4.42	3.41	4.22	4.75	5.41	3.92	ns
LVC MOS33_S16	1.31	1.40	1.60	1.54	3.06	3.43	3.88	3.72	3.82	4.29	4.87	4.23	ns
LVC MOS33_F4	1.31	1.40	1.60	1.54	4.70	5.01	5.36	3.58	5.46	5.87	6.35	4.09	ns
LVC MOS33_F8	1.31	1.40	1.60	1.54	3.62	4.04	4.56	3.06	4.38	4.90	5.55	3.58	ns
LVC MOS33_F12	1.31	1.40	1.60	1.54	2.57	2.85	3.15	2.88	3.33	3.71	4.14	3.39	ns
LVC MOS33_F16	1.31	1.40	1.60	1.54	2.44	2.69	2.96	2.88	3.20	3.55	3.95	3.39	ns
LVC MOS25_S4	1.08	1.16	1.32	1.36	4.49	4.80	5.16	3.44	5.25	5.66	6.15	3.95	ns
LVC MOS25_S8	1.08	1.16	1.32	1.36	3.66	4.04	4.49	3.20	4.42	4.90	5.48	3.72	ns
LVC MOS25_S12	1.08	1.16	1.32	1.36	2.77	3.10	3.49	2.80	3.53	3.96	4.48	3.31	ns
LVC MOS25_S16	1.08	1.16	1.32	1.36	3.24	3.62	4.09	3.14	4.00	4.48	5.08	3.66	ns
LVC MOS25_F4	1.08	1.16	1.32	1.36	3.96	4.31	4.72	3.06	4.72	5.17	5.71	3.58	ns
LVC MOS25_F8	1.08	1.16	1.32	1.36	2.43	2.87	3.42	2.50	3.19	3.73	4.41	3.02	ns
LVC MOS25_F12	1.08	1.16	1.32	1.36	2.23	2.63	3.13	2.48	2.99	3.49	4.12	3.00	ns
LVC MOS25_F16	1.08	1.16	1.32	1.36	1.92	2.17	2.45	2.33	2.68	3.03	3.44	2.84	ns
LVC MOS18_S4	0.64	0.66	0.74	0.87	3.24	3.45	3.66	1.91	4.00	4.31	4.65	2.42	ns
LVC MOS18_S8	0.64	0.66	0.74	0.87	2.58	2.91	3.31	2.50	3.34	3.77	4.30	3.02	ns
LVC MOS18_S12	0.64	0.66	0.74	0.87	2.58	2.91	3.31	2.50	3.34	3.77	4.30	3.02	ns
LVC MOS18_S16	0.64	0.66	0.74	0.87	1.82	2.03	2.24	1.84	2.58	2.89	3.23	2.36	ns
LVC MOS18_S24 ⁽¹⁾	0.64	0.66	0.74	0.87	1.74	1.92	2.08	1.92	2.50	2.78	3.07	2.44	ns
LVC MOS18_F4	0.64	0.66	0.74	0.87	3.12	3.31	3.49	1.77	3.88	4.17	4.48	2.28	ns
LVC MOS18_F8	0.64	0.66	0.74	0.87	1.91	2.13	2.36	2.00	2.67	2.99	3.35	2.52	ns
LVC MOS18_F12	0.64	0.66	0.74	0.87	1.91	2.13	2.36	2.00	2.67	2.99	3.35	2.52	ns
LVC MOS18_F16	0.64	0.66	0.74	0.87	1.52	1.68	1.81	1.72	2.28	2.54	2.80	2.23	ns
LVC MOS18_F24 ⁽¹⁾	0.64	0.66	0.74	0.87	1.34	1.46	1.55	1.66	2.10	2.32	2.54	2.17	ns
LVC MOS15_S4	0.66	0.69	0.81	0.90	3.48	3.74	4.03	2.22	4.24	4.60	5.02	2.73	ns
LVC MOS15_S8	0.66	0.69	0.81	0.90	2.37	2.67	3.01	2.41	3.13	3.53	4.00	2.92	ns
LVC MOS15_S12	0.66	0.69	0.81	0.90	1.83	2.03	2.23	1.91	2.59	2.89	3.22	2.42	ns

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
SSTL18_I_F	0.68	0.72	0.82	0.86	0.94	1.06	1.15	1.32	1.58	1.82	1.97	1.93	ns
SSTL18_II_F	0.68	0.72	0.82	0.87	0.97	1.09	1.16	1.36	1.61	1.84	1.99	1.98	ns
SSTL18_I_DCI_F	0.68	0.72	0.82	0.76	0.89	1.02	1.10	1.30	1.53	1.77	1.92	1.91	ns
SSTL18_II_DCI_F	0.68	0.72	0.82	0.78	0.89	1.02	1.10	1.24	1.53	1.77	1.92	1.85	ns
SSTL18_II_T_DCI_F	0.68	0.72	0.82	0.78	0.89	1.02	1.10	1.27	1.53	1.77	1.92	1.88	ns
SSTL15_F	0.68	0.72	0.82	0.81	0.89	1.01	1.09	1.24	1.53	1.77	1.91	1.85	ns
SSTL15_DCI_F	0.68	0.72	0.82	0.78	0.89	1.01	1.09	1.27	1.53	1.77	1.91	1.88	ns
SSTL15_T_DCI_F	0.68	0.72	0.82	0.80	0.89	1.01	1.09	1.27	1.53	1.77	1.91	1.88	ns
SSTL135_F	0.69	0.72	0.82	0.89	0.88	1.00	1.08	1.27	1.52	1.76	1.90	1.88	ns
SSTL135_DCI_F	0.69	0.72	0.82	0.84	0.89	1.00	1.08	1.27	1.52	1.76	1.90	1.88	ns
SSTL135_T_DCI_F	0.69	0.72	0.82	0.84	0.89	1.00	1.08	1.27	1.52	1.76	1.90	1.88	ns
SSTL12_F	0.69	0.72	0.82	0.95	0.88	1.00	1.08	1.26	1.52	1.76	1.90	1.87	ns
SSTL12_DCI_F	0.69	0.72	0.82	0.91	0.91	1.03	1.11	1.24	1.54	1.79	1.93	1.85	ns
SSTL12_T_DCI_F	0.69	0.72	0.82	0.91	0.91	1.03	1.11	1.26	1.54	1.79	1.93	1.87	ns
DIFF_SSTL18_I_F	0.75	0.79	0.92	0.89	0.94	1.06	1.15	1.38	1.58	1.82	1.97	1.99	ns
DIFF_SSTL18_II_F	0.75	0.79	0.92	0.89	0.97	1.09	1.16	1.40	1.61	1.84	1.99	2.01	ns
DIFF_SSTL18_I_DCI_F	0.75	0.79	0.92	0.76	0.89	1.02	1.10	1.36	1.53	1.77	1.92	1.98	ns
DIFF_SSTL18_II_DCI_F	0.75	0.79	0.92	0.75	0.89	1.02	1.10	1.32	1.53	1.77	1.92	1.93	ns
DIFF_SSTL18_II_T_DCI_F	0.75	0.79	0.92	0.76	0.89	1.02	1.10	1.38	1.53	1.77	1.92	1.99	ns
DIFF_SSTL15_F	0.68	0.72	0.82	0.89	0.89	1.01	1.09	1.24	1.53	1.77	1.91	1.85	ns
DIFF_SSTL15_DCI_F	0.68	0.72	0.82	0.75	0.89	1.01	1.09	1.27	1.53	1.77	1.91	1.88	ns
DIFF_SSTL15_T_DCI_F	0.68	0.72	0.82	0.76	0.89	1.01	1.09	1.35	1.53	1.77	1.91	1.96	ns
DIFF_SSTL135_F	0.69	0.72	0.82	0.91	0.88	1.00	1.08	1.27	1.52	1.76	1.90	1.88	ns
DIFF_SSTL135_DCI_F	0.69	0.72	0.82	0.76	0.89	1.00	1.08	1.27	1.52	1.76	1.90	1.88	ns
DIFF_SSTL135_T_DCI_F	0.69	0.72	0.82	0.76	0.89	1.00	1.08	1.35	1.52	1.76	1.90	1.96	ns
DIFF_SSTL12_F	0.69	0.72	0.82	0.91	0.88	1.00	1.08	1.26	1.52	1.76	1.90	1.87	ns
DIFF_SSTL12_DCI_F	0.69	0.72	0.82	0.78	0.91	1.03	1.11	1.24	1.54	1.79	1.93	1.85	ns
DIFF_SSTL12_T_DCI_F	0.69	0.72	0.82	0.80	0.91	1.03	1.11	1.33	1.54	1.79	1.93	1.94	ns

Notes:

1. This I/O standard is only available in the 1.8V high-performance (HP) banks.

Table 21 specifies the values of T_{IOTPHZ} and $T_{IOIBUFDISABLE}$. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than T_{IOTPHZ} when the DCITERMDISABLE pin is used. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than T_{IOTPHZ} when the INTERMDISABLE pin is used.

Table 21: IOB 3-state Output Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{IOTPHZ}	T input to pad high-impedance	0.76	0.86	0.99	0.62	ns
$T_{IOIBUFDISABLE_HR}$	IBUF turn-on time from IBUFDISABLE to O output for HR I/O banks	1.72	1.89	2.14	2.17	ns
$T_{IOIBUFDISABLE_HP}$	IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks	1.31	1.46	1.76	1.86	ns

Table 23: OLOGIC Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T _{ODCK} /T _{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.45/−0.13	0.50/−0.13	0.58/−0.13	0.79/−0.18	ns
T _{OOCECK} /T _{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	0.35/−0.10	ns
T _{OSRCK} /T _{OCKSR}	SR pin Setup/Hold with respect to CLK	0.32/0.18	0.38/0.18	0.70/0.18	0.62/−0.04	ns
T _{OTCK} /T _{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.49/−0.16	0.56/−0.16	0.68/−0.16	0.67/−0.18	ns
T _{OTCECK} /T _{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	0.31/−0.10	ns
Combinatorial						
T _{ODQ}	D1 to OQ out or T1 to TQ out	0.73	0.81	0.97	1.18	ns
Sequential Delays						
T _{OCKQ}	CLK to OQ/TQ out	0.41	0.43	0.49	0.63	ns
T _{RQ_OLOGICE2}	SR pin to OQ/TQ out (HP I/O banks only)	0.63	0.70	0.83	1.12	ns
T _{GSRQ_OLOGICE2}	Global Set/Reset to Q outputs (HP I/O banks only)	7.60	7.60	10.51	11.39	ns
T _{RQ_OLOGICE3}	SR pin to OQ/TQ out (HR I/O banks only)	0.63	0.70	0.83	1.12	ns
T _{GSRQ_OLOGICE3}	Global Set/Reset to Q outputs (HR I/O banks only)	7.60	7.60	10.51	11.39	ns
Set/Reset						
T _{RPW_OLOGICE2}	Minimum Pulse Width, SR inputs (HP I/O banks only)	0.54	0.54	0.63	0.68	ns, Min
T _{RPW_OLOGICE3}	Minimum Pulse Width, SR inputs (HR I/O banks only)	0.54	0.54	0.63	0.68	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 24: ISERDES Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold for Control Lines						
T _{ISCK_BITSLIP} / T _{ISCKC_BITSLIP}	BITSLIP pin Setup/Hold with respect to CLKDIV	0.01/0.12	0.02/0.13	0.02/0.15	0.02/0.21	ns
T _{ISCK_CE} / T _{ISCKC_CE} ⁽²⁾	CE pin Setup/Hold with respect to CLK (for CE1)	0.39/−0.02	0.44/−0.02	0.63/−0.02	0.51/−0.22	ns
T _{ISCK_CE2} / T _{ISCKC_CE2} ⁽²⁾	CE pin Setup/Hold with respect to CLKDIV (for CE2)	−0.12/0.29	−0.12/0.31	−0.12/0.35	−0.17/0.40	ns
Setup/Hold for Data Lines						
T _{ISDCK_D} /T _{ISCKD_D}	D pin Setup/Hold with respect to CLK	−0.02/0.11	−0.02/0.12	−0.02/0.15	−0.04/0.19	ns
T _{ISDCK_DDLY} / T _{ISCKD_DDLY}	DDLY pin Setup/Hold with respect to CLK (using IDELAY) ⁽¹⁾	−0.02/0.11	−0.02/0.12	−0.02/0.15	−0.03/0.19	ns
T _{ISDCK_D_DDR} / T _{ISCKD_D_DDR}	D pin Setup/Hold with respect to CLK at DDR mode	−0.02/0.11	−0.02/0.12	−0.02/0.15	−0.04/0.19	ns
T _{ISDCK_DDLY_DDR} / T _{ISCKD_DDLY_DDR}	D pin Setup/Hold with respect to CLK at DDR mode (using IDELAY) ⁽¹⁾	0.11/0.11	0.12/0.12	0.15/0.15	0.19/0.19	ns
Sequential Delays						
T _{ISCKO_Q}	CLKDIV to out at Q pin	0.46	0.47	0.58	0.67	ns
Propagation Delays						
T _{ISDO_DO}	D input to DO output pin	0.09	0.10	0.12	0.14	ns

Notes:

1. Recorded at 0 tap value.
2. T_{ISCK_CE2} and T_{ISCK_CE2} are reported as T_{ISCK_CE}/T_{ISCK_CE} in TRACE report.

Table 27: IO_FIFO Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
IO_FIFO Clock to Out Delays						
T _{OFFCKO_DO}	RDCLK to Q outputs	0.51	0.56	0.63	0.81	ns
T _{CKO_FLAGS}	Clock to IO_FIFO Flags	0.59	0.62	0.81	0.77	ns
Setup/Hold						
T _{CCK_D} /T _{CKC_D}	D inputs to WRCLK	0.43/−0.01	0.47/−0.01	0.53/−0.01	0.76/−0.05	ns
T _{IFFCKC_WREN} /T _{IFFCKC_WREN}	WREN to WRCLK	0.39/−0.01	0.43/−0.01	0.50/−0.01	0.70/−0.05	ns
T _{OFFCKC_RDEN} /T _{OFFCKC_RDEN}	RDEN to RDCLK	0.49/0.01	0.53/0.02	0.61/0.02	0.79/−0.02	ns
Minimum Pulse Width						
T _{PWH_IO_FIFO}	RESET, RDCLK, WRCLK	0.81	0.92	1.08	1.29	ns
T _{PWL_IO_FIFO}	RESET, RDCLK, WRCLK	0.81	0.92	1.08	1.29	ns
Maximum Frequency						
F _{MAX}	RDCLK and WRCLK	533.05	470.37	400.00	333.33	MHz

Table 32: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup and Hold Times of the RST Pins						
$T_{\text{DSPDCK}_{\{\text{RSTA}; \text{RSTB}\}}_{\{\text{AREG}; \text{BREG}\}}/T_{\text{DSPCKD}_{\{\text{RSTA}; \text{RSTB}\}}_{\{\text{AREG}; \text{BREG}\}}}$	{RSTA, RSTB} input to {A, B} register CLK	0.34/ 0.10	0.39/ 0.11	0.47/ 0.13	0.53/ 0.34	ns
$T_{\text{DSPDCK_RSTC_CREG}}/T_{\text{DSPCKD_RSTC_CREG}}$	RSTC input to C register CLK	0.06/ 0.22	0.07/ 0.24	0.08/ 0.26	0.08/ 0.31	ns
$T_{\text{DSPDCK_RSTD_DREG}}/T_{\text{DSPCKD_RSTD_DREG}}$	RSTD input to D register CLK	0.37/ 0.06	0.42/ 0.06	0.50/ 0.07	0.57/ 0.07	ns
$T_{\text{DSPDCK_RSTM_MREG}}/T_{\text{DSPCKD_RSTM_MREG}}$	RSTM input to M register CLK	0.18/ 0.18	0.20/ 0.21	0.23/ 0.24	0.24/ 0.29	ns
$T_{\text{DSPDCK_RSTP_PREG}}/T_{\text{DSPCKD_RSTP_PREG}}$	RSTP input to P register CLK	0.24/ 0.01	0.26/ 0.01	0.30/ 0.01	0.37/ 0.00	ns
Combinatorial Delays from Input Pins to Output Pins						
$T_{\text{DSPDO_A_CARRYOUT_MULT}}$	A input to CARRYOUT output using multiplier	3.21	3.69	4.39	5.60	ns
$T_{\text{DSPDO_D_P_MULT}}$	D input to P output using multiplier	3.15	3.61	4.30	5.44	ns
$T_{\text{DSPDO_A_P}}$	A input to P output not using multiplier	1.30	1.48	1.76	2.10	ns
$T_{\text{DSPDO_C_P}}$	C input to P output	1.13	1.30	1.55	1.84	ns
Combinatorial Delays from Input Pins to Cascading Output Pins						
$T_{\text{DSPDO}_{\{\text{A}; \text{B}\}}_{\{\text{ACOUT}; \text{BCOUT}\}}}$	{A, B} input to {ACOUT, BCOUT} output	0.47	0.53	0.63	0.75	ns
$T_{\text{DSPDO}_{\{\text{A}; \text{B}\}}_{\text{CARRYCASCOUT_MULT}}}$	{A, B} input to CARRYCASCOUT output using multiplier	3.44	3.94	4.69	5.96	ns
$T_{\text{DSPDO_D_CARRYCASCOUT_MULT}}$	D input to CARRYCASCOUT output using multiplier	3.36	3.85	4.58	5.77	ns
$T_{\text{DSPDO}_{\{\text{A}; \text{B}\}}_{\text{CARRYCASCOUT}}}$	{A, B} input to CARRYCASCOUT output not using multiplier	1.50	1.72	2.04	2.44	ns
$T_{\text{DSPDO_C_CARRYCASCOUT}}$	C input to CARRYCASCOUT output	1.34	1.53	1.83	2.18	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins						
$T_{\text{DSPDO_ACIN_P_MULT}}$	ACIN input to P output using multiplier	3.09	3.55	4.24	5.42	ns
$T_{\text{DSPDO_ACIN_P}}$	ACIN input to P output not using multiplier	1.16	1.33	1.59	2.07	ns
$T_{\text{DSPDO_ACIN_ACOUT}}$	ACIN input to ACOUT output	0.32	0.37	0.45	0.53	ns
$T_{\text{DSPDO_ACIN_CARRYCASCOUT_MULT}}$	ACIN input to CARRYCASCOUT output using multiplier	3.30	3.79	4.52	5.76	ns
$T_{\text{DSPDO_ACIN_CARRYCASCOUT}}$	ACIN input to CARRYCASCOUT output not using multiplier	1.37	1.57	1.87	2.40	ns
$T_{\text{DSPDO_PCIN_P}}$	PCIN input to P output	0.94	1.08	1.29	1.54	ns
$T_{\text{DSPDO_PCIN_CARRYCASCOUT}}$	PCIN input to CARRYCASCOUT output	1.15	1.32	1.57	1.88	ns
Clock to Outs from Output Register Clock to Output Pins						
$T_{\text{DSPCKO_P_PREG}}$	CLK PREG to P output	0.33	0.35	0.39	0.45	ns
$T_{\text{DSPCKO_CARRYCASCOUT_PREG}}$	CLK PREG to CARRYCASCOUT output	0.44	0.50	0.59	0.71	ns

Table 32: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Clock to Outs from Pipeline Register Clock to Output Pins						
T _{DSPCKO_P_MREG}	CLK MREG to P output	1.42	1.64	1.96	2.31	ns
T _{DSPCKO_CARRYCASCOUT_MREG}	CLK MREG to CARRYCASCOUT output	1.63	1.87	2.24	2.65	ns
T _{DSPCKO_P_ADREG_MULT}	CLK ADREG to P output using multiplier	2.30	2.63	3.13	3.90	ns
T _{DSPCKO_CARRYCASCOUT_ADREG_MULT}	CLK ADREG to CARRYCASCOUT output using multiplier	2.51	2.87	3.41	4.23	ns
Clock to Outs from Input Register Clock to Output Pins						
T _{DSPCKO_P_AREG_MULT}	CLK AREG to P output using multiplier	3.34	3.83	4.55	5.80	ns
T _{DSPCKO_P_BREG}	CLK BREG to P output not using multiplier	1.39	1.59	1.88	2.24	ns
T _{DSPCKO_P_CREG}	CLK CREG to P output not using multiplier	1.43	1.64	1.95	2.32	ns
T _{DSPCKO_P_DREG_MULT}	CLK DREG to P output using multiplier	3.32	3.80	4.51	5.74	ns
Clock to Outs from Input Register Clock to Cascading Output Pins						
T _{DSPCKO_{ACOUT; BCOUT}_{AREG; BREG}}	CLK (ACOUT, BCOUT) to {A,B} register output	0.55	0.62	0.74	0.87	ns
T _{DSPCKO_CARRYCASCOUT_{AREG, BREG}_MULT}	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier	3.55	4.06	4.84	6.13	ns
T _{DSPCKO_CARRYCASCOUT_BREG}	CLK BREG to CARRYCASCOUT output not using multiplier	1.60	1.82	2.16	2.58	ns
T _{DSPCKO_CARRYCASCOUT_DREG_MULT}	CLK DREG to CARRYCASCOUT output using multiplier	3.52	4.03	4.79	6.07	ns
T _{DSPCKO_CARRYCASCOUT_CREG}	CLK CREG to CARRYCASCOUT output	1.64	1.88	2.23	2.65	ns
Maximum Frequency						
F _{MAX}	With all registers used	741.84	650.20	547.95	429.37	MHz
F _{MAX_PATDET}	With pattern detector	627.35	549.75	463.61	365.90	MHz
F _{MAX_MULT_NOMREG}	Two register multiply without MREG	412.20	360.75	303.77	248.32	MHz
F _{MAX_MULT_NOMREG_PATDET}	Two register multiply without MREG with pattern detect	374.25	327.65	276.01	225.73	MHz
F _{MAX_PREADD_MULT_NOADREG}	Without ADREG	468.82	408.66	342.70	263.44	MHz
F _{MAX_PREADD_MULT_NOADREG_PATDET}	Without ADREG with pattern detect	468.82	408.66	342.70	263.44	MHz
F _{MAX_NOPIPELINEREG}	Without pipeline registers (MREG, ADREG)	306.84	267.81	225.02	177.15	MHz
F _{MAX_NOPIPELINEREG_PATDET}	Without pipeline registers (MREG, ADREG) with pattern detect	285.23	249.13	209.38	165.32	MHz

Clock Buffers and Networks

Table 33: Global Clock Switching Characteristics (Including BUFGCTRL)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
$T_{BCCCK_CE}/T_{BCKKC_CE}^{(1)}$	CE pins Setup/Hold	0.12/0.30	0.14/0.38	0.26/0.38	0.23/0.40	ns
$T_{BCCCK_S}/T_{BCKKC_S}^{(1)}$	S pins Setup/Hold	0.12/0.30	0.14/0.38	0.26/0.38	0.23/0.40	ns
$T_{BCKKO_O}^{(2)}$	BUFGCTRL delay from I0/I1 to O	0.08	0.10	0.12	0.10	ns
Maximum Frequency						
F_{MAX_BUFG}	Global clock tree (BUFG)	741.00	710.00	625.00	560.00	MHz

Notes:

- T_{BCCCK_CE} and T_{BCKKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
- T_{BCKKO_O} (BUFG delay from I0 to O) values are the same as T_{BCKKO_O} values.

Table 34: Input/Output Clock Switching Characteristics (BUFIO)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BIOCKO_O}	Clock to out delay from I to O	1.04	1.14	1.32	1.48	ns
Maximum Frequency						
F_{MAX_BUFIO}	I/O clock tree (BUFIO)	800.00	800.00	710.00	710.00	MHz

Table 35: Regional Clock Buffer Switching Characteristics (BUFR)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BRCKO_O}	Clock to out delay from I to O	0.60	0.65	0.77	1.06	ns
$T_{BRCKO_O_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.30	0.32	0.38	0.57	ns
T_{BRDO_O}	Propagation delay from CLR to O	0.71	0.75	0.96	0.93	ns
Maximum Frequency						
$F_{MAX_BUFR}^{(1)}$	Regional clock tree (BUFR)	600.00	540.00	450.00	450.00	MHz

Notes:

- The maximum input frequency to the BUFR is the BUFIO F_{MAX} frequency.

Table 36: Horizontal Clock Buffer Switching Characteristics (BUFH)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BHCKO_O}	BUFH delay from I to O	0.10	0.11	0.13	0.12	ns
T_{BHCK_CE}/T_{BHCK_CE}	CE pin Setup and Hold	0.20/0.16	0.23/0.20	0.38/0.21	0.28/0.09	ns
Maximum Frequency						
F_{MAX_BUFH}	Horizontal clock buffer (BUFH)	741.00	710.00	625.00	560.00	MHz

Table 37: Duty Cycle Distortion and Clock-Tree Skew

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion ⁽¹⁾	All	0.20	0.20	0.20	0.25	ns
T_{CKSKEW}	Global Clock Tree Skew ⁽²⁾	XC7K70T	0.29	0.40	0.40	0.47	ns
		XC7K160T	0.42	0.53	0.57	0.59	ns
		XC7K325T	0.59	0.74	0.79	0.91	ns
		XC7K355T	0.45	0.57	0.59	0.69	ns
		XC7K410T	0.60	0.74	0.79	0.91	ns
		XC7K420T	0.60	0.74	0.79	0.91	ns
		XC7K480T	0.60	0.74	0.79	0.91	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.12	0.12	0.12	0.12	ns
T_{BUFIO_SKEW}	I/O clock tree skew across one clock region	All	0.02	0.02	0.02	0.03	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	0.15	0.15	ns

Notes:

- These parameters represent the worst-case duty cycle distortion observable at the I/O flip flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
- The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx Timing Analyzer tools to evaluate clock skew specific to your application.

Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 40: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL.							
T _{ICKOF}	Clock-capable clock input and OUTFF <i>without</i> MMCM/PLL (near clock region)	XC7K70T	4.98	5.49	6.17	7.04	ns
		XC7K160T	5.23	5.77	6.48	7.38	ns
		XC7K325T	5.72	6.31	7.09	8.07	ns
		XC7K355T	5.34	5.87	6.57	7.51	ns
		XC7K410T	5.84	6.44	7.22	8.21	ns
		XC7K420T	5.50	6.04	6.77	7.73	ns
		XC7K480T	5.50	6.04	6.77	7.73	ns

Notes:

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 41: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL.							
T _{ICKOFFAR}	Clock-capable clock input and OUTFF <i>without</i> MMCM/PLL (far clock region)	XC7K70T	5.29	5.83	6.55	7.47	ns
		XC7K160T	5.84	6.45	7.24	8.24	ns
		XC7K325T	6.33	6.99	7.84	8.92	ns
		XC7K355T	5.95	6.55	7.32	8.36	ns
		XC7K410T	6.45	7.12	7.97	9.07	ns
		XC7K420T	6.41	7.06	7.90	9.01	ns
		XC7K480T	6.41	7.06	7.90	9.01	ns

Notes:

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 53: GTX Transceiver Performance (Cont'd)

Symbol	Description	Output Divider	Speed Grade								Units
			1.0V						0.9V		
			-3		-2/-2L		-1 ⁽¹⁾		-2L ⁽²⁾		
			Package Type								
			FF	FB	FF	FB	FF	FB	FF	FB	
F _{GQPLL} RANGE2	GTX transceiver QPLL frequency range 2		9.8–12.5		9.8–10.3125		N/A		N/A		GHz

Notes:

1. The -1 speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s.
2. The -2L (0.9V) speed grade requires a 4-byte internal data width for operation above 3.8 Gb/s.
3. Data rates between 8.0 Gb/s and 9.8 Gb/s are not available.
4. For QPLL line rate range 2, the maximum line rate with the divider N set to 66 is 10.3125Gb/s.

Table 54: GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
F _{GTXDRPCLK}	GTXDRPCLK maximum frequency	175.01	175.01	156.25	125.00	MHz

Table 55: GTX Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F _{GCLK}	Reference clock frequency range	-3 speed grade	60	–	700	MHz
		All other speed grades	60	–	670	MHz
T _{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T _{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T _{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

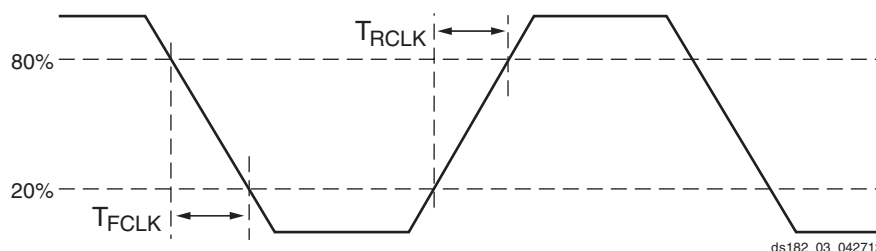


Figure 3: Reference Clock Timing Parameters

Table 56: GTX Transceiver PLL /Lock Time Adaptation

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T _{LOCK}	Initial PLL lock		–	–	1	ms
T _{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37 x10 ⁶	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3 x10 ⁶	UI

Table 57: GTX Transceiver User Clock Switching Characteristics⁽¹⁾⁽²⁾

Symbol	Description	Conditions	Speed Grade				Units
			1.0V			0.9V	
			-3 ⁽³⁾	-2/-2L ⁽³⁾	-1 ⁽⁴⁾	-2L ⁽⁵⁾	
F _{TXOUT}	TXOUTCLK maximum frequency		412.54	412.54	312.50	237.53	MHz
F _{RXOUT}	RXOUTCLK maximum frequency		412.54	412.54	312.50	237.53	MHz
F _{TXIN}	TXUSRCLK maximum frequency	16-bit data path	412.54	412.54	312.50	237.53	MHz
		32-bit data path	391.08	322.37	250.00	206.27	MHz
F _{RXIN}	RXUSRCLK maximum frequency	16-bit data path	412.54	412.54	312.50	237.53	MHz
		32-bit data path	391.08	322.37	250.00	206.27	MHz
F _{TXIN2}	TXUSRCLK2 maximum frequency	16-bit data path	412.54	412.54	312.50	237.53	MHz
		32-bit data path	391.08	322.37	250.00	206.27	MHz
		64-bit data path	195.54	161.19	125.00	103.14	MHz
F _{RXIN2}	RXUSRCLK2 maximum frequency	16-bit data path	412.54	412.54	312.50	237.53	MHz
		32-bit data path	391.08	322.37	250.00	206.27	MHz
		64-bit data path	195.54	161.19	125.00	103.14	MHz

Notes:

1. Clocking must be implemented as described in [UG476: 7 Series FPGAs GTX/GTH Transceiver User Guide](#).
2. These frequencies are not supported for all possible transceiver configurations.
3. For speed grades -3, -2, -2L (1.0V), a 16-bit data path can only be used for speeds less than 6.6 Gb/s.
4. For speed grade -1, a 16-bit data path can only be used for speeds less than 5.0 Gb/s.
5. For speed grade -2L (0.9V), a 16-bit data path can only be used for speeds less than 3.8 Gb/s.

Table 58: GTX Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTXTX}	Serial data rate range		0.500	–	F _{GTXMAX}	Gb/s
T _{RTX}	TX Rise time	20%–80%	–	40	–	ps
T _{FTX}	TX Fall time	80%–20%	–	40	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	500	ps
V _{TXOOBVDPP}	Electrical idle amplitude		–	–	15	mV
T _{TXOOBTRANSITION}	Electrical idle transition time		–	–	140	ns
TJ _{12.5}	Total Jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	–	–	0.28	UI
DJ _{12.5}	Deterministic Jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{11.18}	Total Jitter ⁽²⁾⁽⁴⁾	11.18 Gb/s	–	–	0.28	UI
DJ _{11.18}	Deterministic Jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI

GTX Transceiver Protocol Jitter Characteristics

For Table 60 through Table 65, the [UG476: 7 Series FPGAs GTX/GTH Transceiver User Guide](#) contains recommended settings for optimal usage of protocol specific characteristics.

Table 60: Gigabit Ethernet Protocol Characteristics

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 61: XAUI Protocol Characteristics

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 62: PCI Express Protocol Characteristics⁽¹⁾

Standard	Description		Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation						
PCI Express Gen 1	Total transmitter jitter		2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter		5000	–	0.25	UI
PCI Express Gen 3 ⁽²⁾	Total transmitter jitter uncorrelated		8000	–	31.25	ps
	Deterministic transmitter jitter uncorrelated			–	12	ps
PCI Express Receiver High Frequency Jitter Tolerance						
PCI Express Gen 1	Total receiver jitter tolerance		2500	0.65	–	UI
PCI Express Gen 2 ⁽³⁾	Receiver inherent timing error		5000	0.40	–	UI
	Receiver inherent deterministic timing error			0.30	–	UI
PCI Express Gen 3 ⁽²⁾	Receiver sinusoidal jitter tolerance	0.03 MHz–1.0 MHz	8000	1.00	–	UI
		1.0 MHz–10 MHz		Note 4	–	UI
		10 MHz–100 MHz		0.10	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. PCI-SIG 3.0 certification and compliance test boards are currently not available.
3. Using common REFCLK.
4. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20dB/decade.

Table 67: XADC Specifications (Cont'd)

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
XADC Reference⁽⁵⁾						
External Reference	V _{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-Chip Reference		Ground V _{REFP} pin to AGND, T _j = -40°C to 100°C	1.2375	1.25	1.2625	V

Notes:

- Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
- Only specified for new BitGen option XADCEnhancedLinearity = ON.
- See the ADC chapter in [UG480: 7 Series FPGAs XADC User Guide](#) for a detailed description.
- See the Timing chapter in [UG480: 7 Series FPGAs XADC User Guide](#) for a detailed description.
- Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted. On-chip reference variation is ±1%.

Configuration Switching Characteristics

Table 68: Configuration Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Power-up Timing Characteristics						
T _{PL} ⁽¹⁾	Program latency	5	5	5	5	ms, Max
T _{POR} ⁽¹⁾	Power-on reset (50 ms ramp rate time)	10/50	10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1 ms ramp rate time)	10/35	10/35	10/35	10/35	ms, Min/Max
T _{PROGRAM}	Program pulse width	250	250	250	250	ns, Min
CCLK Output (Master Mode)						
T _{ICCK}	Master CCLK output delay	150	150	150	150	ns, Min
T _{MCCKL}	Master CCLK clock Low time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max
T _{MCCKH}	Master CCLK clock High time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max
F _{MCCK}	Master CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max
	Master CCLK frequency for AES encrypted x16	50.00	50.00	50.00	35.00	MHz, Max
F _{MCCK_START}	Master CCLK frequency at start of configuration	3.00	3.00	3.00	3.00	MHz, Typ
F _{MCCKTOL}	Frequency tolerance, master mode with respect to nominal CCLK	±50	±50	±50	±50	%, Max
CCLK Input (Slave Modes)						
T _{SCCKL}	Slave CCLK clock minimum Low time	2.50	2.50	2.50	2.50	ns, Min
T _{SCCKH}	Slave CCLK clock minimum High time	2.50	2.50	2.50	2.50	ns, Min
F _{SCCK}	Slave CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max
EMCCLK Input (Master Mode)						
T _{EMCCKL}	External master CCLK Low time	2.50	2.50	2.50	2.50	ns, Min
T _{EMCCKH}	External master CCLK High time	2.50	2.50	2.50	2.50	ns, Min
F _{EMCCK}	External master CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max
Internal Configuration Access Port						
F _{ICAPCK}	Internal configuration access port (ICAPE2)	100.00	100.00	100.00	70.00	MHz, Max

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