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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	32575
Number of Logic Elements/Cells	416960
Total RAM Bits	30781440
Number of I/O	400
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1156-BBGA, FCBGA
Supplier Device Package	1156-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7k420t-2ffg1156c

LVDS DC Specifications (LVDS_25)

The LVDS_25 standard is available in the HR I/O banks. See [UG471: 7 Series FPGAs SelectIO Resources User Guide](#) for more information.

Table 12: LVDS_25 DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.375	2.500	2.625	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.700	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.300	1.200	1.425	V

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks. See [UG471: 7 Series FPGAs SelectIO Resources User Guide](#) for more information.

Table 13: LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		1.710	1.800	1.890	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.825	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	350	600	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ± 350 mV	0.300	1.200	1.425	V

Table 18: Maximum Physical Interface (PHY) Rate for Memory Interfaces (FBG Packages)⁽¹⁾⁽²⁾

Memory Standard	I/O Bank Type	V _{CCAUX_IO} ⁽³⁾	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
4:1 Memory Controllers							
DDR3	HP	N/A	1333	1066	800	800	Mb/s
	HR	N/A	1066	800	800	800	Mb/s
DDR3L	HP	N/A	1066	800	667	667	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	N/A	800	800	800	800	Mb/s
	HR	N/A	800	667	667	667	Mb/s
RLDRAM III ⁽⁴⁾	HP	N/A	550	500	450	450	MHz
	HR	N/A	N/A				
2:1 Memory Controllers							
DDR3	HP	N/A	1066	1066	800	800	Mb/s
	HR	N/A	1066	800	800	800	Mb/s
DDR3L	HP	N/A	1066	800	667	667	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	N/A	800	800	800	800	Mb/s
	HR	N/A	800	667	667	667	Mb/s
QDR II+ ⁽⁵⁾	HP	N/A	550	500	450	450	MHz
	HR	N/A	450	400	350	350	MHz
RLDRAM II	HP	N/A	533	500	450	450	MHz
	HR	N/A					
LPDDR2 ⁽⁴⁾	HP	N/A	667	667	667	667	Mb/s
	HR	N/A	667	667	533	533	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see [UG586](#), *7 Series FPGAs Memory Interface Solutions User Guide*.
2. When using the internal V_{REF} the maximum data rate is 800 Mb/s (400 MHz).
3. FBG packages do not have separate V_{CCAUX_IO} supply pins to adjust the pre-driver voltage of the HP I/O banks.
4. RLDRAM III (BL = 4, BL = 8) and LPDDR2 specifications have not been validated with memory IP.
5. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standard	T _{IOP1}				T _{IOP0}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
DIFF_HSTL_II_DCI_F	0.75	0.79	0.92	0.76	0.97	1.08	1.15	1.30	1.61	1.84	1.97	1.91	ns
DIFF_HSTL_I_18_F	0.75	0.79	0.92	0.89	1.04	1.16	1.24	1.38	1.68	1.91	2.06	1.99	ns
DIFF_HSTL_II_18_F	0.75	0.79	0.92	0.89	0.98	1.09	1.16	1.40	1.62	1.85	1.98	2.01	ns
DIFF_HSTL_I_DCI_18_F	0.75	0.79	0.92	0.75	1.04	1.16	1.24	1.38	1.67	1.91	2.06	1.99	ns
DIFF_HSTL_II_DCI_18_F	0.75	0.79	0.92	0.75	0.98	1.09	1.16	1.33	1.61	1.85	1.98	1.94	ns
DIFF_HSTL_II_T_DCI_18_F	0.75	0.79	0.92	0.76	1.04	1.16	1.24	1.38	1.67	1.91	2.06	1.99	ns
LVC MOS18_S2	0.47	0.50	0.60	0.87	3.95	4.28	4.85	3.40	4.59	5.04	5.67	4.01	ns
LVC MOS18_S4	0.47	0.50	0.60	0.87	2.67	2.98	3.43	2.69	3.31	3.73	4.26	3.30	ns
LVC MOS18_S6	0.47	0.50	0.60	0.87	2.14	2.38	2.72	2.18	2.77	3.14	3.54	2.79	ns
LVC MOS18_S8	0.47	0.50	0.60	0.87	1.98	2.21	2.52	2.02	2.61	2.97	3.35	2.63	ns
LVC MOS18_S12	0.47	0.50	0.60	0.87	1.70	1.91	2.17	1.85	2.34	2.67	2.99	2.46	ns
LVC MOS18_S16	0.47	0.50	0.60	0.87	1.57	1.75	1.97	1.76	2.20	2.51	2.79	2.37	ns
LVC MOS18_F2	0.47	0.50	0.60	0.87	3.50	3.87	4.48	2.85	4.14	4.63	5.30	3.46	ns
LVC MOS18_F4	0.47	0.50	0.60	0.87	2.23	2.50	2.87	2.26	2.87	3.25	3.69	2.87	ns
LVC MOS18_F6	0.47	0.50	0.60	0.87	1.80	2.00	2.26	1.52	2.43	2.76	3.08	2.13	ns
LVC MOS18_F8	0.47	0.50	0.60	0.87	1.46	1.72	2.04	1.51	2.10	2.47	2.86	2.12	ns
LVC MOS18_F12	0.47	0.50	0.60	0.87	1.26	1.40	1.53	1.46	1.89	2.16	2.35	2.07	ns
LVC MOS18_F16	0.47	0.50	0.60	0.87	1.19	1.33	1.44	1.46	1.83	2.08	2.26	2.07	ns
LVC MOS15_S2	0.59	0.62	0.73	0.86	3.55	3.89	4.45	3.11	4.19	4.65	5.27	3.73	ns
LVC MOS15_S4	0.59	0.62	0.73	0.86	2.45	2.70	3.06	2.46	3.08	3.45	3.89	3.07	ns
LVC MOS15_S6	0.59	0.62	0.73	0.86	2.24	2.51	2.88	2.33	2.88	3.26	3.71	2.94	ns
LVC MOS15_S8	0.59	0.62	0.73	0.86	1.91	2.16	2.49	2.05	2.55	2.91	3.31	2.66	ns
LVC MOS15_S12	0.59	0.62	0.73	0.86	1.77	1.98	2.23	1.97	2.41	2.73	3.05	2.58	ns
LVC MOS15_S16	0.59	0.62	0.73	0.86	1.62	1.81	2.02	1.85	2.26	2.56	2.84	2.46	ns
LVC MOS15_F2	0.59	0.62	0.73	0.86	3.38	3.69	4.18	2.74	4.02	4.44	5.00	3.35	ns
LVC MOS15_F4	0.59	0.62	0.73	0.86	2.04	2.21	2.44	1.72	2.68	2.97	3.26	2.33	ns
LVC MOS15_F6	0.59	0.62	0.73	0.86	1.47	1.74	2.09	1.49	2.10	2.50	2.91	2.10	ns
LVC MOS15_F8	0.59	0.62	0.73	0.86	1.31	1.46	1.61	1.47	1.95	2.22	2.43	2.08	ns
LVC MOS15_F12	0.59	0.62	0.73	0.86	1.21	1.34	1.45	1.44	1.84	2.10	2.27	2.05	ns
LVC MOS15_F16	0.59	0.62	0.73	0.86	1.18	1.31	1.41	1.41	1.82	2.07	2.23	2.02	ns
LVC MOS12_S2	0.64	0.67	0.78	0.95	3.38	3.80	4.48	3.27	4.02	4.55	5.30	3.88	ns
LVC MOS12_S4	0.64	0.67	0.78	0.95	2.62	2.94	3.43	2.76	3.26	3.70	4.25	3.37	ns
LVC MOS12_S6	0.64	0.67	0.78	0.95	2.05	2.33	2.72	2.24	2.69	3.08	3.54	2.85	ns
LVC MOS12_S8	0.64	0.67	0.78	0.95	1.94	2.18	2.51	2.16	2.58	2.94	3.33	2.77	ns
LVC MOS12_F2	0.64	0.67	0.78	0.95	2.84	3.15	3.62	2.47	3.48	3.90	4.44	3.08	ns
LVC MOS12_F4	0.64	0.67	0.78	0.95	1.97	2.18	2.44	1.69	2.61	2.93	3.26	2.30	ns
LVC MOS12_F6	0.64	0.67	0.78	0.95	1.33	1.51	1.70	1.43	1.96	2.26	2.52	2.04	ns

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
SSTL18_I_F	0.68	0.72	0.82	0.86	0.94	1.06	1.15	1.32	1.58	1.82	1.97	1.93	ns
SSTL18_II_F	0.68	0.72	0.82	0.87	0.97	1.09	1.16	1.36	1.61	1.84	1.99	1.98	ns
SSTL18_I_DCI_F	0.68	0.72	0.82	0.76	0.89	1.02	1.10	1.30	1.53	1.77	1.92	1.91	ns
SSTL18_II_DCI_F	0.68	0.72	0.82	0.78	0.89	1.02	1.10	1.24	1.53	1.77	1.92	1.85	ns
SSTL18_II_T_DCI_F	0.68	0.72	0.82	0.78	0.89	1.02	1.10	1.27	1.53	1.77	1.92	1.88	ns
SSTL15_F	0.68	0.72	0.82	0.81	0.89	1.01	1.09	1.24	1.53	1.77	1.91	1.85	ns
SSTL15_DCI_F	0.68	0.72	0.82	0.78	0.89	1.01	1.09	1.27	1.53	1.77	1.91	1.88	ns
SSTL15_T_DCI_F	0.68	0.72	0.82	0.80	0.89	1.01	1.09	1.27	1.53	1.77	1.91	1.88	ns
SSTL135_F	0.69	0.72	0.82	0.89	0.88	1.00	1.08	1.27	1.52	1.76	1.90	1.88	ns
SSTL135_DCI_F	0.69	0.72	0.82	0.84	0.89	1.00	1.08	1.27	1.52	1.76	1.90	1.88	ns
SSTL135_T_DCI_F	0.69	0.72	0.82	0.84	0.89	1.00	1.08	1.27	1.52	1.76	1.90	1.88	ns
SSTL12_F	0.69	0.72	0.82	0.95	0.88	1.00	1.08	1.26	1.52	1.76	1.90	1.87	ns
SSTL12_DCI_F	0.69	0.72	0.82	0.91	0.91	1.03	1.11	1.24	1.54	1.79	1.93	1.85	ns
SSTL12_T_DCI_F	0.69	0.72	0.82	0.91	0.91	1.03	1.11	1.26	1.54	1.79	1.93	1.87	ns
DIFF_SSTL18_I_F	0.75	0.79	0.92	0.89	0.94	1.06	1.15	1.38	1.58	1.82	1.97	1.99	ns
DIFF_SSTL18_II_F	0.75	0.79	0.92	0.89	0.97	1.09	1.16	1.40	1.61	1.84	1.99	2.01	ns
DIFF_SSTL18_I_DCI_F	0.75	0.79	0.92	0.76	0.89	1.02	1.10	1.36	1.53	1.77	1.92	1.98	ns
DIFF_SSTL18_II_DCI_F	0.75	0.79	0.92	0.75	0.89	1.02	1.10	1.32	1.53	1.77	1.92	1.93	ns
DIFF_SSTL18_II_T_DCI_F	0.75	0.79	0.92	0.76	0.89	1.02	1.10	1.38	1.53	1.77	1.92	1.99	ns
DIFF_SSTL15_F	0.68	0.72	0.82	0.89	0.89	1.01	1.09	1.24	1.53	1.77	1.91	1.85	ns
DIFF_SSTL15_DCI_F	0.68	0.72	0.82	0.75	0.89	1.01	1.09	1.27	1.53	1.77	1.91	1.88	ns
DIFF_SSTL15_T_DCI_F	0.68	0.72	0.82	0.76	0.89	1.01	1.09	1.35	1.53	1.77	1.91	1.96	ns
DIFF_SSTL135_F	0.69	0.72	0.82	0.91	0.88	1.00	1.08	1.27	1.52	1.76	1.90	1.88	ns
DIFF_SSTL135_DCI_F	0.69	0.72	0.82	0.76	0.89	1.00	1.08	1.27	1.52	1.76	1.90	1.88	ns
DIFF_SSTL135_T_DCI_F	0.69	0.72	0.82	0.76	0.89	1.00	1.08	1.35	1.52	1.76	1.90	1.96	ns
DIFF_SSTL12_F	0.69	0.72	0.82	0.91	0.88	1.00	1.08	1.26	1.52	1.76	1.90	1.87	ns
DIFF_SSTL12_DCI_F	0.69	0.72	0.82	0.78	0.91	1.03	1.11	1.24	1.54	1.79	1.93	1.85	ns
DIFF_SSTL12_T_DCI_F	0.69	0.72	0.82	0.80	0.91	1.03	1.11	1.33	1.54	1.79	1.93	1.94	ns

Notes:

1. This I/O standard is only available in the 1.8V high-performance (HP) banks.

Output Serializer/Deserializer Switching Characteristics

Table 25: OSERDES Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T _{OSDCK_D} /T _{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	0.37/0.02	0.40/0.02	0.55/0.02	0.44/−0.24	ns
T _{OSDCK_T} /T _{OSCKD_T} ⁽¹⁾	T input Setup/Hold with respect to CLK	0.49/−0.15	0.56/−0.15	0.68/−0.15	0.67/−0.25	ns
T _{OSDCK_T2} /T _{OSCKD_T2} ⁽¹⁾	T input Setup/Hold with respect to CLKDIV	0.27/−0.15	0.30/−0.15	0.34/−0.15	0.46/−0.25	ns
T _{OSCCK_OCE} /T _{OSCKC_OCE}	OCE input Setup/Hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	0.35/−0.15	ns
T _{OSCCK_S}	SR (Reset) input Setup with respect to CLKDIV	0.41	0.46	0.75	0.70	ns
T _{OSCCK_TCE} /T _{OSCKC_TCE}	TCE input Setup/Hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	0.31/−0.15	ns
Sequential Delays						
T _{OSCKO_OQ}	Clock to out from CLK to OQ	0.35	0.37	0.42	0.54	ns
T _{OSCKO_TQ}	Clock to out from CLK to TQ	0.41	0.43	0.49	0.63	ns
Combinatorial						
T _{OSDO_TTQ}	T input to TQ Out	0.73	0.81	0.97	1.18	ns

Notes:

- T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in TRACE report.

Input/Output Delay Switching Characteristics

Table 26: Input/Output Delay Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
IDELAYCTRL						
T _{DLYCCO_RDY}	Reset to Ready for IDELAYCTRL	3.22	3.22	3.22	3.22	µs
F _{IDELAYCTRL_REF}	Attribute REFCLK frequency = 200.00 ⁽¹⁾	200.00	200.00	200.00	200.00	MHz
	Attribute REFCLK frequency = 300.00 ⁽¹⁾	300.00	300.00	N/A	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	±10	MHz
T _{IDELAYCTRL_RPW}	Minimum Reset pulse width	52.00	52.00	52.00	52.00	ns
IDELAY/ODELAY						
T _{IDELAYRESOLUTION}	IDELAY/ODELAY chain delay resolution	1/(32 x 2 x F _{REF})				ps
T _{IDELAYPAT_JIT} and T _{ODELAYPAT_JIT}	Pattern dependent period jitter in delay chain for clock pattern. ⁽²⁾	0	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23) ⁽³⁾	±5	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23) ⁽⁴⁾	±9	±9	±9	±9	ps per tap
T _{IDELAY_CLK_MAX} / T _{ODELAY_CLK_MAX}	Maximum frequency of CLK input to IDELAY/ODELAY	800.00	800.00	710.00	710.00	MHz
T _{IDCCK_CE} / T _{IDCKC_CE}	CE pin Setup/Hold with respect to C for IDELAY	0.11/0.10	0.14/0.12	0.18/0.14	0.14/0.16	ns
T _{ODCCK_CE} / T _{ODCKC_CE}	CE pin Setup/Hold with respect to C for ODELAY	0.14/0.03	0.16/0.04	0.19/0.05	0.28/0.06	ns
T _{IDCCK_INC} / T _{IDCKC_INC}	INC pin Setup/Hold with respect to C for IDELAY	0.10/0.14	0.12/0.16	0.14/0.20	0.10/0.23	ns
T _{ODCCK_INC} / T _{ODCKC_INC}	INC pin Setup/Hold with respect to C for ODELAY	0.10/0.07	0.12/0.08	0.13/0.09	0.19/0.16	ns
T _{IDCCK_RST} / T _{IDCKC_RST}	RST pin Setup/Hold with respect to C for IDELAY	0.13/0.08	0.14/0.10	0.16/0.12	0.22/0.19	ns
T _{ODCCK_RST} / T _{ODCKC_RST}	RST pin Setup/Hold with respect to C for ODELAY	0.16/0.04	0.19/0.06	0.24/0.08	0.32/0.11	ns
T _{IDDO_IDATAIN}	Propagation delay through IDELAY	Note 5	Note 5	Note 5	Note 5	ps
T _{ODDO_ODATAIN}	Propagation delay through ODELAY	Note 5	Note 5	Note 5	Note 5	ps

Notes:

1. Average Tap Delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY/ODELAY tap setting. See TRACE report for actual values.

Block RAM and FIFO Switching Characteristics

Table 31: Block RAM and FIFO Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Block RAM and FIFO Clock-to-Out Delays						
T_{RCKO_DO} and $T_{RCKO_DO_REG}^{(1)}$	Clock CLK to DOUT output (without output register) ⁽²⁾⁽³⁾	1.57	1.80	2.08	2.44	ns, Max
	Clock CLK to DOUT output (with output register) ⁽⁴⁾⁽⁵⁾	0.54	0.63	0.75	0.86	ns, Max
$T_{RCKO_DO_ECC}$ and $T_{RCKO_DO_ECC_REG}$	Clock CLK to DOUT output with ECC (without output register) ⁽²⁾⁽³⁾	2.35	2.58	3.26	4.49	ns, Max
	Clock CLK to DOUT output with ECC (with output register) ⁽⁴⁾⁽⁵⁾	0.62	0.69	0.80	0.94	ns, Max
$T_{RCKO_DO_CASCOU}$ and $T_{RCKO_DO_CASCOU_REG}$	Clock CLK to DOUT output with Cascade (without output register) ⁽²⁾	2.21	2.45	2.80	3.19	ns, Max
	Clock CLK to DOUT output with Cascade (with output register) ⁽⁴⁾	0.98	1.08	1.24	1.32	ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs ⁽⁶⁾	0.65	0.74	0.89	0.97	ns, Max
$T_{RCKO_POINTERS}$	Clock CLK to FIFO pointers outputs ⁽⁷⁾	0.79	0.87	0.98	1.10	ns, Max
$T_{RCKO_PARITY_ECC}$	Clock CLK to ECCPARITY in ECC encode only mode	0.66	0.72	0.80	0.93	ns, Max
$T_{RCKO_SDBIT_ECC}$ and $T_{RCKO_SDBIT_ECC_REG}$	Clock CLK to BITERR (without output register)	2.17	2.38	3.01	4.15	ns, Max
	Clock CLK to BITERR (with output register)	0.57	0.65	0.76	0.89	ns, Max
$T_{RCKO_RDADDR_ECC}$ and $T_{RCKO_RDADDR_ECC_REG}$	Clock CLK to RDADDR output with ECC (without output register)	0.64	0.74	0.90	0.98	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.71	0.79	0.92	1.10	ns, Max
Setup and Hold Times Before/After Clock CLK						
$T_{RCK_ADDR}/T_{RCKC_ADDR}$	ADDR inputs ⁽⁸⁾	0.38/0.27	0.42/0.28	0.48/0.31	0.65/0.38	ns, Min
$T_{RDCK_DI_WF_NC}/T_{RCKD_DI_WF_NC}$	Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode ⁽⁹⁾	0.49/0.51	0.55/0.53	0.63/0.57	0.78/0.64	ns, Min
$T_{RDCK_DI_RF}/T_{RCKD_DI_RF}$	Data input setup/hold time when block RAM is configured in READ_FIRST mode ⁽⁹⁾	0.17/0.25	0.19/0.29	0.21/0.35	0.25/0.32	ns, Min
$T_{RDCK_DI_ECC}/T_{RCKD_DI_ECC}$	DIN inputs with block RAM ECC in standard mode ⁽⁹⁾	0.42/0.37	0.47/0.39	0.53/0.43	0.66/0.46	ns, Min
$T_{RDCK_DI_ECCW}/T_{RCKD_DI_ECCW}$	DIN inputs with block RAM ECC encode only ⁽⁹⁾	0.79/0.37	0.87/0.39	0.99/0.43	1.17/0.41	ns, Min
$T_{RDCK_DI_ECC_FIFO}/T_{RCKD_DI_ECC_FIFO}$	DIN inputs with FIFO ECC in standard mode ⁽⁹⁾	0.89/0.47	0.98/0.50	1.12/0.54	1.32/0.65	ns, Min
$T_{RCK_INJECTBITERR}/T_{RCKC_INJECTBITERR}$	Inject single/double bit error in ECC mode	0.49/0.30	0.55/0.31	0.63/0.34	0.78/0.41	ns, Min
T_{RCK_EN}/T_{RCKC_EN}	Block RAM Enable (EN) input	0.30/0.17	0.33/0.18	0.38/0.20	0.48/0.22	ns, Min
$T_{RCK_REGCE}/T_{RCKC_REGCE}$	CE input of output register	0.21/0.13	0.25/0.13	0.31/0.14	0.34/0.16	ns, Min
$T_{RCK_RSTREG}/T_{RCKC_RSTREG}$	Synchronous RSTREG input	0.25/0.06	0.27/0.06	0.29/0.06	0.35/0.06	ns, Min

DSP48E1 Switching Characteristics

Table 32: DSP48E1 Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock						
T _{DSPDCK_A_AREG} /T _{DSPCKD_A_AREG}	A input to A register CLK	0.24/ 0.12	0.27/ 0.14	0.31/ 0.16	0.38/ 0.12	ns
T _{DSPDCK_B_BREG} /T _{DSPCKD_B_BREG}	B input to B register CLK	0.28/ 0.13	0.32/ 0.14	0.39/ 0.15	0.51/ 0.16	ns
T _{DSPDCK_C_CREG} /T _{DSPCKD_C_CREG}	C input to C register CLK	0.15/ 0.15	0.17/ 0.17	0.20/ 0.20	0.31/ 0.21	ns
T _{DSPDCK_D_DREG} /T _{DSPCKD_D_DREG}	D input to D register CLK	0.21/ 0.19	0.27/ 0.22	0.35/ 0.26	0.46/ 0.20	ns
T _{DSPDCK_ACIN_AREG} /T _{DSPCKD_ACIN_AREG}	ACIN input to A register CLK	0.21/ 0.12	0.24/ 0.14	0.27/ 0.16	0.31/ 0.12	ns
T _{DSPDCK_BCIN_BREG} /T _{DSPCKD_BCIN_BREG}	BCIN input to B register CLK	0.22/ 0.13	0.25/ 0.14	0.30/ 0.15	0.34/ 0.16	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock						
T _{DSPDCK_{A, B}_MREG_MULT} / T _{DSPCKD_B_MREG_MULT}	{A, B,} input to M register CLK using multiplier	2.04/ −0.01	2.34/ −0.01	2.79/ −0.01	3.66/ −0.06	ns
T _{DSPDCK_{A, B}_ADREG} / T _{DSPCKD_D_ADREG}	{A, D} input to AD register CLK	1.09/ −0.02	1.25/ −0.02	1.49/ −0.02	1.94/ −0.23	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock						
T _{DSPDCK_{A, B}_PREG_MULT} / T _{DSPCKD_{A, B}_PREG_MULT}	{A, B,} input to P register CLK using multiplier	3.41/ −0.24	3.90/ −0.24	4.64/ −0.24	5.89/ −0.41	ns
T _{DSPDCK_D_PREG_MULT} / T _{DSPCKD_D_PREG_MULT}	D input to P register CLK using multiplier	3.33/ −0.62	3.81/ −0.62	4.53/ −0.62	5.70/ −1.42	ns
T _{DSPDCK_{A, B}_PREG} / T _{DSPCKD_{A, B}_PREG}	A or B input to P register CLK not using multiplier	1.47/ −0.24	1.68/ −0.24	2.00/ −0.24	2.37/ −0.41	ns
T _{DSPDCK_C_PREG} / T _{DSPCKD_C_PREG}	C input to P register CLK not using multiplier	1.30/ −0.22	1.49/ −0.22	1.78/ −0.22	2.11/ −0.36	ns
T _{DSPDCK_PCIN_PREG} / T _{DSPCKD_PCIN_PREG}	PCIN input to P register CLK	1.12/ −0.13	1.28/ −0.13	1.52/ −0.13	1.81/ −0.21	ns
Setup and Hold Times of the CE Pins						
T _{DSPDCK_{CEA;CEB}_{AREG;BREG}} / T _{DSPCKD_{CEA;CEB}_{AREG;BREG}}	{CEA; CEB} input to {A; B} register CLK	0.30/ 0.05	0.36/ 0.06	0.44/ 0.09	0.55/ 0.09	ns
T _{DSPDCK_CEC_CREG} / T _{DSPCKD_CEC_CREG}	CEC input to C register CLK	0.24/ 0.08	0.29/ 0.09	0.36/ 0.11	0.43/ 0.11	ns
T _{DSPDCK_CED_DREG} / T _{DSPCKD_CED_DREG}	CED input to D register CLK	0.31/ −0.02	0.36/ −0.02	0.44/ −0.02	0.58/ 0.12	ns
T _{DSPDCK_CEM_MREG} / T _{DSPCKD_CEM_MREG}	CEM input to M register CLK	0.26/ 0.15	0.29/ 0.17	0.33/ 0.20	0.39/ 0.25	ns
T _{DSPDCK_CEP_PREG} / T _{DSPCKD_CEP_PREG}	CEP input to P register CLK	0.31/ 0.01	0.36/ 0.01	0.45/ 0.01	0.54/ 0.00	ns

Table 32: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup and Hold Times of the RST Pins						
$T_{\text{DSPDCK}_{\{\text{RSTA}; \text{RSTB}\}}_{\{\text{AREG}; \text{BREG}\}}/T_{\text{DSPCKD}_{\{\text{RSTA}; \text{RSTB}\}}_{\{\text{AREG}; \text{BREG}\}}}$	{RSTA, RSTB} input to {A, B} register CLK	0.34/ 0.10	0.39/ 0.11	0.47/ 0.13	0.53/ 0.34	ns
$T_{\text{DSPDCK_RSTC_CREG}}/T_{\text{DSPCKD_RSTC_CREG}}$	RSTC input to C register CLK	0.06/ 0.22	0.07/ 0.24	0.08/ 0.26	0.08/ 0.31	ns
$T_{\text{DSPDCK_RSTD_DREG}}/T_{\text{DSPCKD_RSTD_DREG}}$	RSTD input to D register CLK	0.37/ 0.06	0.42/ 0.06	0.50/ 0.07	0.57/ 0.07	ns
$T_{\text{DSPDCK_RSTM_MREG}}/T_{\text{DSPCKD_RSTM_MREG}}$	RSTM input to M register CLK	0.18/ 0.18	0.20/ 0.21	0.23/ 0.24	0.24/ 0.29	ns
$T_{\text{DSPDCK_RSTP_PREG}}/T_{\text{DSPCKD_RSTP_PREG}}$	RSTP input to P register CLK	0.24/ 0.01	0.26/ 0.01	0.30/ 0.01	0.37/ 0.00	ns
Combinatorial Delays from Input Pins to Output Pins						
$T_{\text{DSPDO_A_CARRYOUT_MULT}}$	A input to CARRYOUT output using multiplier	3.21	3.69	4.39	5.60	ns
$T_{\text{DSPDO_D_P_MULT}}$	D input to P output using multiplier	3.15	3.61	4.30	5.44	ns
$T_{\text{DSPDO_A_P}}$	A input to P output not using multiplier	1.30	1.48	1.76	2.10	ns
$T_{\text{DSPDO_C_P}}$	C input to P output	1.13	1.30	1.55	1.84	ns
Combinatorial Delays from Input Pins to Cascading Output Pins						
$T_{\text{DSPDO}_{\{\text{A}; \text{B}\}}_{\{\text{ACOUT}; \text{BCOUT}\}}}$	{A, B} input to {ACOUT, BCOUT} output	0.47	0.53	0.63	0.75	ns
$T_{\text{DSPDO}_{\{\text{A}; \text{B}\}}_{\text{CARRYCASCOUT_MULT}}}$	{A, B} input to CARRYCASCOUT output using multiplier	3.44	3.94	4.69	5.96	ns
$T_{\text{DSPDO_D_CARRYCASCOUT_MULT}}$	D input to CARRYCASCOUT output using multiplier	3.36	3.85	4.58	5.77	ns
$T_{\text{DSPDO}_{\{\text{A}; \text{B}\}}_{\text{CARRYCASCOUT}}}$	{A, B} input to CARRYCASCOUT output not using multiplier	1.50	1.72	2.04	2.44	ns
$T_{\text{DSPDO_C_CARRYCASCOUT}}$	C input to CARRYCASCOUT output	1.34	1.53	1.83	2.18	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins						
$T_{\text{DSPDO_ACIN_P_MULT}}$	ACIN input to P output using multiplier	3.09	3.55	4.24	5.42	ns
$T_{\text{DSPDO_ACIN_P}}$	ACIN input to P output not using multiplier	1.16	1.33	1.59	2.07	ns
$T_{\text{DSPDO_ACIN_ACOUT}}$	ACIN input to ACOUT output	0.32	0.37	0.45	0.53	ns
$T_{\text{DSPDO_ACIN_CARRYCASCOUT_MULT}}$	ACIN input to CARRYCASCOUT output using multiplier	3.30	3.79	4.52	5.76	ns
$T_{\text{DSPDO_ACIN_CARRYCASCOUT}}$	ACIN input to CARRYCASCOUT output not using multiplier	1.37	1.57	1.87	2.40	ns
$T_{\text{DSPDO_PCIN_P}}$	PCIN input to P output	0.94	1.08	1.29	1.54	ns
$T_{\text{DSPDO_PCIN_CARRYCASCOUT}}$	PCIN input to CARRYCASCOUT output	1.15	1.32	1.57	1.88	ns
Clock to Outs from Output Register Clock to Output Pins						
$T_{\text{DSPCKO_P_PREG}}$	CLK PREG to P output	0.33	0.35	0.39	0.45	ns
$T_{\text{DSPCKO_CARRYCASCOUT_PREG}}$	CLK PREG to CARRYCASCOUT output	0.44	0.50	0.59	0.71	ns

Table 32: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Clock to Outs from Pipeline Register Clock to Output Pins						
T_DSPCKO_P_MREG	CLK MREG to P output	1.42	1.64	1.96	2.31	ns
T_DSPCKO_CARRYCASCOUT_MREG	CLK MREG to CARRYCASCOUT output	1.63	1.87	2.24	2.65	ns
T_DSPCKO_P_ADREG_MULT	CLK ADREG to P output using multiplier	2.30	2.63	3.13	3.90	ns
T_DSPCKO_CARRYCASCOUT_ADREG_MULT	CLK ADREG to CARRYCASCOUT output using multiplier	2.51	2.87	3.41	4.23	ns
Clock to Outs from Input Register Clock to Output Pins						
T_DSPCKO_P_AREG_MULT	CLK AREG to P output using multiplier	3.34	3.83	4.55	5.80	ns
T_DSPCKO_P_BREG	CLK BREG to P output not using multiplier	1.39	1.59	1.88	2.24	ns
T_DSPCKO_P_CREG	CLK CREG to P output not using multiplier	1.43	1.64	1.95	2.32	ns
T_DSPCKO_P_DREG_MULT	CLK DREG to P output using multiplier	3.32	3.80	4.51	5.74	ns
Clock to Outs from Input Register Clock to Cascading Output Pins						
T_DSPCKO_{ACOUT; BCOUT}_{AREG; BREG}	CLK (ACOUT, BCOUT) to {A,B} register output	0.55	0.62	0.74	0.87	ns
T_DSPCKO_CARRYCASCOUT_{AREG, BREG}_MULT	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier	3.55	4.06	4.84	6.13	ns
T_DSPCKO_CARRYCASCOUT_BREG	CLK BREG to CARRYCASCOUT output not using multiplier	1.60	1.82	2.16	2.58	ns
T_DSPCKO_CARRYCASCOUT_DREG_MULT	CLK DREG to CARRYCASCOUT output using multiplier	3.52	4.03	4.79	6.07	ns
T_DSPCKO_CARRYCASCOUT_CREG	CLK CREG to CARRYCASCOUT output	1.64	1.88	2.23	2.65	ns
Maximum Frequency						
F_MAX	With all registers used	741.84	650.20	547.95	429.37	MHz
F_MAX_PATDET	With pattern detector	627.35	549.75	463.61	365.90	MHz
F_MAX_MULT_NOMREG	Two register multiply without MREG	412.20	360.75	303.77	248.32	MHz
F_MAX_MULT_NOMREG_PATDET	Two register multiply without MREG with pattern detect	374.25	327.65	276.01	225.73	MHz
F_MAX_PREADD_MULT_NOADREG	Without ADREG	468.82	408.66	342.70	263.44	MHz
F_MAX_PREADD_MULT_NOADREG_PATDET	Without ADREG with pattern detect	468.82	408.66	342.70	263.44	MHz
F_MAX_NOPIPELINEREG	Without pipeline registers (MREG, ADREG)	306.84	267.81	225.02	177.15	MHz
F_MAX_NOPIPELINEREG_PATDET	Without pipeline registers (MREG, ADREG) with pattern detect	285.23	249.13	209.38	165.32	MHz

Table 39: PLL Specification (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
PLL_F _{PFDMAX}	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized	550.00	500.00	450.00	450.00	MHz
	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	300.00	300.00	300.00	300.00	MHz
PLL_F _{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	19.00	19.00	19.00	19.00	MHz
PLL_T _{FBDELAY}	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle				
Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK						
T _{PLLCKC_DADDR} / T _{PLLCKC_DADDR}	Setup and hold of D address	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{PLLCKC_DI} / T _{PLLCKC_DI}	Setup and hold of D input	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{PLLCKC_DEN} / T _{PLLCKC_DEN}	Setup and hold of D enable	1.76/0.00	1.97/0.00	2.29/0.00	2.40/0.00	ns, Min
T _{PLLCKC_DWE} / T _{PLLCKC_DWE}	Setup and hold of D write enable	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{PLLCKO_DRDY}	CLK to out of DRDY	0.65	0.72	0.99	0.70	ns, Max
F _{DCK}	DCLK frequency	200.00	200.00	200.00	100.00	MHz, Max

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 40: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL.							
T _{ICKOF}	Clock-capable clock input and OUTFF <i>without</i> MMCM/PLL (near clock region)	XC7K70T	4.98	5.49	6.17	7.04	ns
		XC7K160T	5.23	5.77	6.48	7.38	ns
		XC7K325T	5.72	6.31	7.09	8.07	ns
		XC7K355T	5.34	5.87	6.57	7.51	ns
		XC7K410T	5.84	6.44	7.22	8.21	ns
		XC7K420T	5.50	6.04	6.77	7.73	ns
		XC7K480T	5.50	6.04	6.77	7.73	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 41: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL.							
T _{ICKOFFAR}	Clock-capable clock input and OUTFF <i>without</i> MMCM/PLL (far clock region)	XC7K70T	5.29	5.83	6.55	7.47	ns
		XC7K160T	5.84	6.45	7.24	8.24	ns
		XC7K325T	6.33	6.99	7.84	8.92	ns
		XC7K355T	5.95	6.55	7.32	8.36	ns
		XC7K410T	6.45	7.12	7.97	9.07	ns
		XC7K420T	6.41	7.06	7.90	9.01	ns
		XC7K480T	6.41	7.06	7.90	9.01	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 42: Clock-Capable Clock Input to Output Delay With MMCM

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> MMCM.							
T _{ICKOFMMCMCC}	Clock-capable clock input and OUTFF <i>with</i> MMCM	XC7K70T	0.95	0.95	0.95	1.74	ns
		XC7K160T	0.96	0.96	0.96	1.78	ns
		XC7K325T	1.00	1.00	1.00	1.82	ns
		XC7K355T	1.00	1.00	1.00	1.78	ns
		XC7K410T	1.00	1.00	1.00	1.82	ns
		XC7K420T	1.07	1.07	1.07	1.82	ns
		XC7K480T	1.07	1.07	1.07	1.82	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 43: Clock-Capable Clock Input to Output Delay With PLL

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> PLL.							
T _{ICKOFPLLCC}	Clock-capable clock input and OUTFF <i>with</i> PLL	XC7K70T	0.84	0.84	0.84	1.45	ns
		XC7K160T	0.89	0.89	0.89	1.54	ns
		XC7K325T	0.89	0.89	0.89	1.54	ns
		XC7K355T	0.89	0.89	0.89	1.50	ns
		XC7K410T	0.89	0.89	0.89	1.54	ns
		XC7K420T	0.96	0.96	0.96	1.54	ns
		XC7K480T	0.96	0.96	0.96	1.54	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Table 44: Pin-to-Pin, Clock-to-Out using BUFIO

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> BUFIO.						
T _{ICKOFCS}	Clock-to-Out of I/O clock for HR I/O banks	4.93	5.52	6.20	6.97	ns
	Clock-to-Out of I/O clock for HP I/O banks	4.85	5.44	6.11	6.90	ns

Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Kintex-7 FPGA clock transmitter and receiver data-valid windows.

Table 50: Package Skew

Symbol	Description	Device	Package	Value	Units
T _{PKGSKEW}	Package Skew ⁽¹⁾	XC7K70T	FBG484	108	ps
			FBG676	135	ps
		XC7K160T	FBG484	118	ps
			FBG676	136	ps
			FFG676	161	ps
		XC7K325T	FBG676	146	ps
			FFG676	154	ps
			FBG900	163	ps
			FFG900	161	ps
		XC7K355T	FFG901	149	ps
		XC7K410T	FBG676	165	ps
			FFG676	168	ps
			FBG900	151	ps
			FFG900	146	ps
		XC7K420T	FFG901	149	ps
			FFG1156	145	ps
		XC7K480T	FFG901	149	ps
			FFG1156	145	ps

Notes:

- These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
- Package delay information is available for these device/package combinations. This information can be used to deskew the package.

Table 53: GTX Transceiver Performance (Cont'd)

Symbol	Description	Output Divider	Speed Grade								Units
			1.0V						0.9V		
			-3		-2/-2L		-1 ⁽¹⁾		-2L ⁽²⁾		
			Package Type								
			FF	FB	FF	FB	FF	FB	FF	FB	
F _{GQPLL} RANGE2	GTX transceiver QPLL frequency range 2		9.8—12.5		9.8—10.3125		N/A		N/A		GHz

Notes:

1. The -1 speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s.
2. The -2L (0.9V) speed grade requires a 4-byte internal data width for operation above 3.8 Gb/s.
3. Data rates between 8.0 Gb/s and 9.8 Gb/s are not available.
4. For QPLL line rate range 2, the maximum line rate with the divider N set to 66 is 10.3125Gb/s.

Table 54: GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
F _{GTXDRPCLK}	GTXDRPCLK maximum frequency	175.01	175.01	156.25	125.00	MHz

Table 55: GTX Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F _{GCLK}	Reference clock frequency range	-3 speed grade	60	–	700	MHz
		All other speed grades	60	–	670	MHz
T _{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T _{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T _{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

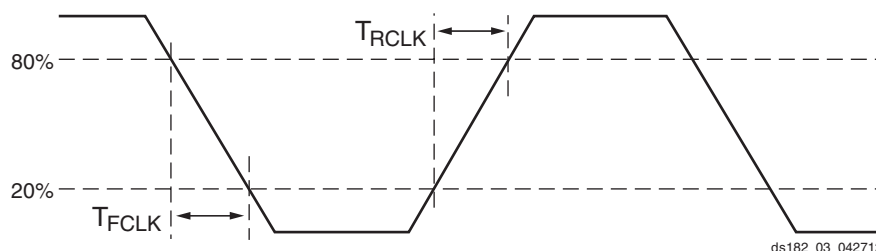


Figure 3: Reference Clock Timing Parameters

Table 56: GTX Transceiver PLL /Lock Time Adaptation

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T _{LOCK}	Initial PLL lock		–	–	1	ms
T _{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37 x10 ⁶	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3 x10 ⁶	UI

Table 57: GTX Transceiver User Clock Switching Characteristics⁽¹⁾⁽²⁾

Symbol	Description	Conditions	Speed Grade				Units
			1.0V			0.9V	
			-3 ⁽³⁾	-2/-2L ⁽³⁾	-1 ⁽⁴⁾	-2L ⁽⁵⁾	
F _{TXOUT}	TXOUTCLK maximum frequency		412.54	412.54	312.50	237.53	MHz
F _{RXOUT}	RXOUTCLK maximum frequency		412.54	412.54	312.50	237.53	MHz
F _{TXIN}	TXUSRCLK maximum frequency	16-bit data path	412.54	412.54	312.50	237.53	MHz
		32-bit data path	391.08	322.37	250.00	206.27	MHz
F _{RXIN}	RXUSRCLK maximum frequency	16-bit data path	412.54	412.54	312.50	237.53	MHz
		32-bit data path	391.08	322.37	250.00	206.27	MHz
F _{TXIN2}	TXUSRCLK2 maximum frequency	16-bit data path	412.54	412.54	312.50	237.53	MHz
		32-bit data path	391.08	322.37	250.00	206.27	MHz
		64-bit data path	195.54	161.19	125.00	103.14	MHz
F _{RXIN2}	RXUSRCLK2 maximum frequency	16-bit data path	412.54	412.54	312.50	237.53	MHz
		32-bit data path	391.08	322.37	250.00	206.27	MHz
		64-bit data path	195.54	161.19	125.00	103.14	MHz

Notes:

1. Clocking must be implemented as described in [UG476: 7 Series FPGAs GTX/GTH Transceiver User Guide](#).
2. These frequencies are not supported for all possible transceiver configurations.
3. For speed grades -3, -2, -2L (1.0V), a 16-bit data path can only be used for speeds less than 6.6 Gb/s.
4. For speed grade -1, a 16-bit data path can only be used for speeds less than 5.0 Gb/s.
5. For speed grade -2L (0.9V), a 16-bit data path can only be used for speeds less than 3.8 Gb/s.

Table 58: GTX Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F _{GTXTX}	Serial data rate range		0.500	–	F _{GTXMAX}	Gb/s
T _{RTX}	TX Rise time	20%–80%	–	40	–	ps
T _{FTX}	TX Fall time	80%–20%	–	40	–	ps
T _{LLSKEW}	TX lane-to-lane skew ⁽¹⁾		–	–	500	ps
V _{TXOOBVDPP}	Electrical idle amplitude		–	–	15	mV
T _{TXOOBTRANSITION}	Electrical idle transition time		–	–	140	ns
TJ _{12.5}	Total Jitter ⁽²⁾⁽⁴⁾	12.5 Gb/s	–	–	0.28	UI
DJ _{12.5}	Deterministic Jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI
TJ _{11.18}	Total Jitter ⁽²⁾⁽⁴⁾	11.18 Gb/s	–	–	0.28	UI
DJ _{11.18}	Deterministic Jitter ⁽²⁾⁽⁴⁾		–	–	0.17	UI

Table 58: GTX Transceiver Transmitter Switching Characteristics (Cont'd)

Symbol	Description	Condition	Min	Typ	Max	Units
TJ _{10.3125}	Total Jitter ⁽²⁾⁽⁴⁾	10.3125 Gb/s	—	—	0.28	UI
DJ _{10.3125}	Deterministic Jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{9.953}	Total Jitter ⁽²⁾⁽⁴⁾	9.953 Gb/s	—	—	0.28	UI
DJ _{9.953}	Deterministic Jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{9.8}	Total Jitter ⁽²⁾⁽⁴⁾	9.8 Gb/s	—	—	0.28	UI
DJ _{9.8}	Deterministic Jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{8.0}	Total Jitter ⁽²⁾⁽⁴⁾	8.0 Gb/s	—	—	0.30	UI
DJ _{8.0}	Deterministic Jitter ⁽²⁾⁽⁴⁾		—	—	0.15	UI
TJ _{6.6_QPLL}	Total Jitter ⁽²⁾⁽⁴⁾	6.6 Gb/s	—	—	0.28	UI
DJ _{6.6_QPLL}	Deterministic Jitter ⁽²⁾⁽⁴⁾		—	—	0.17	UI
TJ _{6.6_CPLL}	Total Jitter ⁽³⁾⁽⁴⁾	6.6 Gb/s	—	—	0.30	UI
DJ _{6.6_CPLL}	Deterministic Jitter ⁽³⁾⁽⁴⁾		—	—	0.15	UI
TJ _{5.0}	Total Jitter ⁽³⁾⁽⁴⁾	5.0 Gb/s	—	—	0.30	UI
DJ _{5.0}	Deterministic Jitter ⁽³⁾⁽⁴⁾		—	—	0.15	UI
TJ _{4.25}	Total Jitter ⁽³⁾⁽⁴⁾	4.25 Gb/s	—	—	0.30	UI
DJ _{4.25}	Deterministic Jitter ⁽³⁾⁽⁴⁾		—	—	0.15	UI
TJ _{3.75}	Total Jitter ⁽³⁾⁽⁴⁾	3.75 Gb/s	—	—	0.30	UI
DJ _{3.75}	Deterministic Jitter ⁽³⁾⁽⁴⁾		—	—	0.15	UI
TJ _{3.2}	Total Jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁵⁾	—	—	0.2	UI
DJ _{3.2}	Deterministic Jitter ⁽³⁾⁽⁴⁾		—	—	0.1	UI
TJ _{3.2L}	Total Jitter ⁽³⁾⁽⁴⁾	3.20 Gb/s ⁽⁶⁾	—	—	0.32	UI
DJ _{3.2L}	Deterministic Jitter ⁽³⁾⁽⁴⁾		—	—	0.16	UI
TJ _{2.5}	Total Jitter ⁽³⁾⁽⁴⁾	2.5 Gb/s ⁽⁷⁾	—	—	0.20	UI
DJ _{2.5}	Deterministic Jitter ⁽³⁾⁽⁴⁾		—	—	0.08	UI
TJ _{1.25}	Total Jitter ⁽³⁾⁽⁴⁾	1.25 Gb/s ⁽⁸⁾	—	—	0.15	UI
DJ _{1.25}	Deterministic Jitter ⁽³⁾⁽⁴⁾		—	—	0.06	UI
TJ ₅₀₀	Total Jitter ⁽³⁾⁽⁴⁾	500 Mb/s	—	—	0.1	UI
DJ ₅₀₀	Deterministic Jitter ⁽³⁾⁽⁴⁾		—	—	0.03	UI

Notes:

- Using same REFCLK input with TX phase alignment enabled for up to 12 consecutive transmitters (three fully populated GTX Quads).
- Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of $1e^{-12}$.
- CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
- CPLL frequency at 1.6 GHz and TXOUT_DIV = 1.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.

Table 65: CPRI Protocol Characteristics

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
	9830.4	–	Note 1	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2	0.95	–	UI
	6144.0	0.95	–	UI
	9830.4	Note 1	–	UI

Notes:

1. Tested per SFP+ specification, see Table 64.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:

<http://www.xilinx.com/technology/protocols/pciexpress.htm>

Table 66: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
F _{PIPECLK}	Pipe clock maximum frequency	250.00	250.00	250.00	250.00	MHz
F _{USERCLK}	User clock maximum frequency	500.00	500.00	250.00	250.00	MHz
F _{USERCLK2}	User clock 2 maximum frequency	250.00	250.00	250.00	250.00	MHz
F _{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	250.00	MHz

XADC Specifications

Table 67: XADC Specifications

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V _{CCADC} = 1.8V ± 5%, V _{REFP} = 1.25V, V _{REFN} = 0V, ADCCLK = 26 MHz, T _j = −40°C to 100°C, Typical values at T _j =+40°C						
ADC Accuracy ⁽¹⁾						
Resolution			12	–	–	Bits
Integral Nonlinearity ⁽²⁾	INL		–	–	±3	LSBs
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset Error		Offset calibration enabled	–	–	±6	LSBs
Gain Error		Gain calibration disabled	–	–	±0.5	%
Offset Matching		Offset calibration enabled	–	–	4	LSBs
Gain Matching		Gain calibration disabled	–	–	0.3	%
Sample Rate			0.1	–	1	MS/s
Signal to Noise Ratio ⁽²⁾	SNR	F _{SAMPLE} = 500KS/s, F _{IN} = 20KHz	60	–	–	dB
RMS Code Noise		External 1.25V reference	–	–	2	LSBs
		On-chip reference	–	3	–	LSBs
Total Harmonic Distortion ⁽²⁾	THD	F _{SAMPLE} = 500KS/s, F _{IN} = 20KHz	–	70	–	dB
ADC Accuracy at Extended Temperatures (-55°C to 125°C)						
Resolution			10	–	–	Bits
Integral Nonlinearity ⁽²⁾	INL		–	–	±1	LSB (at 10 bits)
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	
Analog Inputs ⁽³⁾						
ADC Input Ranges		Unipolar operation	0	–	1	V
		Bipolar operation	−0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum External Channel Input Ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	−0.1	–	V _{CCADC}	V
Auxiliary Channel Full Resolution Bandwidth	FRBW		250	–	–	KHz
On-Chip Sensors						
Temperature Sensor Error		T _j = −40°C to 100°C.	–	–	±4	°C
		T _j = −55°C to +125°C	–	–	±6	°C
Supply Sensor Error		Measurement range of V _{CCAUX} 1.8V ±5% T _j = −40°C to +100°C	–	–	±1	%
		Measurement range of V _{CCAUX} 1.8V ±5% T _j = −55°C to +125°C	–	–	±2	%
Conversion Rate ⁽⁴⁾						
Conversion Time - Continuous	t _{CONV}	Number of ADCCLK cycles	26	–	32	Cycles
Conversion Time - Event	t _{CONV}	Number of CLK cycles	–	–	21	Cycles
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	26	MHz
DCLK Duty Cycle			40	–	60	%

Date	Version	Description
07/25/12	1.6	Updated the descriptions, changed V_{IN} and Note 2 and added Note 4 in Table 1. In Table 2, changed descriptions and notes, removed Note 7, changed GTX transceiver parameters and values and added Note 9. Updated parameters in Table 3. Added Table 4 and Table 5. Changed the typical values for many of the devices in Table 7. Updated LVCMOS12 and the SSTLs in Table 9. Updated many of the specifications in Table 10 and Table 11. Updated speed specification to v1.06 (-3, -2, -2L(1.0V), -1) and v1.05 (-2L(0.9V)) with appropriate changes to Table 14 and Table 15 including production release of the XC7K325T and the XC7K410T in the -2, -2L(1.0V), and -1 speed designations. Added notes and specifications to Table 17 and Table 18. Updated the IOB Pad Input/Output/3-State discussion and changed Table 21 by adding $T_{IOIBUFDISABLE}$. Removed many of the combinatorial delay specifications and T_{CINCK}/T_{CKCIN} from Table 28. Rearranged Table 51 including moving some parameters to Table 1. Added Table 56. Updated Table 57. In Table 59, updated SJ Jitter Tolerance with Stressed Eye section, page 51 and Note 8. Added Note 1, Note 2, and Note 3 to Table 62. Added Note 1 and Note 2 to Table 63, and line rate ranges. Updated Table 64 including adding Note 1. Updated Table 65 including adding Note 1. In Table 67 updated Note 1 and added Note 4. In Table 68, updated T_{POR} and F_{EMCCK}.
09/04/12	1.7	Updated Table 14 and Table 15 for production release of the XC7K160T in the -2, -2L(1.0V), and -1 speed designations.
09/26/12	1.8	In Table 2 , revised V_{CCINT} and V_{CCBRAM} and added Note 2 . Updated Table 14 and Table 15 for production release of the XC7K480T in the -2, -2L(1.0V), and -1 speed designations and the XC7K325T and XC7K410T in the -3 speed designation.
10/10/12	1.9	Updated the $I_{CCINTMIN}$ value for the XC7K355T in Table 7 . Updated Table 14 and Table 15 for production release of the XC7K420T in the -2, -2L(1.0V), and -1 speed designations.
10/25/12	2.0	Updated the AC Switching Characteristics based upon ISE 14.3 v1.07 for the -3, -2, -2L (1.0V), -1 speed specifications, and ISE 14.3 v1.06 for the -2L (0.9V) speed specifications throughout the document. Updated Table 14 and Table 15 for production release of the XC7K355T in the -2, -2L(1.0V), and -1 speed designations. Also updated Table 14 and Table 15 for production release of the XC7K325T and XC7K410T in the -2L (0.9V). Added values for Table 16 -2L (0.9V). Added package skew values to Table 50. In Table 53, increased -1 speed grade (FF package) F_{GTMAX} value from 6.6 Gb/s to 8.0 Gb/s.
10/31/12	2.1	Updated Table 14 and Table 15 for production release of the XC7K70T in the -2, -2L(1.0V), and -1 speed designations.
11/26/12	2.2	Updated Table 14 and Table 15 for production release of -3 speed designation for XC7K70T, XC7K160T, XC7K355T, XC7K420T, and XC7K480T. Removed Note 4 from Table 67 .
12/05/12	2.3	Updated Table 14 and Table 15 for production release of the -2L (0.9V) speed designation for XC7K160T, XC7K420T, and XC7K480T. Updated Note 1 in Table 50 .
12/12/12	2.4	Updated Table 14 and Table 15 for production release of the -2L (0.9V) speed designation for XC7K70T and XC7K355T. Added Internal Configuration Access Port section to Table 68 .