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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 37325 |
| Number of Logic Elements/Cells | 477760 |
| Total RAM Bits | 35205120 |
| Number of I/O | 400 |
| Number of Gates | - |
| Voltage - Supply | 0.97V ~ 1.03V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1156-BBGA, FCBGA |
| Supplier Device Package | 1156-FCBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc7k480t-2ffv1156c |

*Table 1:* **Absolute Maximum Ratings (1) *(Cont'd)***

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $I_{DCIN}$ | DC input current for receiver input pins DC coupled $V_{MGTAVTT}$ = 1.2V | – | 14 | mA |
| $I_{DCOUT}$ | DC output current for transmitter pins DC coupled $V_{MGTAVTT}$ = 1.2V | – | 14 | mA |
| **XADC** | | | | |
| $V_{CCADC}$ | XADC supply relative to GNDADC | –0.5 | 2.0 | V |
| $V_{REFP}$ | XADC reference input relative to GNDADC | –0.5 | 2.0 | V |
| **Temperature** | | | | |
| $T_{STG}$ | Storage temperature (ambient) | –65 | 150 | °C |
| $T_{SOL}$ | Maximum soldering temperature for Pb/Sn component bodies (6) | – | +220 | °C |
| | Maximum soldering temperature for Pb-free component bodies (6) | – | +260 | °C |
| $T_j$ | Maximum junction temperature(6) | – | +125 | °C |

**Notes:**

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. The lower absolute voltage specification always applies.
3. For I/O operation, refer to UG471: *7 Series FPGAs SelectIO Resources User Guide*.
4. The maximum limit applied to DC and AC signals.
5. For maximum undershoot and overshoot AC specifications, see Table 4 and Table 5.
6. For soldering guidelines and thermal considerations, see UG475: *7 Series FPGA Packaging and Pinout Specification*.

*Table 2:* **Recommended Operating Conditions (1)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **FPGA Logic** | | | | | |
| $V_{CCINT}$(2) | Internal supply voltage | 0.97 | 1.00 | 1.03 | V |
| | For -2L (0.9V) devices: internal supply voltage | 0.87 | 0.90 | 0.93 | V |
| $V_{CCBRAM}$(2) | Block RAM supply voltage | 0.97 | 1.00 | 1.03 | V |
| | For -2L (0.9V) devices: block RAM supply voltage | 0.87 | 0.90 | 1.03 | V |
| $V_{CCAUX}$ | Auxiliary supply voltage | 1.71 | 1.80 | 1.89 | V |
| $V_{CCO}$(3)(4) | Supply voltage for 3.3V HR I/O banks | 1.14 | – | 3.465 | V |
| | Supply voltage for 1.8V HP I/O banks | 1.14 | – | 1.89 | V |
| $V_{CCAUX_IO}$ | Auxiliary supply voltage when set to 1.8V | 1.71 | 1.80 | 1.89 | V |
| | Auxiliary supply voltage when set to 2.0V | 1.94 | 2.00 | 2.06 | V |
| $V_{IN}$(5) | I/O input voltage | –0.20 | – | $V_{CCO}$ + 0.2 | V |
| | I/O input voltage for $V_{REF}$ and differential I/O standards | –0.20 | – | 2.625 | V |
| $I_{IN}$(6) | Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode. | – | – | 10 | mA |
| $V_{CCBATT}$(7) | Battery voltage | 1.0 | – | 1.89 | V |
| **GTX Transceiver** | | | | | |
| $V_{MGTAVCC}$(8) | Analog supply voltage for the GTX transceiver QPLL frequency range ≤ 10.3125 GHz(9)(10) | 0.97 | 1.0 | 1.08 | V |
| | Analog supply voltage for the GTX transceiver QPLL frequency range > 10.3125 GHz | 1.02 | 1.05 | 1.08 | V |
| $V_{MGTAVTT}$(8) | Analog supply voltage for the GTX transmitter and receiver termination circuits | 1.17 | 1.2 | 1.23 | V |
| $V_{MGTVCCAUX}$(8) | Auxiliary analog QPLL voltage supply for the transceivers | 1.75 | 1.80 | 1.85 | V |

*Table 2:* **Recommended Operating Conditions (1) *(Cont'd)***

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{MGTAVTTRCAL}$ (8) | Analog supply voltage for the resistor calibration circuit of the GTX transceiver column | 1.17 | 1.2 | 1.23 | V |
| **XADC** | | | | | |
| $V_{CCADC}$ | XADC supply relative to GNDADC | 1.71 | 1.80 | 1.89 | V |
| $V_{REFP}$ | Externally supplied reference voltage | 1.20 | 1.25 | 1.30 | V |
| **Temperature** | | | | | |
| $T_j$ | Junction temperature operating range for commercial (C) temperature devices | 0 | – | 85 | °C |
| | Junction temperature operating range for extended (E) temperature devices | 0 | – | 100 | °C |
| | Junction temperature operating range for industrial (I) temperature devices | –40 | – | 100 | °C |

**Notes:**

1. All voltages are relative to ground.
2. $V_{CCINT}$ and $V_{CCBRAM}$ should be connected to the same supply.
3. Configuration data is retained even if $V_{CCO}$ drops to 0V.
4. Includes $V_{CCO}$ of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
5. The lower absolute voltage specification always applies.
6. A total of 200 mA per bank should not be exceeded.
7. $V_{CCBATT}$ is required only when using bitstream encryption. If battery is not used, connect $V_{CCBATT}$ to either ground or $V_{CCAUX}$.
8. Each voltage listed requires the filter circuit described in UG476: *7 Series FPGAs GTX/GTH Transceiver User Guide*.
9. For data rates ≤ 10.3125 Gb/s, $V_{MGTAVCC}$ should be 1.0V ±3% for lower power consumption.
10. For lower power consumption, $V_{MGTAVCC}$ should be 1.0V ±3% over the entire CPLL frequency range.

*Table 3:* **DC Characteristics Over Recommended Operating Conditions**

| Symbol | Description | Min | Typ(1) | Max | Units |
|---|---|---|---|---|---|
| $V_{DRINT}$ | Data retention $V_{CCINT}$ voltage (below which configuration data might be lost) | 0.75 | – | – | V |
| $V_{DRI}$ | Data retention $V_{CCAUX}$ voltage (below which configuration data might be lost) | 1.5 | – | – | V |
| $I_{REF}$ | $V_{REF}$ leakage current per pin | – | – | 15 | µA |
| $I_L$ | Input or output leakage current per pin (sample-tested) | – | – | 15 | µA |
| $C_{IN}$ (2) | Die input capacitance at the pad | – | – | 8 | pF |
| $I_{RPU}$ | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 3.3V | 90 | – | 330 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 2.5V | 68 | – | 250 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.8V | 34 | – | 220 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.5V | 23 | – | 150 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.2V | 12 | – | 120 | µA |
| $I_{RPD}$ | Pad pull-down (when selected) @ $V_{IN}$ = 3.3V | 68 | – | 330 | µA |
| | Pad pull-down (when selected) @ $V_{IN}$ = 1.8V | 45 | – | 180 | µA |
| $I_{CCADC}$ | Analog supply current, analog circuits in powered up state | – | – | 25 | mA |
| $I_{BATT}$ (3) | Battery supply current | – | – | 150 | nA |

*Table 3:* **DC Characteristics Over Recommended Operating Conditions *(Cont'd)***

| Symbol | Description | Min | Typ[1] | Max | Units |
|---|---|---|---|---|---|
| $R_{IN_TERM}$[4] | Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_40) for commercial (C), industrial (I), and extended (E) temperature devices | 28 | 40 | 55 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_50) for commercial (C), industrial (I), and extended (E) temperature devices | 35 | 50 | 65 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_60) for commercial (C), industrial (I), and extended (E) temperature devices | 44 | 60 | 83 | Ω |
| n | Temperature diode ideality factor | – | 1.010 | – | – |
| r | Temperature diode series resistance | – | 2 | – | Ω |

**Notes:**

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a $V_{CCO}/2$ level.

*Table 4:* **Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks[1]**

| AC Voltage Overshoot | % of UI @–40°C to 100°C | AC Voltage Undershoot | % of UI @–40°C to 100°C |
|---|---|---|---|
| $V_{CCO}$ + 0.40 | 100 | –0.40 | 100 |
| $V_{CCO}$ + 0.45 | 100 | –0.45 | 61.7 |
| $V_{CCO}$ + 0.50 | 100 | –0.50 | 25.8 |
| $V_{CCO}$ + 0.55 | 100 | –0.55 | 11.0 |
| $V_{CCO}$ + 0.60 | 46.6 | –0.60 | 4.77 |
| $V_{CCO}$ + 0.65 | 21.2 | –0.65 | 2.10 |
| $V_{CCO}$ + 0.70 | 9.75 | –0.70 | 0.94 |
| $V_{CCO}$ + 0.75 | 4.55 | –0.75 | 0.43 |
| $V_{CCO}$ + 0.80 | 2.15 | –0.80 | 0.20 |
| $V_{CCO}$ + 0.85 | 1.02 | –0.85 | 0.09 |
| $V_{CCO}$ + 0.90 | 0.49 | –0.90 | 0.04 |
| $V_{CCO}$ + 0.95 | 0.24 | –0.95 | 0.02 |

**Notes:**

1. A total of 200 mA per bank should not be exceeded.

*Table 5:* **Maximum Allowed AC Voltage Overshoot and Undershoot for 1.8V HP I/O Banks[1][2]**

| AC Voltage Overshoot | % of UI @–40°C to 100°C | AC Voltage Undershoot | % of UI @–40°C to 100°C |
|---|---|---|---|
| $V_{CCO}$ + 0.40 | 100 | –0.40 | 100 |
| $V_{CCO}$ + 0.45 | 100 | –0.45 | 100 |
| $V_{CCO}$ + 0.50 | 100 | –0.50 | 100 |
| $V_{CCO}$ + 0.55 | 100 | –0.55 | 100 |
| $V_{CCO}$ + 0.60 | 50.0 | –0.60 | 50.0 |
| $V_{CCO}$ + 0.65 | 50.0 | –0.65 | 50.0 |
| $V_{CCO}$ + 0.70 | 47.0 | –0.70 | 50.0 |
| $V_{CCO}$ + 0.75 | 21.2 | –0.75 | 50.0 |

*Table 5:* **Maximum Allowed AC Voltage Overshoot and Undershoot for 1.8V HP I/O Banks(1)(2) *(Cont'd)***

| AC Voltage Overshoot | % of UI @–40°C to 100°C | AC Voltage Undershoot | % of UI @–40°C to 100°C |
|---|---|---|---|
| $V_{CCO}$ + 0.80 | 9.71 | –0.80 | 50.0 |
| $V_{CCO}$ + 0.85 | 4.51 | –0.85 | 28.4 |
| $V_{CCO}$ + 0.90 | 2.12 | –0.90 | 12.7 |
| $V_{CCO}$ + 0.95 | 1.01 | –0.95 | 5.79 |

**Notes:**

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.

*Table 6:* **Typical Quiescent Supply Current**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| $I_{CCINTQ}$ | Quiescent $V_{CCINT}$ supply current | XC7K70T | 241 | 241 | 241 | 187 | mA |
| | | XC7K160T | 474 | 474 | 474 | 368 | mA |
| | | XC7K325T | 810 | 810 | 810 | 629 | mA |
| | | XC7K355T | 993 | 993 | 993 | 771 | mA |
| | | XC7K410T | 1080 | 1080 | 1080 | 838 | mA |
| | | XC7K420T | 1313 | 1313 | 1313 | 1019 | mA |
| | | XC7K480T | 1313 | 1313 | 1313 | 1019 | mA |
| $I_{CCOQ}$ | Quiescent $V_{CCO}$ supply current | XC7K70T | 1 | 1 | 1 | 1 | mA |
| | | XC7K160T | 1 | 1 | 1 | 1 | mA |
| | | XC7K325T | 1 | 1 | 1 | 1 | mA |
| | | XC7K355T | 1 | 1 | 1 | 1 | mA |
| | | XC7K410T | 1 | 1 | 1 | 1 | mA |
| | | XC7K420T | 1 | 1 | 1 | 1 | mA |
| | | XC7K480T | 1 | 1 | 1 | 1 | mA |
| $I_{CCAUXQ}$ | Quiescent $V_{CCAUX}$ supply current | XC7K70T | 21 | 21 | 21 | 21 | mA |
| | | XC7K160T | 40 | 40 | 40 | 40 | mA |
| | | XC7K325T | 68 | 68 | 68 | 68 | mA |
| | | XC7K355T | 75 | 75 | 75 | 75 | mA |
| | | XC7K410T | 85 | 85 | 85 | 85 | mA |
| | | XC7K420T | 99 | 99 | 99 | 99 | mA |
| | | XC7K480T | 99 | 99 | 99 | 99 | mA |
| $I_{CCAUX_IOQ}$ | Quiescent $V_{CCAUX_IO}$ supply current | XC7K70T | N/A | N/A | N/A | N/A | mA |
| | | XC7K160T | 2 | 2 | 2 | 2 | mA |
| | | XC7K325T | 2 | 2 | 2 | 2 | mA |
| | | XC7K355T | N/A | N/A | N/A | N/A | mA |
| | | XC7K410T | 2 | 2 | 2 | 2 | mA |
| | | XC7K420T | N/A | N/A | N/A | N/A | mA |
| | | XC7K480T | N/A | N/A | N/A | N/A | mA |

# AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in ISE® software 14.3 v1.07 for the -3, -2, -2L(1.0V), -1, and v1.06 for -2L(0.9V) speed grades.

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

***Advance Product Specification***

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

***Preliminary Product Specification***

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

***Product Specification***

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

## Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Kintex-7 FPGAs.

## Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 14 correlates the current status of each Kintex-7 device on a per speed grade basis.

*Table 14:* **Kintex-7 Device Speed Grade Designations**

| Device | Speed Grade Designations | | |
|---|---|---|---|
| | Advance | Preliminary | Production |
| XC7K70T | | | -3, -2, -2L(1.0V), -1, and -2L (0.9V) |
| XC7K160T | | | -3, -2, -2L(1.0V), -1, and -2L (0.9V) |
| XC7K325T | | | -3, -2, -2L(1.0V), -1, and -2L (0.9V) |
| XC7K355T | | | -3, -2, -2L(1.0V), -1, and -2L (0.9V) |
| XC7K410T | | | -3, -2, -2L(1.0V), -1, and -2L (0.9V) |
| XC7K420T | | | -3, -2, -2L(1.0V), -1, and -2L (0.9V) |
| XC7K480T | | | -3, -2, -2L(1.0V), -1, and -2L (0.9V) |

*Table 19:* **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | 1.0V | | | 0.9V | 1.0V | | | 0.9V | 1.0V | | | 0.9V | |
| | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | |
| HSTL_I_F | 0.61 | 0.64 | 0.73 | 0.79 | 1.10 | 1.19 | 1.23 | 1.41 | 1.86 | 2.05 | 2.22 | 1.92 | ns |
| HSTL_II_F | 0.61 | 0.64 | 0.73 | 0.78 | 1.05 | 1.18 | 1.28 | 1.42 | 1.81 | 2.04 | 2.27 | 1.94 | ns |
| HSTL_I_18_F | 0.64 | 0.67 | 0.76 | 0.79 | 1.05 | 1.18 | 1.28 | 1.44 | 1.81 | 2.04 | 2.27 | 1.95 | ns |
| HSTL_II_18_F | 0.64 | 0.67 | 0.76 | 0.79 | 1.03 | 1.14 | 1.23 | 1.42 | 1.79 | 2.00 | 2.22 | 1.94 | ns |
| DIFF_HSTL_I_F | 0.63 | 0.67 | 0.77 | 0.78 | 1.09 | 1.18 | 1.22 | 1.48 | 1.85 | 2.04 | 2.21 | 2.00 | ns |
| DIFF_HSTL_II_F | 0.63 | 0.67 | 0.77 | 0.79 | 1.02 | 1.11 | 1.14 | 1.48 | 1.78 | 1.97 | 2.13 | 2.00 | ns |
| DIFF_HSTL_I_18_F | 0.65 | 0.69 | 0.78 | 0.79 | 1.08 | 1.17 | 1.21 | 1.48 | 1.84 | 2.03 | 2.20 | 2.00 | ns |
| DIFF_HSTL_II_18_F | 0.65 | 0.69 | 0.78 | 0.81 | 1.01 | 1.10 | 1.13 | 1.48 | 1.77 | 1.96 | 2.12 | 2.00 | ns |
| LVCMOS33_S4 | 1.31 | 1.40 | 1.60 | 1.54 | 5.23 | 5.61 | 6.09 | 4.13 | 5.99 | 6.47 | 7.08 | 4.64 | ns |
| LVCMOS33_S8 | 1.31 | 1.40 | 1.60 | 1.54 | 4.46 | 4.85 | 5.33 | 3.84 | 5.22 | 5.71 | 6.32 | 4.36 | ns |
| LVCMOS33_S12 | 1.31 | 1.40 | 1.60 | 1.54 | 3.46 | 3.89 | 4.42 | 3.41 | 4.22 | 4.75 | 5.41 | 3.92 | ns |
| LVCMOS33_S16 | 1.31 | 1.40 | 1.60 | 1.54 | 3.06 | 3.43 | 3.88 | 3.72 | 3.82 | 4.29 | 4.87 | 4.23 | ns |
| LVCMOS33_F4 | 1.31 | 1.40 | 1.60 | 1.54 | 4.70 | 5.01 | 5.36 | 3.58 | 5.46 | 5.87 | 6.35 | 4.09 | ns |
| LVCMOS33_F8 | 1.31 | 1.40 | 1.60 | 1.54 | 3.62 | 4.04 | 4.56 | 3.06 | 4.38 | 4.90 | 5.55 | 3.58 | ns |
| LVCMOS33_F12 | 1.31 | 1.40 | 1.60 | 1.54 | 2.57 | 2.85 | 3.15 | 2.88 | 3.33 | 3.71 | 4.14 | 3.39 | ns |
| LVCMOS33_F16 | 1.31 | 1.40 | 1.60 | 1.54 | 2.44 | 2.69 | 2.96 | 2.88 | 3.20 | 3.55 | 3.95 | 3.39 | ns |
| LVCMOS25_S4 | 1.08 | 1.16 | 1.32 | 1.36 | 4.49 | 4.80 | 5.16 | 3.44 | 5.25 | 5.66 | 6.15 | 3.95 | ns |
| LVCMOS25_S8 | 1.08 | 1.16 | 1.32 | 1.36 | 3.66 | 4.04 | 4.49 | 3.20 | 4.42 | 4.90 | 5.48 | 3.72 | ns |
| LVCMOS25_S12 | 1.08 | 1.16 | 1.32 | 1.36 | 2.77 | 3.10 | 3.49 | 2.80 | 3.53 | 3.96 | 4.48 | 3.31 | ns |
| LVCMOS25_S16 | 1.08 | 1.16 | 1.32 | 1.36 | 3.24 | 3.62 | 4.09 | 3.14 | 4.00 | 4.48 | 5.08 | 3.66 | ns |
| LVCMOS25_F4 | 1.08 | 1.16 | 1.32 | 1.36 | 3.96 | 4.31 | 4.72 | 3.06 | 4.72 | 5.17 | 5.71 | 3.58 | ns |
| LVCMOS25_F8 | 1.08 | 1.16 | 1.32 | 1.36 | 2.43 | 2.87 | 3.42 | 2.50 | 3.19 | 3.73 | 4.41 | 3.02 | ns |
| LVCMOS25_F12 | 1.08 | 1.16 | 1.32 | 1.36 | 2.23 | 2.63 | 3.13 | 2.48 | 2.99 | 3.49 | 4.12 | 3.00 | ns |
| LVCMOS25_F16 | 1.08 | 1.16 | 1.32 | 1.36 | 1.92 | 2.17 | 2.45 | 2.33 | 2.68 | 3.03 | 3.44 | 2.84 | ns |
| LVCMOS18_S4 | 0.64 | 0.66 | 0.74 | 0.87 | 3.24 | 3.45 | 3.66 | 1.91 | 4.00 | 4.31 | 4.65 | 2.42 | ns |
| LVCMOS18_S8 | 0.64 | 0.66 | 0.74 | 0.87 | 2.58 | 2.91 | 3.31 | 2.50 | 3.34 | 3.77 | 4.30 | 3.02 | ns |
| LVCMOS18_S12 | 0.64 | 0.66 | 0.74 | 0.87 | 2.58 | 2.91 | 3.31 | 2.50 | 3.34 | 3.77 | 4.30 | 3.02 | ns |
| LVCMOS18_S16 | 0.64 | 0.66 | 0.74 | 0.87 | 1.82 | 2.03 | 2.24 | 1.84 | 2.58 | 2.89 | 3.23 | 2.36 | ns |
| LVCMOS18_S24(1) | 0.64 | 0.66 | 0.74 | 0.87 | 1.74 | 1.92 | 2.08 | 1.92 | 2.50 | 2.78 | 3.07 | 2.44 | ns |
| LVCMOS18_F4 | 0.64 | 0.66 | 0.74 | 0.87 | 3.12 | 3.31 | 3.49 | 1.77 | 3.88 | 4.17 | 4.48 | 2.28 | ns |
| LVCMOS18_F8 | 0.64 | 0.66 | 0.74 | 0.87 | 1.91 | 2.13 | 2.36 | 2.00 | 2.67 | 2.99 | 3.35 | 2.52 | ns |
| LVCMOS18_F12 | 0.64 | 0.66 | 0.74 | 0.87 | 1.91 | 2.13 | 2.36 | 2.00 | 2.67 | 2.99 | 3.35 | 2.52 | ns |
| LVCMOS18_F16 | 0.64 | 0.66 | 0.74 | 0.87 | 1.52 | 1.68 | 1.81 | 1.72 | 2.28 | 2.54 | 2.80 | 2.23 | ns |
| LVCMOS18_F24(1) | 0.64 | 0.66 | 0.74 | 0.87 | 1.34 | 1.46 | 1.55 | 1.66 | 2.10 | 2.32 | 2.54 | 2.17 | ns |
| LVCMOS15_S4 | 0.66 | 0.69 | 0.81 | 0.90 | 3.48 | 3.74 | 4.03 | 2.22 | 4.24 | 4.60 | 5.02 | 2.73 | ns |
| LVCMOS15_S8 | 0.66 | 0.69 | 0.81 | 0.90 | 2.37 | 2.67 | 3.01 | 2.41 | 3.13 | 3.53 | 4.00 | 2.92 | ns |
| LVCMOS15_S12 | 0.66 | 0.69 | 0.81 | 0.90 | 1.83 | 2.03 | 2.23 | 1.91 | 2.59 | 2.89 | 3.22 | 2.42 | ns |

*Table 20:* **1.8V IOB High Performance (HP) Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | 1.0V | | | 0.9V | 1.0V | | | 0.9V | 1.0V | | | 0.9V | |
| | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | |
| SSTL18_I_F | 0.68 | 0.72 | 0.82 | 0.86 | 0.94 | 1.06 | 1.15 | 1.32 | 1.58 | 1.82 | 1.97 | 1.93 | ns |
| SSTL18_II_F | 0.68 | 0.72 | 0.82 | 0.87 | 0.97 | 1.09 | 1.16 | 1.36 | 1.61 | 1.84 | 1.99 | 1.98 | ns |
| SSTL18_I_DCI_F | 0.68 | 0.72 | 0.82 | 0.76 | 0.89 | 1.02 | 1.10 | 1.30 | 1.53 | 1.77 | 1.92 | 1.91 | ns |
| SSTL18_II_DCI_F | 0.68 | 0.72 | 0.82 | 0.78 | 0.89 | 1.02 | 1.10 | 1.24 | 1.53 | 1.77 | 1.92 | 1.85 | ns |
| SSTL18_II_T_DCI_F | 0.68 | 0.72 | 0.82 | 0.78 | 0.89 | 1.02 | 1.10 | 1.27 | 1.53 | 1.77 | 1.92 | 1.88 | ns |
| SSTL15_F | 0.68 | 0.72 | 0.82 | 0.81 | 0.89 | 1.01 | 1.09 | 1.24 | 1.53 | 1.77 | 1.91 | 1.85 | ns |
| SSTL15_DCI_F | 0.68 | 0.72 | 0.82 | 0.78 | 0.89 | 1.01 | 1.09 | 1.27 | 1.53 | 1.77 | 1.91 | 1.88 | ns |
| SSTL15_T_DCI_F | 0.68 | 0.72 | 0.82 | 0.80 | 0.89 | 1.01 | 1.09 | 1.27 | 1.53 | 1.77 | 1.91 | 1.88 | ns |
| SSTL135_F | 0.69 | 0.72 | 0.82 | 0.89 | 0.88 | 1.00 | 1.08 | 1.27 | 1.52 | 1.76 | 1.90 | 1.88 | ns |
| SSTL135_DCI_F | 0.69 | 0.72 | 0.82 | 0.84 | 0.89 | 1.00 | 1.08 | 1.27 | 1.52 | 1.76 | 1.90 | 1.88 | ns |
| SSTL135_T_DCI_F | 0.69 | 0.72 | 0.82 | 0.84 | 0.89 | 1.00 | 1.08 | 1.27 | 1.52 | 1.76 | 1.90 | 1.88 | ns |
| SSTL12_F | 0.69 | 0.72 | 0.82 | 0.95 | 0.88 | 1.00 | 1.08 | 1.26 | 1.52 | 1.76 | 1.90 | 1.87 | ns |
| SSTL12_DCI_F | 0.69 | 0.72 | 0.82 | 0.91 | 0.91 | 1.03 | 1.11 | 1.24 | 1.54 | 1.79 | 1.93 | 1.85 | ns |
| SSTL12_T_DCI_F | 0.69 | 0.72 | 0.82 | 0.91 | 0.91 | 1.03 | 1.11 | 1.26 | 1.54 | 1.79 | 1.93 | 1.87 | ns |
| DIFF_SSTL18_I_F | 0.75 | 0.79 | 0.92 | 0.89 | 0.94 | 1.06 | 1.15 | 1.38 | 1.58 | 1.82 | 1.97 | 1.99 | ns |
| DIFF_SSTL18_II_F | 0.75 | 0.79 | 0.92 | 0.89 | 0.97 | 1.09 | 1.16 | 1.40 | 1.61 | 1.84 | 1.99 | 2.01 | ns |
| DIFF_SSTL18_I_DCI_F | 0.75 | 0.79 | 0.92 | 0.76 | 0.89 | 1.02 | 1.10 | 1.36 | 1.53 | 1.77 | 1.92 | 1.98 | ns |
| DIFF_SSTL18_II_DCI_F | 0.75 | 0.79 | 0.92 | 0.75 | 0.89 | 1.02 | 1.10 | 1.32 | 1.53 | 1.77 | 1.92 | 1.93 | ns |
| DIFF_SSTL18_II_T_DCI_F | 0.75 | 0.79 | 0.92 | 0.76 | 0.89 | 1.02 | 1.10 | 1.38 | 1.53 | 1.77 | 1.92 | 1.99 | ns |
| DIFF_SSTL15_F | 0.68 | 0.72 | 0.82 | 0.89 | 0.89 | 1.01 | 1.09 | 1.24 | 1.53 | 1.77 | 1.91 | 1.85 | ns |
| DIFF_SSTL15_DCI_F | 0.68 | 0.72 | 0.82 | 0.75 | 0.89 | 1.01 | 1.09 | 1.27 | 1.53 | 1.77 | 1.91 | 1.88 | ns |
| DIFF_SSTL15_T_DCI_F | 0.68 | 0.72 | 0.82 | 0.76 | 0.89 | 1.01 | 1.09 | 1.35 | 1.53 | 1.77 | 1.91 | 1.96 | ns |
| DIFF_SSTL135_F | 0.69 | 0.72 | 0.82 | 0.91 | 0.88 | 1.00 | 1.08 | 1.27 | 1.52 | 1.76 | 1.90 | 1.88 | ns |
| DIFF_SSTL135_DCI_F | 0.69 | 0.72 | 0.82 | 0.76 | 0.89 | 1.00 | 1.08 | 1.27 | 1.52 | 1.76 | 1.90 | 1.88 | ns |
| DIFF_SSTL135_T_DCI_F | 0.69 | 0.72 | 0.82 | 0.76 | 0.89 | 1.00 | 1.08 | 1.35 | 1.52 | 1.76 | 1.90 | 1.96 | ns |
| DIFF_SSTL12_F | 0.69 | 0.72 | 0.82 | 0.91 | 0.88 | 1.00 | 1.08 | 1.26 | 1.52 | 1.76 | 1.90 | 1.87 | ns |
| DIFF_SSTL12_DCI_F | 0.69 | 0.72 | 0.82 | 0.78 | 0.91 | 1.03 | 1.11 | 1.24 | 1.54 | 1.79 | 1.93 | 1.85 | ns |
| DIFF_SSTL12_T_DCI_F | 0.69 | 0.72 | 0.82 | 0.80 | 0.91 | 1.03 | 1.11 | 1.33 | 1.54 | 1.79 | 1.93 | 1.94 | ns |

**Notes:**

1. This I/O standard is only available in the 1.8V high-performance (HP) banks.

Table 21 specifies the values of $T_{IOTPHZ}$ and $T_{IOIBUFDISABLE}$. $T_{IOTPHZ}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than $T_{IOTPHZ}$ when the DCITERMDISABLE pin is used. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than $T_{IOTPHZ}$ when the INTERMDISABLE pin is used.

*Table 21:* **IOB 3-state Output Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $T_{IOTPHZ}$ | T input to pad high-impedance | 0.76 | 0.86 | 0.99 | 0.62 | ns |
| $T_{IOIBUFDISABLE_HR}$ | IBUF turn-on time from IBUFDISABLE to O output for HR I/O banks | 1.72 | 1.89 | 2.14 | 2.17 | ns |
| $T_{IOIBUFDISABLE_HP}$ | IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks | 1.31 | 1.46 | 1.76 | 1.86 | ns |

## Input Serializer/Deserializer Switching Characteristics

*Table 24:* **ISERDES Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Setup/Hold for Control Lines** | | | | | | |
| $T_{ISCCK_BITSLIP}$/ $T_{ISCKC_BITSLIP}$ | BITSLIP pin Setup/Hold with respect to CLKDIV | 0.01/0.12 | 0.02/0.13 | 0.02/0.15 | 0.02/0.21 | ns |
| $T_{ISCCK_CE}$/ $T_{ISCKC_CE}$(2) | CE pin Setup/Hold with respect to CLK (for CE1) | 0.39/–0.02 | 0.44/–0.02 | 0.63/–0.02 | 0.51/–0.22 | ns |
| $T_{ISCCK_CE2}$/ $T_{ISCKC_CE2}$(2) | CE pin Setup/Hold with respect to CLKDIV (for CE2) | –0.12/0.29 | –0.12/0.31 | –0.12/0.35 | –0.17/0.40 | ns |
| **Setup/Hold for Data Lines** | | | | | | |
| $T_{ISDCK_D}$/$T_{ISCKD_D}$ | D pin Setup/Hold with respect to CLK | –0.02/0.11 | –0.02/0.12 | –0.02/0.15 | –0.04/0.19 | ns |
| $T_{ISDCK_DDLY}$/ $T_{ISCKD_DDLY}$ | DDLY pin Setup/Hold with respect to CLK (using IDELAY)(1) | –0.02/0.11 | –0.02/0.12 | –0.02/0.15 | –0.03/0.19 | ns |
| $T_{ISDCK_D_DDR}$/ $T_{ISCKD_D_DDR}$ | D pin Setup/Hold with respect to CLK at DDR mode | –0.02/0.11 | –0.02/0.12 | –0.02/0.15 | –0.04/0.19 | ns |
| $T_{ISDCK_DDLY_DDR}$/ $T_{ISCKD_DDLY_DDR}$ | D pin Setup/Hold with respect to CLK at DDR mode (using IDELAY)(1) | 0.11/0.11 | 0.12/0.12 | 0.15/0.15 | 0.19/0.19 | ns |
| **Sequential Delays** | | | | | | |
| $T_{ISCKO_Q}$ | CLKDIV to out at Q pin | 0.46 | 0.47 | 0.58 | 0.67 | ns |
| **Propagation Delays** | | | | | | |
| $T_{ISDO_DO}$ | D input to DO output pin | 0.09 | 0.10 | 0.12 | 0.14 | ns |

**Notes:**

1. Recorded at 0 tap value.
2. $T_{ISCCK_CE2}$ and $T_{ISCKC_CE2}$ are reported as $T_{ISCCK_CE}$/$T_{ISCKC_CE}$ in TRACE report.

## MMCM Switching Characteristics

*Table 38:* **MMCM Specification**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | | 1.0V | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $MMCM_F_{INMAX}$ | Maximum Input Clock Frequency | 1066.00 | 933.00 | 800.00 | 800.00 | MHz |
| $MMCM_F_{INMIN}$ | Minimum Input Clock Frequency | 10.00 | 10.00 | 10.00 | 10.00 | MHz |
| $MMCM_F_{INJITTER}$ | Maximum Input Clock Period Jitter | < 20% of clock input period or 1 ns Max | | | | |
| $MMCM_F_{INDUTY}$ | Allowable Input Duty Cycle: 10—49 MHz | 25.00 | 25.00 | 25.00 | 25.00 | % |
| | Allowable Input Duty Cycle: 50—199 MHz | 30.00 | 30.00 | 30.00 | 30.00 | % |
| | Allowable Input Duty Cycle: 200—399 MHz | 35.00 | 35.00 | 35.00 | 35.00 | % |
| | Allowable Input Duty Cycle: 400—499 MHz | 40.00 | 40.00 | 40.00 | 40.00 | % |
| | Allowable Input Duty Cycle: >500 MHz | 45.00 | 45.00 | 45.00 | 45.00 | % |
| $MMCM_F_{MIN_PSCLK}$ | Minimum Dynamic Phase Shift Clock Frequency | 0.01 | 0.01 | 0.01 | 0.01 | MHz |
| $MMCM_F_{MAX_PSCLK}$ | Maximum Dynamic Phase Shift Clock Frequency | 550.00 | 500.00 | 450.00 | 450.00 | MHz |
| $MMCM_F_{VCOMIN}$ | Minimum MMCM VCO Frequency | 600.00 | 600.00 | 600.00 | 600.00 | MHz |
| $MMCM_F_{VCOMAX}$ | Maximum MMCM VCO Frequency | 1600.00 | 1440.00 | 1200.00 | 1200.00 | MHz |
| $MMCM_F_{BANDWIDTH}$ | Low MMCM Bandwidth at Typical(1) | 1.00 | 1.00 | 1.00 | 1.00 | MHz |
| | High MMCM Bandwidth at Typical(1) | 4.00 | 4.00 | 4.00 | 4.00 | MHz |
| $MMCM_T_{STATPHAOFFSET}$ | Static Phase Offset of the MMCM Outputs(2) | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| $MMCM_T_{OUTJITTER}$ | MMCM Output Jitter | Note 3 | | | | |
| $MMCM_T_{OUTDUTY}$ | MMCM Output Clock Duty Cycle Precision(4) | 0.20 | 0.20 | 0.20 | 0.25 | ns |
| $MMCM_T_{LOCKMAX}$ | MMCM Maximum Lock Time | 100.00 | 100.00 | 100.00 | 100.00 | µs |
| $MMCM_F_{OUTMAX}$ | MMCM Maximum Output Frequency | 1066.00 | 933.00 | 800.00 | 800.00 | MHz |
| $MMCM_F_{OUTMIN}$ | MMCM Minimum Output Frequency(5)(6) | 4.69 | 4.69 | 4.69 | 4.69 | MHz |
| $MMCM_T_{EXTFDVAR}$ | External Clock Feedback Variation | < 20% of clock input period or 1 ns Max | | | | |
| $MMCM_RST_{MINPULSE}$ | Minimum Reset Pulse Width | 5.00 | 5.00 | 5.00 | 5.00 | ns |
| $MMCM_F_{PFDMAX}$ | Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized | 550.00 | 500.00 | 450.00 | 450.00 | MHz |
| | Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low | 300.00 | 300.00 | 300.00 | 300.00 | MHz |
| $MMCM_F_{PFDMIN}$ | Minimum Frequency at the Phase Frequency Detector | 10.00 | 10.00 | 10.00 | 10.00 | MHz |
| $MMCM_T_{FBDELAY}$ | / | | | | | |

# GTX Transceiver Specifications