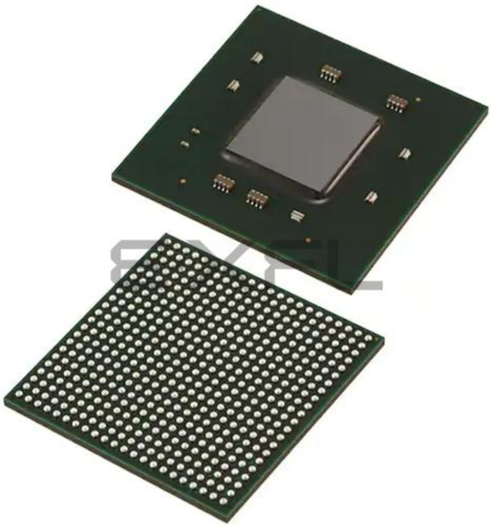
AMD Xilinx - XC7K70T-2FBG484I Datasheet



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Details	
Product Status	Active
Number of LABs/CLBs	5125
Number of Logic Elements/Cells	65600
Total RAM Bits	4976640
Number of I/O	285
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA, FCBGA
Supplier Device Package	484-FCBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7k70t-2fbg484i

Table 2: Recommended Operating Conditions [(1)] *(Cont'd)*

Symbol	Description	Min	Typ	Max	Units
$V_{MGTAVTTRCAL}$(8)	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	1.17	1.2	1.23	V
XADC					
V_{CCADC}	XADC supply relative to GNDADC	1.71	1.80	1.89	V
V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
Temperature					
T_j	Junction temperature operating range for commercial (C) temperature devices	0	–	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	–	100	°C

Notes:

1. All voltages are relative to ground.
2. V_{CCINT} and V_{CCBRAM} should be connected to the same supply.
3. Configuration data is retained even if V_{CCO} drops to 0V.
4. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
5. The lower absolute voltage specification always applies.
6. A total of 200 mA per bank should not be exceeded.
7. V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX}.
8. Each voltage listed requires the filter circuit described in UG476: *7 Series FPGAs GTX/GTH Transceiver User Guide*.
9. For data rates ≤ 10.3125 Gb/s, $V_{MGTAVCC}$ should be 1.0V ±3% for lower power consumption.
10. For lower power consumption, $V_{MGTAVCC}$ should be 1.0V ±3% over the entire CPLL frequency range.

Table 3: DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Min	Typ(1)	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	1.5	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	15	µA
I_L	Input or output leakage current per pin (sample-tested)	–	–	15	µA
C_{IN}(2)	Die input capacitance at the pad	–	–	8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V	90	–	330	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V	68	–	250	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V	34	–	220	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V	23	–	150	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V	12	–	120	µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.3V	68	–	330	µA
	Pad pull-down (when selected) @ V_{IN} = 1.8V	45	–	180	µA
I_{CCADC}	Analog supply current, analog circuits in powered up state	–	–	25	mA
I_{BATT}(3)	Battery supply current	–	–	150	nA

Table 3: **DC Characteristics Over Recommended Operating Conditions *(Cont'd)***

Symbol	Description	Min	Typ[(1)]	Max	Units
R_{IN_TERM}(4)	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_40) for commercial (C), industrial (I), and extended (E) temperature devices	28	40	55	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_50) for commercial (C), industrial (I), and extended (E) temperature devices	35	50	65	Ω
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_60) for commercial (C), industrial (I), and extended (E) temperature devices	44	60	83	Ω
n	Temperature diode ideality factor	–	1.010	–	–
r	Temperature diode series resistance	–	2	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a $V_{CCO}/2$ level.

Table 4: **Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks(1)**

AC Voltage Overshoot	% of UI @–40°C to 100°C	AC Voltage Undershoot	% of UI @–40°C to 100°C
V_{CCO} + 0.40	100	–0.40	100
V_{CCO} + 0.45	100	–0.45	61.7
V_{CCO} + 0.50	100	–0.50	25.8
V_{CCO} + 0.55	100	–0.55	11.0
V_{CCO} + 0.60	46.6	–0.60	4.77
V_{CCO} + 0.65	21.2	–0.65	2.10
V_{CCO} + 0.70	9.75	–0.70	0.94
V_{CCO} + 0.75	4.55	–0.75	0.43
V_{CCO} + 0.80	2.15	–0.80	0.20
V_{CCO} + 0.85	1.02	–0.85	0.09
V_{CCO} + 0.90	0.49	–0.90	0.04
V_{CCO} + 0.95	0.24	–0.95	0.02

Notes:

1. A total of 200 mA per bank should not be exceeded.

Table 5: **Maximum Allowed AC Voltage Overshoot and Undershoot for 1.8V HP I/O Banks(1)(2)**

AC Voltage Overshoot	% of UI @–40°C to 100°C	AC Voltage Undershoot	% of UI @–40°C to 100°C
V_{CCO} + 0.40	100	–0.40	100
V_{CCO} + 0.45	100	–0.45	100
V_{CCO} + 0.50	100	–0.50	100
V_{CCO} + 0.55	100	–0.55	100
V_{CCO} + 0.60	50.0	–0.60	50.0
V_{CCO} + 0.65	50.0	–0.65	50.0
V_{CCO} + 0.70	47.0	–0.70	50.0
V_{CCO} + 0.75	21.2	–0.75	50.0

Table 5: **Maximum Allowed AC Voltage Overshoot and Undershoot for 1.8V HP I/O Banks[(1)][(2)] *(Cont'd)***

AC Voltage Overshoot	% of UI @–40°C to 100°C	AC Voltage Undershoot	% of UI @–40°C to 100°C
V_{CCO} + 0.80	9.71	–0.80	50.0
V_{CCO} + 0.85	4.51	–0.85	28.4
V_{CCO} + 0.90	2.12	–0.90	12.7
V_{CCO} + 0.95	1.01	–0.95	5.79

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.

Table 6: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC7K70T	241	241	241	187	mA
		XC7K160T	474	474	474	368	mA
		XC7K325T	810	810	810	629	mA
		XC7K355T	993	993	993	771	mA
		XC7K410T	1080	1080	1080	838	mA
		XC7K420T	1313	1313	1313	1019	mA
		XC7K480T	1313	1313	1313	1019	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC7K70T	1	1	1	1	mA
		XC7K160T	1	1	1	1	mA
		XC7K325T	1	1	1	1	mA
		XC7K355T	1	1	1	1	mA
		XC7K410T	1	1	1	1	mA
		XC7K420T	1	1	1	1	mA
		XC7K480T	1	1	1	1	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC7K70T	21	21	21	21	mA
		XC7K160T	40	40	40	40	mA
		XC7K325T	68	68	68	68	mA
		XC7K355T	75	75	75	75	mA
		XC7K410T	85	85	85	85	mA
		XC7K420T	99	99	99	99	mA
		XC7K480T	99	99	99	99	mA
I_{CCAUX_IOQ}	Quiescent V_{CCAUX_IO} supply current	XC7K70T	N/A	N/A	N/A	N/A	mA
		XC7K160T	2	2	2	2	mA
		XC7K325T	2	2	2	2	mA
		XC7K355T	N/A	N/A	N/A	N/A	mA
		XC7K410T	2	2	2	2	mA
		XC7K420T	N/A	N/A	N/A	N/A	mA
		XC7K480T	N/A	N/A	N/A	N/A	mA

Table 7 shows the minimum current, in addition to I_{CCQ}, that are required by Kintex-7 devices for proper power-on and configuration. If the current minimums shown in Table 6 and Table 7 are met, the device powers on after all five supplies have passed through their power-on reset threshold voltages. The FPGA must not be configured until after V_{CCINT} is applied.

Once initialized and configured, use the XPower tools to estimate current drain on these supplies.

Table 7: **Power-On Current for Kintex-7 Devices**

Device	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	I_{CCAUX_IOMIN}	$I_{CCBRAMMIN}$	Units
	Typ[(1)]	Typ[(1)]	Typ[(1)]	Typ[(1)]	Typ[(1)]	
XC7K70T	I_{CCINTQ} + 450	I_{CCAUXQ} + 40	I_{CCOQ} + 40 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 40	mA
XC7K160T	I_{CCINTQ} + 550	I_{CCAUXQ} + 50	I_{CCOQ} + 40 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 40	mA
XC7K325T	I_{CCINTQ} + 600	I_{CCAUXQ} + 80	I_{CCOQ} + 40 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 40	mA
XC7K355T	I_{CCINTQ} + 1450	I_{CCAUXQ} + 109	I_{CCOQ} + 40 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 81	mA
XC7K410T	I_{CCINTQ} + 1500	I_{CCAUXQ} + 125	I_{CCOQ} + 40 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 90	mA
XC7K420T	I_{CCINTQ} + 2200	I_{CCAUXQ} + 180	I_{CCOQ} + 40 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 108	mA
XC7K480T	I_{CCINTQ} + 2200	I_{CCAUXQ} + 180	I_{CCOQ} + 40 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 108	mA

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Use the XPower Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate maximum power-on currents.

Table 8: **Power Supply Ramp Time**

Symbol	Description	Conditions	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}		0.2	50	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO}		0.2	50	ms
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}		0.2	50	ms
T_{VCCAUX_IO}	Ramp time from GND to 90% of V_{CCAUX_IO}		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM}		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$	$T_J = 100°C$[(1)]	–	500	ms
		$T_J = 85°C$[(1)]	–	800	
$T_{MGTAVCC}$	Ramp time from GND to 90% of $V_{MGTAVCC}$		0.2	50	ms
$T_{MGTAVTT}$	Ramp time from GND to 90% of $V_{MGTAVTT}$		0.2	50	ms
$T_{MGTVCCAUX}$	Ramp time from GND to 90% of $V_{MGTVCCAUX}$		0.2	50	ms

Notes:

1. Based on 240,000 power cycles with nominal V_{CCO} of 3.3V or 36,500 power cycles with a worst case V_{CCO} of 3.465V.

Table 17: **Maximum Physical Interface (PHY) Rate for Memory Interfaces (FFG Packages)(1)(2)**

Memory Standard	**I/O Bank Type**	V_{CCAUX_IO}	**Speed Grade**				**Units**
			1.0V			**0.9V**	
			-3	**-2/-2L**	**-1**	**-2L**	
4:1 Memory Controllers							
DDR3	HP	2.0V	1866	1866	1600	1333	Mb/s
	HP	1.8V	1600	1333	1066	1066	Mb/s
	HR	N/A	1066	1066	800	800	Mb/s
DDR3L	HP	2.0V	1600	1600	1333	1066	Mb/s
	HP	1.8V	1333	1066	800	800	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	2.0V	800	800	800	800	Mb/s
	HP	1.8V	800	800	800	800	Mb/s
	HR	N/A	800	800	800	800	Mb/s
RLDRAM III(3)	HP	2.0V	800	667	667	533	MHz
	HP	1.8V	550	500	450	450	MHz
	HR	N/A	N/A				
2:1 Memory Controllers							
DDR3	HP	2.0V	1066	1066	800	800	Mb/s
	HP	1.8V	1066	1066	800	800	Mb/s
	HR	N/A	1066	1066	800	800	Mb/s
DDR3L	HP	2.0V	1066	1066	800	800	Mb/s
	HP	1.8V	1066	1066	800	800	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	2.0V	800	800	800	800	Mb/s
	HP	1.8V					
	HR	N/A					
QDR II+(4)	HP	2.0V	550	500	450	450	MHz
	HP	1.8V					
	HR	N/A	500	450	400	400	MHz
RLDRAM II	HP	2.0V	533	500	450	450	MHz
	HP	1.8V					
	HR	N/A					
LPDDR2(3)	HP	2.0V	800	800	800	800	Mb/s
	HP	1.8V	800	800	800	800	Mb/s
	HR	N/A	800	667	667	667	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see UG586, *7 Series FPGAs Memory Interface Solutions User Guide*.
2. When using the internal V_{REF}, the maximum data rate is 800 Mb/s (400 MHz).
3. RLDRAM III (BL = 4, BL = 8) and LPDDR2 specifications have not been validated with memory IP.
4. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

IOB Pad Input/Output/3-State

Table 19 (3.3V high-range IOB (HR)) and Table 20 (1.8V high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than T_{IOTP} when the DCITERMDISABLE pin is used. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 19: **3.3V IOB High Range (HR) Switching Characteristics**

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVTTL_S4	1.31	1.42	1.64	1.51	5.27	5.63	6.05	4.13	6.03	6.49	7.04	4.64	ns
LVTTL_S8	1.31	1.42	1.64	1.51	4.45	4.83	5.30	3.86	5.21	5.69	6.29	4.38	ns
LVTTL_S12	1.31	1.42	1.64	1.51	4.45	4.83	5.29	3.84	5.21	5.69	6.28	4.36	ns
LVTTL_S16	1.31	1.42	1.64	1.51	3.47	3.88	4.40	3.39	4.23	4.74	5.39	3.91	ns
LVTTL_S24	1.31	1.42	1.64	1.51	3.58	3.99	4.51	3.61	4.34	4.85	5.50	4.13	ns
LVTTL_F4	1.31	1.42	1.64	1.51	4.70	4.98	5.29	3.58	5.46	5.84	6.28	4.09	ns
LVTTL_F8	1.31	1.42	1.64	1.51	3.66	4.06	4.56	3.06	4.42	4.92	5.55	3.58	ns
LVTTL_F12	1.31	1.42	1.64	1.51	3.66	4.06	4.56	3.05	4.42	4.92	5.55	3.56	ns
LVTTL_F16	1.31	1.42	1.64	1.51	2.57	2.85	3.15	2.88	3.33	3.71	4.14	3.39	ns
LVTTL_F24	1.31	1.42	1.64	1.51	2.41	2.64	2.89	2.94	3.17	3.50	3.88	3.45	ns
LVDS_25(1)	0.64	0.68	0.80	0.83	1.36	1.47	1.55	1.58	2.12	2.33	2.54	2.09	ns
MINI_LVDS_25	0.68	0.70	0.79	0.83	1.36	1.47	1.55	1.59	2.12	2.33	2.54	2.11	ns
BLVDS_25(1)	0.65	0.69	0.80	0.83	1.83	2.02	2.20	2.16	2.59	2.88	3.19	2.67	ns
RSDS_25 (point to point)(1)	0.63	0.68	0.79	0.83	1.36	1.48	1.55	1.59	2.12	2.34	2.54	2.11	ns
PPDS_25(1)	0.65	0.69	0.80	0.83	1.36	1.49	1.58	1.59	2.12	2.35	2.57	2.11	ns
TMDS_33(1)	0.72	0.76	0.86	0.83	1.43	1.54	1.60	1.70	2.19	2.40	2.59	2.22	ns
PCI33_3(1)	1.28	1.41	1.65	1.50	2.71	3.08	3.52	3.42	3.47	3.94	4.51	3.94	ns
HSUL_12	0.63	0.64	0.71	0.79	2.06	2.31	2.59	2.13	2.82	3.17	3.58	2.64	ns
DIFF_HSUL_12	0.58	0.61	0.70	0.81	1.83	2.04	2.26	1.92	2.59	2.90	3.25	2.44	ns
HSTL_I_S	0.61	0.64	0.73	0.79	1.55	1.69	1.80	1.91	2.31	2.55	2.79	2.42	ns
HSTL_II_S	0.61	0.64	0.73	0.78	1.21	1.34	1.43	1.70	1.97	2.20	2.42	2.22	ns
HSTL_I_18_S	0.64	0.67	0.76	0.79	1.28	1.39	1.45	1.58	2.04	2.25	2.44	2.09	ns
HSTL_II_18_S	0.64	0.67	0.76	0.79	1.18	1.31	1.40	1.69	1.94	2.17	2.39	2.20	ns
DIFF_HSTL_I_S	0.63	0.67	0.77	0.78	1.42	1.54	1.61	1.84	2.18	2.40	2.60	2.36	ns
DIFF_HSTL_II_S	0.63	0.67	0.77	0.79	1.15	1.24	1.27	1.78	1.91	2.10	2.26	2.30	ns
DIFF_HSTL_I_18_S	0.65	0.69	0.78	0.79	1.27	1.38	1.43	1.67	2.03	2.24	2.42	2.19	ns
DIFF_HSTL_II_18_S	0.65	0.69	0.78	0.81	1.14	1.23	1.26	1.72	1.90	2.09	2.25	2.23	ns

Table 20: **1.8V IOB High Performance (HP) Switching Characteristics**

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVDS	0.75	0.79	0.92	0.89	1.05	1.17	1.24	1.43	1.68	1.92	2.06	2.04	ns
HSUL_12	0.69	0.72	0.82	0.95	1.65	1.84	2.05	1.80	2.29	2.59	2.87	2.41	ns
DIFF_HSUL_12	0.69	0.72	0.82	0.92	1.65	1.84	2.05	1.47	2.29	2.59	2.87	2.08	ns
HSTL_I_S	0.68	0.72	0.82	0.84	1.15	1.28	1.38	1.46	1.79	2.03	2.20	2.07	ns
HSTL_II_S	0.68	0.72	0.82	0.84	1.05	1.17	1.26	1.44	1.69	1.93	2.08	2.05	ns
HSTL_I_18_S	0.70	0.72	0.82	0.86	1.12	1.24	1.34	1.41	1.75	2.00	2.16	2.02	ns
HSTL_II_18_S	0.70	0.72	0.82	0.86	1.06	1.18	1.26	1.44	1.70	1.94	2.08	2.05	ns
HSTL_I_12_S	0.68	0.72	0.82	0.94	1.14	1.27	1.37	1.43	1.78	2.02	2.20	2.04	ns
HSTL_I_DCI_S	0.68	0.72	0.82	0.78	1.11	1.23	1.33	1.36	1.74	1.99	2.15	1.98	ns
HSTL_II_DCI_S	0.68	0.72	0.82	0.78	1.05	1.17	1.26	1.33	1.69	1.93	2.08	1.94	ns
HSTL_II_T_DCI_S	0.70	0.72	0.82	0.76	1.15	1.28	1.38	1.40	1.78	2.03	2.20	2.01	ns
HSTL_I_DCI_18_S	0.70	0.72	0.82	0.76	1.11	1.23	1.33	1.36	1.74	1.99	2.15	1.98	ns
HSTL_II_DCI_18_S	0.70	0.72	0.82	0.76	1.05	1.16	1.24	1.32	1.69	1.92	2.06	1.93	ns
HSTL_II _T_DCI_18_S	0.70	0.72	0.82	0.76	1.11	1.23	1.33	1.36	1.74	1.99	2.15	1.98	ns
DIFF_HSTL_I_S	0.75	0.79	0.92	0.89	1.15	1.28	1.38	1.47	1.79	2.03	2.20	2.08	ns
DIFF_HSTL_II_S	0.75	0.79	0.92	0.89	1.05	1.17	1.26	1.47	1.69	1.93	2.08	2.08	ns
DIFF_HSTL_I_DCI_S	0.75	0.79	0.92	0.76	1.15	1.28	1.38	1.47	1.78	2.03	2.20	2.08	ns
DIFF_HSTL_II_DCI_S	0.75	0.79	0.92	0.76	1.05	1.17	1.26	1.40	1.69	1.93	2.08	2.01	ns
DIFF_HSTL_I_18_S	0.75	0.79	0.92	0.89	1.12	1.24	1.34	1.46	1.75	2.00	2.16	2.07	ns
DIFF_HSTL_II_18_S	0.75	0.79	0.92	0.89	1.06	1.18	1.26	1.47	1.70	1.94	2.08	2.08	ns
DIFF_HSTL_I_DCI_18_S	0.75	0.79	0.92	0.75	1.11	1.23	1.33	1.46	1.74	1.99	2.15	2.07	ns
DIFF_HSTL_II_DCI_18_S	0.75	0.79	0.92	0.75	1.05	1.16	1.24	1.41	1.69	1.92	2.06	2.02	ns
DIFF_HSTL_II _T_DCI_18_S	0.75	0.79	0.92	0.76	1.11	1.23	1.33	1.46	1.74	1.99	2.15	2.07	ns
HSTL_I_F	0.68	0.72	0.82	0.84	1.02	1.14	1.22	1.26	1.66	1.90	2.04	1.87	ns
HSTL_II_F	0.68	0.72	0.82	0.84	0.97	1.08	1.15	1.29	1.61	1.84	1.97	1.90	ns
HSTL_I_18_F	0.70	0.72	0.82	0.86	1.04	1.16	1.24	1.32	1.68	1.91	2.06	1.93	ns
HSTL_II_18_F	0.70	0.72	0.82	0.86	0.98	1.09	1.16	1.35	1.62	1.85	1.98	1.96	ns
HSTL_I_12_F	0.68	0.72	0.82	0.94	1.02	1.13	1.21	1.26	1.65	1.88	2.03	1.87	ns
HSTL_I_DCI_F	0.68	0.72	0.82	0.78	1.04	1.16	1.24	1.30	1.67	1.91	2.06	1.91	ns
HSTL_II_DCI_F	0.68	0.72	0.82	0.78	0.97	1.08	1.15	1.22	1.61	1.84	1.97	1.83	ns
HSTL_II_T_DCI_F	0.70	0.72	0.82	0.76	1.02	1.14	1.22	1.26	1.66	1.90	2.04	1.87	ns
HSTL_I_DCI_18_F	0.70	0.72	0.82	0.76	1.04	1.16	1.24	1.30	1.67	1.91	2.06	1.91	ns
HSTL_II_DCI_18_F	0.70	0.72	0.82	0.76	0.98	1.09	1.16	1.27	1.61	1.85	1.98	1.88	ns
HSTL_II _T_DCI_18_F	0.70	0.72	0.82	0.76	1.04	1.16	1.24	1.30	1.67	1.91	2.06	1.91	ns
DIFF_HSTL_I_F	0.75	0.79	0.92	0.89	1.02	1.14	1.22	1.35	1.66	1.90	2.04	1.96	ns
DIFF_HSTL_II_F	0.75	0.79	0.92	0.89	0.97	1.08	1.15	1.35	1.61	1.84	1.97	1.96	ns
DIFF_HSTL_I_DCI_F	0.75	0.79	0.92	0.76	1.02	1.14	1.22	1.35	1.66	1.90	2.04	1.96	ns

Table 20: **1.8V IOB High Performance (HP) Switching Characteristics** ***(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
DIFF_HSTL_II_DCI_F	0.75	0.79	0.92	0.76	0.97	1.08	1.15	1.30	1.61	1.84	1.97	1.91	ns
DIFF_HSTL_I_18_F	0.75	0.79	0.92	0.89	1.04	1.16	1.24	1.38	1.68	1.91	2.06	1.99	ns
DIFF_HSTL_II_18_F	0.75	0.79	0.92	0.89	0.98	1.09	1.16	1.40	1.62	1.85	1.98	2.01	ns
DIFF_HSTL_I_DCI_18_F	0.75	0.79	0.92	0.75	1.04	1.16	1.24	1.38	1.67	1.91	2.06	1.99	ns
DIFF_HSTL_II_DCI_18_F	0.75	0.79	0.92	0.75	0.98	1.09	1.16	1.33	1.61	1.85	1.98	1.94	ns
DIFF_HSTL_II _T_DCI_18_F	0.75	0.79	0.92	0.76	1.04	1.16	1.24	1.38	1.67	1.91	2.06	1.99	ns
LVCMOS18_S2	0.47	0.50	0.60	0.87	3.95	4.28	4.85	3.40	4.59	5.04	5.67	4.01	ns
LVCMOS18_S4	0.47	0.50	0.60	0.87	2.67	2.98	3.43	2.69	3.31	3.73	4.26	3.30	ns
LVCMOS18_S6	0.47	0.50	0.60	0.87	2.14	2.38	2.72	2.18	2.77	3.14	3.54	2.79	ns
LVCMOS18_S8	0.47	0.50	0.60	0.87	1.98	2.21	2.52	2.02	2.61	2.97	3.35	2.63	ns
LVCMOS18_S12	0.47	0.50	0.60	0.87	1.70	1.91	2.17	1.85	2.34	2.67	2.99	2.46	ns
LVCMOS18_S16	0.47	0.50	0.60	0.87	1.57	1.75	1.97	1.76	2.20	2.51	2.79	2.37	ns
LVCMOS18_F2	0.47	0.50	0.60	0.87	3.50	3.87	4.48	2.85	4.14	4.63	5.30	3.46	ns
LVCMOS18_F4	0.47	0.50	0.60	0.87	2.23	2.50	2.87	2.26	2.87	3.25	3.69	2.87	ns
LVCMOS18_F6	0.47	0.50	0.60	0.87	1.80	2.00	2.26	1.52	2.43	2.76	3.08	2.13	ns
LVCMOS18_F8	0.47	0.50	0.60	0.87	1.46	1.72	2.04	1.51	2.10	2.47	2.86	2.12	ns
LVCMOS18_F12	0.47	0.50	0.60	0.87	1.26	1.40	1.53	1.46	1.89	2.16	2.35	2.07	ns
LVCMOS18_F16	0.47	0.50	0.60	0.87	1.19	1.33	1.44	1.46	1.83	2.08	2.26	2.07	ns
LVCMOS15_S2	0.59	0.62	0.73	0.86	3.55	3.89	4.45	3.11	4.19	4.65	5.27	3.73	ns
LVCMOS15_S4	0.59	0.62	0.73	0.86	2.45	2.70	3.06	2.46	3.08	3.45	3.89	3.07	ns
LVCMOS15_S6	0.59	0.62	0.73	0.86	2.24	2.51	2.88	2.33	2.88	3.26	3.71	2.94	ns
LVCMOS15_S8	0.59	0.62	0.73	0.86	1.91	2.16	2.49	2.05	2.55	2.91	3.31	2.66	ns
LVCMOS15_S12	0.59	0.62	0.73	0.86	1.77	1.98	2.23	1.97	2.41	2.73	3.05	2.58	ns
LVCMOS15_S16	0.59	0.62	0.73	0.86	1.62	1.81	2.02	1.85	2.26	2.56	2.84	2.46	ns
LVCMOS15_F2	0.59	0.62	0.73	0.86	3.38	3.69	4.18	2.74	4.02	4.44	5.00	3.35	ns
LVCMOS15_F4	0.59	0.62	0.73	0.86	2.04	2.21	2.44	1.72	2.68	2.97	3.26	2.33	ns
LVCMOS15_F6	0.59	0.62	0.73	0.86	1.47	1.74	2.09	1.49	2.10	2.50	2.91	2.10	ns
LVCMOS15_F8	0.59	0.62	0.73	0.86	1.31	1.46	1.61	1.47	1.95	2.22	2.43	2.08	ns
LVCMOS15_F12	0.59	0.62	0.73	0.86	1.21	1.34	1.45	1.44	1.84	2.10	2.27	2.05	ns
LVCMOS15_F16	0.59	0.62	0.73	0.86	1.18	1.31	1.41	1.41	1.82	2.07	2.23	2.02	ns
LVCMOS12_S2	0.64	0.67	0.78	0.95	3.38	3.80	4.48	3.27	4.02	4.55	5.30	3.88	ns
LVCMOS12_S4	0.64	0.67	0.78	0.95	2.62	2.94	3.43	2.76	3.26	3.70	4.25	3.37	ns
LVCMOS12_S6	0.64	0.67	0.78	0.95	2.05	2.33	2.72	2.24	2.69	3.08	3.54	2.85	ns
LVCMOS12_S8	0.64	0.67	0.78	0.95	1.94	2.18	2.51	2.16	2.58	2.94	3.33	2.77	ns
LVCMOS12_F2	0.64	0.67	0.78	0.95	2.84	3.15	3.62	2.47	3.48	3.90	4.44	3.08	ns
LVCMOS12_F4	0.64	0.67	0.78	0.95	1.97	2.18	2.44	1.69	2.61	2.93	3.26	2.30	ns
LVCMOS12_F6	0.64	0.67	0.78	0.95	1.33	1.51	1.70	1.43	1.96	2.26	2.52	2.04	ns

Input/Output Delay Switching Characteristics

Table 26: **Input/Output Delay Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
IDELAYCTRL						
T_{DLYCCO_RDY}	Reset to Ready for IDELAYCTRL	3.22	3.22	3.22	3.22	µs
$F_{IDELAYCTRL\_REF}$	Attribute REFCLK frequency = 200.00(1)	200.00	200.00	200.00	200.00	MHz
	Attribute REFCLK frequency = 300.00(1)	300.00	300.00	N/A	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	±10	MHz
$T_{IDELAYCTRL\_RPW}$	Minimum Reset pulse width	52.00	52.00	52.00	52.00	ns
IDELAY/ODELAY						
$T_{IDELAYRESOLUTION}$	IDELAY/ODELAY chain delay resolution	1/(32 x 2 x F_{REF})				ps
$T_{IDELAYPAT\_JIT}$ and $T_{ODELAYPAT\_JIT}$	Pattern dependent period jitter in delay chain for clock pattern.(2)	0	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(3)	±5	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(4)	±9	±9	±9	±9	ps per tap
$T_{IDELAY\_CLK\_MAX}$/ $T_{ODELAY\_CLK\_MAX}$	Maximum frequency of CLK input to IDELAY/ODELAY	800.00	800.00	710.00	710.00	MHz
T_{IDCCK_CE} / T_{IDCKC_CE}	CE pin Setup/Hold with respect to C for IDELAY	0.11/0.10	0.14/0.12	0.18/0.14	0.14/0.16	ns
T_{ODCCK_CE} / T_{ODCKC_CE}	CE pin Setup/Hold with respect to C for ODELAY	0.14/0.03	0.16/0.04	0.19/0.05	0.28/0.06	ns
T_{IDCCK_INC}/ T_{IDCKC_INC}	INC pin Setup/Hold with respect to C for IDELAY	0.10/0.14	0.12/0.16	0.14/0.20	0.10/0.23	ns
T_{ODCCK_INC}/ T_{ODCKC_INC}	INC pin Setup/Hold with respect to C for ODELAY	0.10/0.07	0.12/0.08	0.13/0.09	0.19/0.16	ns
T_{IDCCK_RST}/ T_{IDCKC_RST}	RST pin Setup/Hold with respect to C for IDELAY	0.13/0.08	0.14/0.10	0.16/0.12	0.22/0.19	ns
T_{ODCCK_RST}/ T_{ODCKC_RST}	RST pin Setup/Hold with respect to C for ODELAY	0.16/0.04	0.19/0.06	0.24/0.08	0.32/0.11	ns
$T_{IDDO\_IDATAIN}$	Propagation delay through IDELAY	Note 5	Note 5	Note 5	Note 5	ps
$T_{ODDO\_ODATAIN}$	Propagation delay through ODELAY	Note 5	Note 5	Note 5	Note 5	ps

Notes:

1. Average Tap Delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY/ODELAY tap setting. See TRACE report for actual values.

CLB Switching Characteristics

Table 28: **CLB Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Combinatorial Delays						
T_{ILO}	An – Dn LUT address to A	0.05	0.05	0.06	0.07	ns, Max
T_{ILO_2}	An – Dn LUT address to AMUX/CMUX	0.15	0.16	0.19	0.22	ns, Max
T_{ILO_3}	An – Dn LUT address to BMUX_A	0.24	0.25	0.30	0.37	ns, Max
T_{ITO}	An – Dn inputs to A – D Q outputs	0.58	0.61	0.74	0.91	ns, Max
T_{AXA}	AX inputs to AMUX output	0.38	0.40	0.49	0.62	ns, Max
T_{AXB}	AX inputs to BMUX output	0.40	0.42	0.52	0.66	ns, Max
T_{AXC}	AX inputs to CMUX output	0.39	0.41	0.50	0.62	ns, Max
T_{AXD}	AX inputs to DMUX output	0.43	0.44	0.52	0.67	ns, Max
T_{BXB}	BX inputs to BMUX output	0.31	0.33	0.40	0.51	ns, Max
T_{BXD}	BX inputs to DMUX output	0.38	0.39	0.47	0.62	ns, Max
T_{CXC}	CX inputs to CMUX output	0.27	0.28	0.34	0.43	ns, Max
T_{CXD}	CX inputs to DMUX output	0.33	0.34	0.41	0.54	ns, Max
T_{DXD}	DX inputs to DMUX output	0.32	0.33	0.40	0.52	ns, Max
Sequential Delays						
T_{CKO}	Clock to AQ – DQ outputs	0.26	0.27	0.32	0.40	ns, Max
T_{SHCKO}	Clock to AMUX – DMUX outputs	0.32	0.32	0.39	0.46	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T_{AS}/T_{AH}	A_N – D_N input to CLK on A – D Flip Flops	0.01/0.12	0.02/0.13	0.03/0.18	0.02/0.18	ns, Min
T_{DICK}/T_{CKDI}	A_X – D_X input to CLK on A – D Flip Flops	0.04/0.14	0.04/0.14	0.05/0.20	0.05/0.21	ns, Min
	A_X – D_X input through MUXs and/or carry logic to CLK on A – D Flip Flops	0.36/0.10	0.37/0.11	0.46/0.16	0.56/0.15	ns, Min
T_{CECK_CLB}/ T_{CKCE_CLB}	CE input to CLK on A – D Flip Flops	0.19/0.05	0.20/0.05	0.25/0.05	0.24/0.04	ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D Flip Flops	0.30/0.05	0.31/0.07	0.37/0.09	0.48/0.05	ns, Min
Set/Reset						
T_{SRMIN}	SR input minimum pulse width	0.52	0.78	1.04	0.95	ns, Min
T_{RQ}	Delay from SR input to AQ – DQ flip-flops	0.38	0.38	0.46	0.59	ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops	0.34	0.35	0.43	0.54	ns, Max
F_{TOG}	Toggle frequency (for export control)	1818	1818	1818	1286	MHz

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 29: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Sequential Delays						
T_{SHCKO}	Clock to A – B outputs	0.68	0.70	0.85	1.08	ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs	0.91	0.95	1.15	1.44	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{DS_LRAM}/T_{DH_LRAM}	A – D inputs to CLK	0.45/0.23	0.45/0.24	0.54/0.27	0.69/0.33	ns, Min
T_{AS_LRAM}/T_{AH_LRAM}	Address An inputs to clock	0.13/0.50	0.14/0.50	0.17/0.58	0.21/0.63	ns, Min
	Address An inputs through MUXs and/or carry logic to clock	0.40/0.16	0.42/0.17	0.52/0.23	0.63/0.23	ns, Min
T_{WS_LRAM}/T_{WH_LRAM}	WE input to clock	0.29/0.09	0.30/0.09	0.36/0.09	0.46/0.10	ns, Min
T_{CECK_LRAM}/ T_{CKCE_LRAM}	CE input to CLK	0.29/0.09	0.30/0.09	0.37/0.09	0.47/0.10	ns, Min
Clock CLK						
T_{MPW}	Minimum pulse width	0.68	0.77	0.91	1.11	ns, Min
T_{MCP}	Minimum clock period	1.35	1.54	1.82	2.22	ns, Min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time.
2. T_{SHCKO} also represents the CLK to XMUX output. Refer to TRACE report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 30: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Sequential Delays						
T_{REG}	Clock to A – D outputs	0.96	0.98	1.20	1.35	ns, Max
T_{REG_MUX}	Clock to AMUX – DMUX output	1.19	1.23	1.50	1.72	ns, Max
T_{REG_M31}	Clock to DMUX output via M31 output	0.89	0.91	1.10	1.25	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{WS_SHFREG}/ T_{WH_SHFREG}	WE input	0.26/0.09	0.27/0.09	0.33/0.09	0.41/0.10	ns, Min
T_{CECK_SHFREG}/ T_{CKCE_SHFREG}	CE input to CLK	0.27/0.09	0.28/0.09	0.33/0.09	0.42/0.10	ns, Min
T_{DS_SHFREG}/ T_{DH_SHFREG}	A – D inputs to CLK	0.28/0.26	0.28/0.26	0.33/0.30	0.41/0.36	ns, Min
Clock CLK						
T_{MPW_SHFREG}	Minimum pulse width	0.55	0.65	0.78	0.91	ns, Min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time.

Table 36: **Horizontal Clock Buffer Switching Characteristics (BUFH)**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BHCKO_O}	BUFH delay from I to O	0.10	0.11	0.13	0.12	ns
$T_{BHCCK\_CE}/T_{BHCKC\_CE}$	CE pin Setup and Hold	0.20/0.16	0.23/0.20	0.38/0.21	0.28/0.09	ns
Maximum Frequency						
F_{MAX_BUFH}	Horizontal clock buffer (BUFH)	741.00	710.00	625.00	560.00	MHz

Table 37: **Duty Cycle Distortion and Clock-Tree Skew**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion(1)	All	0.20	0.20	0.20	0.25	ns
T_{CKSKEW}	Global Clock Tree Skew(2)	XC7K70T	0.29	0.40	0.40	0.47	ns
		XC7K160T	0.42	0.53	0.57	0.59	ns
		XC7K325T	0.59	0.74	0.79	0.91	ns
		XC7K355T	0.45	0.57	0.59	0.69	ns
		XC7K410T	0.60	0.74	0.79	0.91	ns
		XC7K420T	0.60	0.74	0.79	0.91	ns
		XC7K480T	0.60	0.74	0.79	0.91	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.12	0.12	0.12	0.12	ns
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region	All	0.02	0.02	0.02	0.03	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	0.15	0.15	ns

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the I/O flip flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx Timing Analyzer tools to evaluate clock skew specific to your application.

Table 42: Clock-Capable Clock Input to Output Delay With MMCM

Symbol	**Description**	**Device**	**Speed Grade**				**Units**
			1.0V			**0.9V**	
			-3	**-2/-2L**	**-1**	**-2L**	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* MMCM.							
$T_{ICKOFMMCMCC}$	Clock-capable clock input and OUTFF *with* MMCM	XC7K70T	0.95	0.95	0.95	1.74	ns
		XC7K160T	0.96	0.96	0.96	1.78	ns
		XC7K325T	1.00	1.00	1.00	1.82	ns
		XC7K355T	1.00	1.00	1.00	1.78	ns
		XC7K410T	1.00	1.00	1.00	1.82	ns
		XC7K420T	1.07	1.07	1.07	1.82	ns
		XC7K480T	1.07	1.07	1.07	1.82	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 43: Clock-Capable Clock Input to Output Delay With PLL

Symbol	**Description**	**Device**	**Speed Grade**				**Units**
			1.0V			**0.9V**	
			-3	**-2/-2L**	**-1**	**-2L**	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* PLL.							
$T_{ICKOFPLLCC}$	Clock-capable clock input and OUTFF *with* PLL	XC7K70T	0.84	0.84	0.84	1.45	ns
		XC7K160T	0.89	0.89	0.89	1.54	ns
		XC7K325T	0.89	0.89	0.89	1.54	ns
		XC7K355T	0.89	0.89	0.89	1.50	ns
		XC7K410T	0.89	0.89	0.89	1.54	ns
		XC7K420T	0.96	0.96	0.96	1.54	ns
		XC7K480T	0.96	0.96	0.96	1.54	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Table 44: Pin-to-Pin, Clock-to-Out using BUFIO

Symbol	**Description**	**Speed Grade**				**Units**
		1.0V			**0.9V**	
		-3	**-2/-2L**	**-1**	**-2L**	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* BUFIO.						
$T_{ICKOFCS}$	Clock-to-Out of I/O clock for HR I/O banks	4.93	5.52	6.20	6.97	ns
	Clock-to-Out of I/O clock for HP I/O banks	4.85	5.44	6.11	6.90	ns

Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Kintex-7 FPGA clock transmitter and receiver data-valid windows.

Table 50: **Package Skew**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package Skew(1)	XC7K70T	FBG484	108	ps
			FBG676	135	ps
		XC7K160T	FBG484	118	ps
			FBG676	136	ps
			FFG676	161	ps
		XC7K325T	FBG676	146	ps
			FFG676	154	ps
			FBG900	163	ps
			FFG900	161	ps
		XC7K355T	FFG901	149	ps
		XC7K410T	FBG676	165	ps
			FFG676	168	ps
			FBG900	151	ps
			FFG900	146	ps
		XC7K420T	FFG901	149	ps
			FFG1156	145	ps
		XC7K480T	FFG901	149	ps
			FFG1156	145	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

GTX Transceiver Specifications

GTX Transceiver DC Input and Output Levels

Table 51 summarizes the DC output specifications of the GTX transceivers in Kintex-7 FPGAs. Consult UG476: *7 Series FPGAs GTX/GTH Transceiver User Guide* for further details.

Table 51: **GTX Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPOUT}	Differential peak-to-peak output voltage[1]	Transmitter output swing is set to maximum setting	–	–	1000	mV
$V_{CMOUTDC}$	DC common mode output voltage.	Equation based	$V_{MGTAVTT} – DV_{PPOUT}/4$			mV
R_{OUT}	Differential output resistance		–	100	–	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	12	ps
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V_{IN}	Absolute input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–200	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–	2/3 $V_{MGTAVTT}$	–	mV
R_{IN}	Differential input resistance		–	100	–	Ω
C_{EXT}	Recommended external AC coupling capacitor[2]		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in UG476: *7 Series FPGAs GTX/GTH Transceiver User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

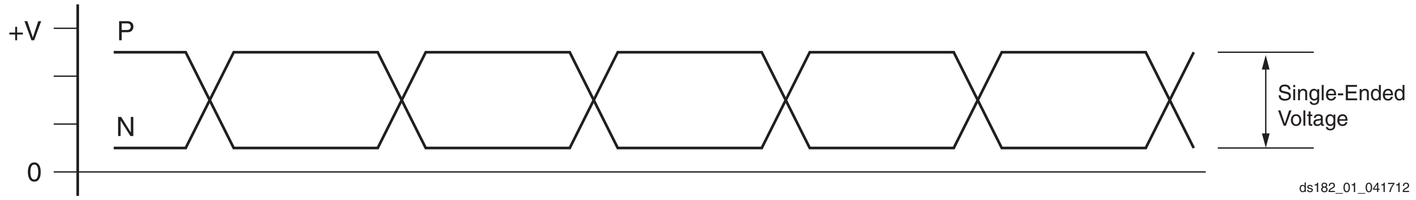

Figure 1: **Single-Ended Peak-to-Peak Voltage**

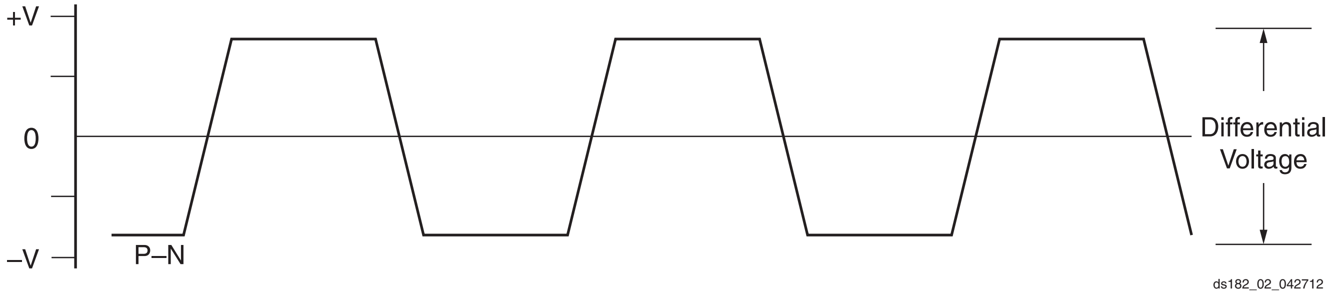

Figure 2: **Differential Peak-to-Peak Voltage**

Table 52 summarizes the DC specifications of the clock input of the GTX transceiver. Consult UG476: *7 Series FPGAs GTX/GTH Transceiver User Guide* for further details.

Table 52: **GTX Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTX Transceiver Switching Characteristics

Consult UG476: *7 Series FPGAs GTX/GTH Transceiver User Guide* for further information.

Table 53: **GTX Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade								Units
			1.0V						0.9V		
			-3		-2/-2L		-1[1]		-2L[2]		
			Package Type								
			FF	FB	FF	FB	FF	FB	FF	FB	
F_{GTXMAX}[3]	Maximum GTX transceiver data rate		12.5	6.6	10.3125	6.6	8.0	6.6	6.6	6.6	Gb/s
F_{GTXMIN}[3]	Minimum GTX transceiver data rate		0.500	0.500	0.500	0.500	0.500	0.500	0.500	0.500	Gb/s
$F_{GTXCRANGE}$	CPLL line rate range	1	3.2–6.6								Gb/s
		2	1.6–3.3								Gb/s
		4	0.8–1.65								Gb/s
		8	0.5–0.825								Gb/s
		16	N/A								Gb/s
$F_{GTXQRANGE1}$	QPLL line rate range 1	1	5.93–8.0	5.93–6.6	5.93–8.0	5.93–6.6	5.93–8.0	5.93–6.6	5.93–6.6		Gb/s
		2	2.965–4.0		2.965–4.0		2.965–4.0		2.965–3.3		Gb/s
		4	1.4825–2.0		1.4825–2.0		1.4825–2.0		1.4825–1.65		Gb/s
		8	0.74125–1.0		0.74125–1.0		0.74125–1.0		0.74125–0.825		Gb/s
		16	N/A		N/A		N/A		N/A		Gb/s
$F_{GTXQRANGE2}$	QPLL line rate range 2[4]	1	9.8–12.5	N/A	9.8–10.3125	N/A	N/A		N/A		Gb/s
		2	4.9–6.25		4.9–5.15625		N/A		N/A		Gb/s
		4	2.45–3.125		2.45–2.578125		N/A		N/A		Gb/s
		8	1.225–1.5625		1.225–1.2890625		N/A		N/A		Gb/s
		16	0.6125–0.78125		0.6125–0.64453125		N/A		N/A		Gb/s
$F_{GCPLLRANGE}$	GTX transceiver CPLL frequency range		1.6–3.3		1.6–3.3		1.6–3.3		1.6–3.3		GHz
$F_{GQPLLRANGE1}$	GTX transceiver QPLL frequency range 1		5.93–8.0		5.93–8.0		5.93–8.0		5.93–6.6		GHz

Table 56: GTX Transceiver PLL /Lock Time Adaptation

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37 x10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3 x10^6	UI

Table 57: GTX Transceiver User Clock Switching Characteristics(1)(2)

Symbol	Description	Conditions	Speed Grade				Units
			1.0V			0.9V	
			-3(3)	-2/-2L(3)	-1(4)	-2L(5)	
F_{TXOUT}	TXOUTCLK maximum frequency		412.54	412.54	312.50	237.53	MHz
F_{RXOUT}	RXOUTCLK maximum frequency		412.54	412.54	312.50	237.53	MHz
F_{TXIN}	TXUSRCLK maximum frequency	16-bit data path	412.54	412.54	312.50	237.53	MHz
		32-bit data path	391.08	322.37	250.00	206.27	MHz
F_{RXIN}	RXUSRCLK maximum frequency	16-bit data path	412.54	412.54	312.50	237.53	MHz
		32-bit data path	391.08	322.37	250.00	206.27	MHz
F_{TXIN2}	TXUSRCLK2 maximum frequency	16-bit data path	412.54	412.54	312.50	237.53	MHz
		32-bit data path	391.08	322.37	250.00	206.27	MHz
		64-bit data path	195.54	161.19	125.00	103.14	MHz
F_{RXIN2}	RXUSRCLK2 maximum frequency	16-bit data path	412.54	412.54	312.50	237.53	MHz
		32-bit data path	391.08	322.37	250.00	206.27	MHz
		64-bit data path	195.54	161.19	125.00	103.14	MHz

Notes:

1. Clocking must be implemented as described in UG476: *7 Series FPGAs GTX/GTH Transceiver User Guide*.
2. These frequencies are not supported for all possible transceiver configurations.
3. For speed grades -3, -2, -2L (1.0V), a 16-bit data path can only be used for speeds less than 6.6 Gb/s.
4. For speed grade -1, a 16-bit data path can only be used for speeds less than 5.0 Gb/s.
5. For speed grade -2L (0.9V), a 16-bit data path can only be used for speeds less than 3.8 Gb/s.

Table 58: GTX Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTXTX}	Serial data rate range		0.500	–	F_{GTXMAX}	Gb/s
T_{RTX}	TX Rise time	20%–80%	–	40	–	ps
T_{FTX}	TX Fall time	80%–20%	–	40	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	500	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	15	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	140	ns
$TJ_{12.5}$	Total Jitter(2)(4)	12.5 Gb/s	–	–	0.28	UI
$DJ_{12.5}$	Deterministic Jitter(2)(4)		–	–	0.17	UI
$TJ_{11.18}$	Total Jitter(2)(4)	11.18 Gb/s	–	–	0.28	UI
$DJ_{11.18}$	Deterministic Jitter(2)(4)		–	–	0.17	UI

Table 63: CEI-6G and CEI-11G Protocol Characteristics

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter[1]	4976–6375	CEI-6G-SR	–	0.3	UI
		CEI-6G-LR	–	0.3	UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance[1]	4976–6375	CEI-6G-SR	0.6	–	UI
		CEI-6G-LR	0.95	–	UI
CEI-11G Transmitter Jitter Generation					
Total transmitter jitter[2]	9950–11100	CEI-11G-SR	–	0.3	UI
		CEI-11G-LR/MR	–	0.3	UI
CEI-11G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance[2]	9950–11100	CEI-11G-SR	0.65	–	UI
		CEI-11G-MR	0.65	–	UI
		CEI-11G-LR	0.825	–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.
2. Tested at line rate of 9950 Mb/s using 155.46875 MHz reference clock and 11100 Mb/s using 173.4375 MHz reference clock.

Table 64: SFP+ Protocol Characteristics

Description	Line Rate (Mb/s)	Min	Max	Units
SFP+ Transmitter Jitter Generation				
Total transmitter jitter	9830.40[1]	–	0.28	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			
SFP+ Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	9830.40[1]	0.7	–	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			

Notes:

1. Line rated used for CPRI over SFP+ applications.

XADC Specifications

Table 67: **XADC Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V_{CCADC} = 1.8V ± 5%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 26 MHz, T_j = –40°C to 100°C, Typical values at T_j=+40°C						
ADC Accuracy[1]						
Resolution			12	–	–	Bits
Integral Nonlinearity[2]	INL		–	–	±3	LSBs
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset Error		Offset calibration enabled	–	–	±6	LSBs
Gain Error		Gain calibration disabled	–	–	±0.5	%
Offset Matching		Offset calibration enabled	–	–	4	LSBs
Gain Matching		Gain calibration disabled	–	–	0.3	%
Sample Rate			0.1	–	1	MS/s
Signal to Noise Ratio[2]	SNR	F_{SAMPLE} = 500KS/s, F_{IN} = 20KHz	60	–	–	dB
RMS Code Noise		External 1.25V reference	–	–	2	LSBs
		On-chip reference	–	3	–	LSBs
Total Harmonic Distortion[2]	THD	F_{SAMPLE} = 500KS/s, F_{IN} = 20KHz	–	70	–	dB
ADC Accuracy at Extended Temperatures (-55°C to 125°C)						
Resolution			10	–	–	Bits
Integral Nonlinearity[2]	INL		–	–	±1	LSB (at 10 bits)
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	
Analog Inputs[3]						
ADC Input Ranges		Unipolar operation	0	–	1	V
		Bipolar operation	–0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum External Channel Input Ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	–0.1	–	V_{CCADC}	V
Auxiliary Channel Full Resolution Bandwidth	FRBW		250	–	–	KHz
On-Chip Sensors						
Temperature Sensor Error		T_j = –40°C to 100°C.	–	–	±4	°C
		T_j = –55°C to +125°C	–	–	±6	°C
Supply Sensor Error		Measurement range of V_{CCAUX} 1.8V ±5% T_j = –40°C to +100°C	–	–	±1	%
		Measurement range of V_{CCAUX} 1.8V ±5% T_j = –55°C to +125°C	–	–	±2	%
Conversion Rate[4]						
Conversion Time - Continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	Cycles
Conversion Time - Event	t_{CONV}	Number of CLK cycles	–	–	21	Cycles
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	26	MHz
DCLK Duty Cycle			40	–	60	%

Date	Version	Description
07/25/12	1.6	Updated the descriptions, changed V_{IN} and Note 2 and added Note 4 in Table 1. In Table 2, changed descriptions and notes, removed Note 7, changed GTX transceiver parameters and values and added Note 9. Updated parameters in Table 3. Added Table 4 and Table 5. Changed the typical values for many of the devices in Table 7. Updated LVCMOS12 and the SSTLs in Table 9. Updated many of the specifications in Table 10 and Table 11. Updated speed specification to v1.06 (-3, -2, -2L(1.0V), -1) and v1.05 (-2L(0.9V)) with appropriate changes to Table 14 and Table 15 including production release of the XC7K325T and the XC7K410T in the -2, -2L(1.0V), and -1 speed designations. Added notes and specifications to Table 17 and Table 18. Updated the IOB Pad Input/Output/3-State discussion and changed Table 21 by adding $T_{IOIBUFDISABLE}$. Removed many of the combinatorial delay specifications and T_{CINCK}/T_{CKCIN} from Table 28. Rearranged Table 51 including moving some parameters to Table 1. Added Table 56. Updated Table 57. In Table 59, updated SJ Jitter Tolerance with Stressed Eye section, page 51 and Note 8. Added Note 1, Note 2, and Note 3 to Table 62. Added Note 1 and Note 2 to Table 63, and line rate ranges. Updated Table 64 including adding Note 1. Updated Table 65 including adding Note 1. In Table 67 updated Note 1 and added Note 4. In Table 68, updated T_{POR} and F_{EMCCK}.
09/04/12	1.7	Updated Table 14 and Table 15 for production release of the XC7K160T in the -2, -2L(1.0V), and -1 speed designations.
09/26/12	1.8	In Table 2, revised V_{CCINT} and V_{CCBRAM} and added Note 2. Updated Table 14 and Table 15 for production release of the XC7K480T in the -2, -2L(1.0V), and -1 speed designations and the XC7K325T and XC7K410T in the -3 speed designation.
10/10/12	1.9	Updated the $I_{CCINTMIN}$ value for the XC7K355T in Table 7. Updated Table 14 and Table 15 for production release of the XC7K420T in the -2, -2L(1.0V), and -1 speed designations.
10/25/12	2.0	Updated the AC Switching Characteristics based upon ISE 14.3 v1.07 for the -3, -2, -2L (1.0V), -1 speed specifications, and ISE 14.3 v1.06 for the -2L (0.9V) speed specifications throughout the document. Updated Table 14 and Table 15 for production release of the XC7K355T in the -2, -2L(1.0V), and -1 speed designations. Also updated Table 14 and Table 15 for production release of the XC7K325T and XC7K410T in the -2L (0.9V). Added values for Table 16 -2L (0.9V). Added package skew values to Table 50. In Table 53, increased -1 speed grade (FF package) F_{GTXMAX} value from 6.6 Gb/s to 8.0 Gb/s.
10/31/12	2.1	Updated Table 14 and Table 15 for production release of the XC7K70T in the -2, -2L(1.0V), and -1 speed designations.
11/26/12	2.2	Updated Table 14 and Table 15 for production release of -3 speed designation for XC7K70T, XC7K160T, XC7K355T, XC7K420T, and XC7K480T. Removed Note 4 from Table 67.
12/05/12	2.3	Updated Table 14 and Table 15 for production release of the -2L (0.9V) speed designation for XC7K160T, XC7K420T, and XC7K480T. Updated Note 1 in Table 50.
12/12/12	2.4	Updated Table 14 and Table 15 for production release of the -2L (0.9V) speed designation for XC7K70T and XC7K355T. Added Internal Configuration Access Port section to Table 68.