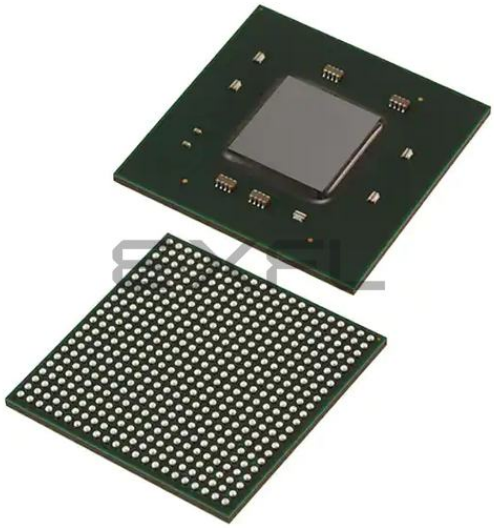
# AMD Xilinx - XC7K70T-3FBG484E Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 5125 |
| Number of Logic Elements/Cells | 65600 |
| Total RAM Bits | 4976640 |
| Number of I/O | 285 |
| Number of Gates | - |
| Voltage - Supply | 0.97V ~ 1.03V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 100°C (TJ) |
| Package / Case | 484-BBGA, FCBGA |
| Supplier Device Package | 484-FCBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc7k70t-3fbg484e |

*Table 6:* **Typical Quiescent Supply Current *(Cont'd)***

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| $I_{CCBRAMQ}$ | Quiescent $V_{CCBRAM}$ supply current | XC7K70T | 6 | 6 | 6 | 6 | mA |
| | | XC7K160T | 14 | 14 | 14 | 14 | mA |
| | | XC7K325T | 19 | 19 | 19 | 19 | mA |
| | | XC7K355T | 31 | 31 | 31 | 31 | mA |
| | | XC7K410T | 34 | 34 | 34 | 34 | mA |
| | | XC7K420T | 41 | 41 | 41 | 41 | mA |
| | | XC7K480T | 41 | 41 | 41 | 41 | mA |

**Notes:**

1. Typical values are specified at nominal voltage, 85°C junction temperatures ($T_j$) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the XPower™ Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified.

## Power-On/Off Power Supply Sequencing

The recommended power-on sequence is $V_{CCINT}$, $V_{CCBRAM}$, $V_{CCAUX}$, $V_{CCAUX\_IO}$, and $V_{CCO}$ to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If $V_{CCINT}$ and $V_{CCBRAM}$ have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If $V_{CCAUX}$, $V_{CCAUX\_IO}$, and $V_{CCO}$ have the same recommended voltage levels then they can be powered by the same supply and ramped simultaneously.

For $V_{CCO}$ voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between $V_{CCO}$ and $V_{CCAUX}$ must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTX transceivers is $V_{CCINT}$, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, $V_{CCINT}$, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and $V_{CCINT}$ can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} - V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to 0.3 x $T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before $V_{CCINT}$ and $V_{MGTAVTT} - V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during $V_{CCINT}$ ramp up. The duration of the current draw can be up to 0.3 x $T_{VCCINT}$ (ramp time from GND to 90% of $V_{CCINT}$). The reverse is true for power-down.

## LVDS DC Specifications (LVDS_25)

The LVDS_25 standard is available in the HR I/O banks. See UG471: *7 Series FPGAs SelectIO Resources User Guide* for more information.

*Table 12:* **LVDS_25 DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply Voltage | | 2.375 | 2.500 | 2.625 | V |
| $V_{OH}$ | Output High Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | – | – | 1.675 | V |
| $V_{OL}$ | Output Low Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 0.700 | – | – | V |
| $V_{ODIFF}$ | Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 247 | 350 | 600 | mV |
| $V_{OCM}$ | Output Common-Mode Voltage | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 1.000 | 1.250 | 1.425 | V |
| $V_{IDIFF}$ | Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High | | 100 | 350 | 600 | mV |
| $V_{ICM}$ | Input Common-Mode Voltage | | 0.300 | 1.200 | 1.425 | V |

## LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks. See UG471: *7 Series FPGAs SelectIO Resources User Guide* for more information.

*Table 13:* **LVDS DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply Voltage | | 1.710 | 1.800 | 1.890 | V |
| $V_{OH}$ | Output High Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | – | – | 1.675 | V |
| $V_{OL}$ | Output Low Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 0.825 | – | – | V |
| $V_{ODIFF}$ | Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 247 | 350 | 600 | mV |
| $V_{OCM}$ | Output Common-Mode Voltage | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 1.000 | 1.250 | 1.425 | V |
| $V_{IDIFF}$ | Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High | Common-mode input voltage = 1.25V | 100 | 350 | 600 | mV |
| $V_{ICM}$ | Input Common-Mode Voltage | Differential input voltage = ±350 mV | 0.300 | 1.200 | 1.425 | V |

# AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in ISE® software 14.3 v1.07 for the -3, -2, -2L(1.0V), -1, and v1.06 for -2L(0.9V) speed grades.

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

***Advance Product Specification***

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

***Preliminary Product Specification***

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

***Product Specification***

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

## Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Kintex-7 FPGAs.

## Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 14 correlates the current status of each Kintex-7 device on a per speed grade basis.

*Table 14:* **Kintex-7 Device Speed Grade Designations**

| Device | Speed Grade Designations | | |
|---|---|---|---|
| | Advance | Preliminary | Production |
| XC7K70T | | | -3, -2, -2L(1.0V), -1, and -2L (0.9V) |
| XC7K160T | | | -3, -2, -2L(1.0V), -1, and -2L (0.9V) |
| XC7K325T | | | -3, -2, -2L(1.0V), -1, and -2L (0.9V) |
| XC7K355T | | | -3, -2, -2L(1.0V), -1, and -2L (0.9V) |
| XC7K410T | | | -3, -2, -2L(1.0V), -1, and -2L (0.9V) |
| XC7K420T | | | -3, -2, -2L(1.0V), -1, and -2L (0.9V) |
| XC7K480T | | | -3, -2, -2L(1.0V), -1, and -2L (0.9V) |

## IOB Pad Input/Output/3-State

Table 19 (3.3V high-range IOB (HR)) and Table 20 (1.8V high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{IOPI}$ is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{IOOP}$ is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{IOTP}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than $T_{IOTP}$ when the DCITERMDISABLE pin is used. In HR I/O banks, the IN_TERM termination turn-on time is always faster than $T_{IOTP}$ when the INTERMDISABLE pin is used.

*Table 19:* **3.3V IOB High Range (HR) Switching Characteristics**

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | 1.0V | | | 0.9V | 1.0V | | | 0.9V | 1.0V | | | 0.9V | |
| | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | |
| LVTTL_S4 | 1.31 | 1.42 | 1.64 | 1.51 | 5.27 | 5.63 | 6.05 | 4.13 | 6.03 | 6.49 | 7.04 | 4.64 | ns |
| LVTTL_S8 | 1.31 | 1.42 | 1.64 | 1.51 | 4.45 | 4.83 | 5.30 | 3.86 | 5.21 | 5.69 | 6.29 | 4.38 | ns |
| LVTTL_S12 | 1.31 | 1.42 | 1.64 | 1.51 | 4.45 | 4.83 | 5.29 | 3.84 | 5.21 | 5.69 | 6.28 | 4.36 | ns |
| LVTTL_S16 | 1.31 | 1.42 | 1.64 | 1.51 | 3.47 | 3.88 | 4.40 | 3.39 | 4.23 | 4.74 | 5.39 | 3.91 | ns |
| LVTTL_S24 | 1.31 | 1.42 | 1.64 | 1.51 | 3.58 | 3.99 | 4.51 | 3.61 | 4.34 | 4.85 | 5.50 | 4.13 | ns |
| LVTTL_F4 | 1.31 | 1.42 | 1.64 | 1.51 | 4.70 | 4.98 | 5.29 | 3.58 | 5.46 | 5.84 | 6.28 | 4.09 | ns |
| LVTTL_F8 | 1.31 | 1.42 | 1.64 | 1.51 | 3.66 | 4.06 | 4.56 | 3.06 | 4.42 | 4.92 | 5.55 | 3.58 | ns |
| LVTTL_F12 | 1.31 | 1.42 | 1.64 | 1.51 | 3.66 | 4.06 | 4.56 | 3.05 | 4.42 | 4.92 | 5.55 | 3.56 | ns |
| LVTTL_F16 | 1.31 | 1.42 | 1.64 | 1.51 | 2.57 | 2.85 | 3.15 | 2.88 | 3.33 | 3.71 | 4.14 | 3.39 | ns |
| LVTTL_F24 | 1.31 | 1.42 | 1.64 | 1.51 | 2.41 | 2.64 | 2.89 | 2.94 | 3.17 | 3.50 | 3.88 | 3.45 | ns |
| LVDS_25(1) | 0.64 | 0.68 | 0.80 | 0.83 | 1.36 | 1.47 | 1.55 | 1.58 | 2.12 | 2.33 | 2.54 | 2.09 | ns |
| MINI_LVDS_25 | 0.68 | 0.70 | 0.79 | 0.83 | 1.36 | 1.47 | 1.55 | 1.59 | 2.12 | 2.33 | 2.54 | 2.11 | ns |
| BLVDS_25(1) | 0.65 | 0.69 | 0.80 | 0.83 | 1.83 | 2.02 | 2.20 | 2.16 | 2.59 | 2.88 | 3.19 | 2.67 | ns |
| RSDS_25 (point to point)(1) | 0.63 | 0.68 | 0.79 | 0.83 | 1.36 | 1.48 | 1.55 | 1.59 | 2.12 | 2.34 | 2.54 | 2.11 | ns |
| PPDS_25(1) | 0.65 | 0.69 | 0.80 | 0.83 | 1.36 | 1.49 | 1.58 | 1.59 | 2.12 | 2.35 | 2.57 | 2.11 | ns |
| TMDS_33(1) | 0.72 | 0.76 | 0.86 | 0.83 | 1.43 | 1.54 | 1.60 | 1.70 | 2.19 | 2.40 | 2.59 | 2.22 | ns |
| PCI33_3(1) | 1.28 | 1.41 | 1.65 | 1.50 | 2.71 | 3.08 | 3.52 | 3.42 | 3.47 | 3.94 | 4.51 | 3.94 | ns |
| HSUL_12 | 0.63 | 0.64 | 0.71 | 0.79 | 2.06 | 2.31 | 2.59 | 2.13 | 2.82 | 3.17 | 3.58 | 2.64 | ns |
| DIFF_HSUL_12 | 0.58 | 0.61 | 0.70 | 0.81 | 1.83 | 2.04 | 2.26 | 1.92 | 2.59 | 2.90 | 3.25 | 2.44 | ns |
| HSTL_I_S | 0.61 | 0.64 | 0.73 | 0.79 | 1.55 | 1.69 | 1.80 | 1.91 | 2.31 | 2.55 | 2.79 | 2.42 | ns |
| HSTL_II_S | 0.61 | 0.64 | 0.73 | 0.78 | 1.21 | 1.34 | 1.43 | 1.70 | 1.97 | 2.20 | 2.42 | 2.22 | ns |
| HSTL_I_18_S | 0.64 | 0.67 | 0.76 | 0.79 | 1.28 | 1.39 | 1.45 | 1.58 | 2.04 | 2.25 | 2.44 | 2.09 | ns |
| HSTL_II_18_S | 0.64 | 0.67 | 0.76 | 0.79 | 1.18 | 1.31 | 1.40 | 1.69 | 1.94 | 2.17 | 2.39 | 2.20 | ns |
| DIFF_HSTL_I_S | 0.63 | 0.67 | 0.77 | 0.78 | 1.42 | 1.54 | 1.61 | 1.84 | 2.18 | 2.40 | 2.60 | 2.36 | ns |
| DIFF_HSTL_II_S | 0.63 | 0.67 | 0.77 | 0.79 | 1.15 | 1.24 | 1.27 | 1.78 | 1.91 | 2.10 | 2.26 | 2.30 | ns |
| DIFF_HSTL_I_18_S | 0.65 | 0.69 | 0.78 | 0.79 | 1.27 | 1.38 | 1.43 | 1.67 | 2.03 | 2.24 | 2.42 | 2.19 | ns |
| DIFF_HSTL_II_18_S | 0.65 | 0.69 | 0.78 | 0.81 | 1.14 | 1.23 | 1.26 | 1.72 | 1.90 | 2.09 | 2.25 | 2.23 | ns |

*Table 19:* **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | 1.0V | | | 0.9V | 1.0V | | | 0.9V | 1.0V | | | 0.9V | |
| | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | |
| HSTL_I_F | 0.61 | 0.64 | 0.73 | 0.79 | 1.10 | 1.19 | 1.23 | 1.41 | 1.86 | 2.05 | 2.22 | 1.92 | ns |
| HSTL_II_F | 0.61 | 0.64 | 0.73 | 0.78 | 1.05 | 1.18 | 1.28 | 1.42 | 1.81 | 2.04 | 2.27 | 1.94 | ns |
| HSTL_I_18_F | 0.64 | 0.67 | 0.76 | 0.79 | 1.05 | 1.18 | 1.28 | 1.44 | 1.81 | 2.04 | 2.27 | 1.95 | ns |
| HSTL_II_18_F | 0.64 | 0.67 | 0.76 | 0.79 | 1.03 | 1.14 | 1.23 | 1.42 | 1.79 | 2.00 | 2.22 | 1.94 | ns |
| DIFF_HSTL_I_F | 0.63 | 0.67 | 0.77 | 0.78 | 1.09 | 1.18 | 1.22 | 1.48 | 1.85 | 2.04 | 2.21 | 2.00 | ns |
| DIFF_HSTL_II_F | 0.63 | 0.67 | 0.77 | 0.79 | 1.02 | 1.11 | 1.14 | 1.48 | 1.78 | 1.97 | 2.13 | 2.00 | ns |
| DIFF_HSTL_I_18_F | 0.65 | 0.69 | 0.78 | 0.79 | 1.08 | 1.17 | 1.21 | 1.48 | 1.84 | 2.03 | 2.20 | 2.00 | ns |
| DIFF_HSTL_II_18_F | 0.65 | 0.69 | 0.78 | 0.81 | 1.01 | 1.10 | 1.13 | 1.48 | 1.77 | 1.96 | 2.12 | 2.00 | ns |
| LVCMOS33_S4 | 1.31 | 1.40 | 1.60 | 1.54 | 5.23 | 5.61 | 6.09 | 4.13 | 5.99 | 6.47 | 7.08 | 4.64 | ns |
| LVCMOS33_S8 | 1.31 | 1.40 | 1.60 | 1.54 | 4.46 | 4.85 | 5.33 | 3.84 | 5.22 | 5.71 | 6.32 | 4.36 | ns |
| LVCMOS33_S12 | 1.31 | 1.40 | 1.60 | 1.54 | 3.46 | 3.89 | 4.42 | 3.41 | 4.22 | 4.75 | 5.41 | 3.92 | ns |
| LVCMOS33_S16 | 1.31 | 1.40 | 1.60 | 1.54 | 3.06 | 3.43 | 3.88 | 3.72 | 3.82 | 4.29 | 4.87 | 4.23 | ns |
| LVCMOS33_F4 | 1.31 | 1.40 | 1.60 | 1.54 | 4.70 | 5.01 | 5.36 | 3.58 | 5.46 | 5.87 | 6.35 | 4.09 | ns |
| LVCMOS33_F8 | 1.31 | 1.40 | 1.60 | 1.54 | 3.62 | 4.04 | 4.56 | 3.06 | 4.38 | 4.90 | 5.55 | 3.58 | ns |
| LVCMOS33_F12 | 1.31 | 1.40 | 1.60 | 1.54 | 2.57 | 2.85 | 3.15 | 2.88 | 3.33 | 3.71 | 4.14 | 3.39 | ns |
| LVCMOS33_F16 | 1.31 | 1.40 | 1.60 | 1.54 | 2.44 | 2.69 | 2.96 | 2.88 | 3.20 | 3.55 | 3.95 | 3.39 | ns |
| LVCMOS25_S4 | 1.08 | 1.16 | 1.32 | 1.36 | 4.49 | 4.80 | 5.16 | 3.44 | 5.25 | 5.66 | 6.15 | 3.95 | ns |
| LVCMOS25_S8 | 1.08 | 1.16 | 1.32 | 1.36 | 3.66 | 4.04 | 4.49 | 3.20 | 4.42 | 4.90 | 5.48 | 3.72 | ns |
| LVCMOS25_S12 | 1.08 | 1.16 | 1.32 | 1.36 | 2.77 | 3.10 | 3.49 | 2.80 | 3.53 | 3.96 | 4.48 | 3.31 | ns |
| LVCMOS25_S16 | 1.08 | 1.16 | 1.32 | 1.36 | 3.24 | 3.62 | 4.09 | 3.14 | 4.00 | 4.48 | 5.08 | 3.66 | ns |
| LVCMOS25_F4 | 1.08 | 1.16 | 1.32 | 1.36 | 3.96 | 4.31 | 4.72 | 3.06 | 4.72 | 5.17 | 5.71 | 3.58 | ns |
| LVCMOS25_F8 | 1.08 | 1.16 | 1.32 | 1.36 | 2.43 | 2.87 | 3.42 | 2.50 | 3.19 | 3.73 | 4.41 | 3.02 | ns |
| LVCMOS25_F12 | 1.08 | 1.16 | 1.32 | 1.36 | 2.23 | 2.63 | 3.13 | 2.48 | 2.99 | 3.49 | 4.12 | 3.00 | ns |
| LVCMOS25_F16 | 1.08 | 1.16 | 1.32 | 1.36 | 1.92 | 2.17 | 2.45 | 2.33 | 2.68 | 3.03 | 3.44 | 2.84 | ns |
| LVCMOS18_S4 | 0.64 | 0.66 | 0.74 | 0.87 | 3.24 | 3.45 | 3.66 | 1.91 | 4.00 | 4.31 | 4.65 | 2.42 | ns |
| LVCMOS18_S8 | 0.64 | 0.66 | 0.74 | 0.87 | 2.58 | 2.91 | 3.31 | 2.50 | 3.34 | 3.77 | 4.30 | 3.02 | ns |
| LVCMOS18_S12 | 0.64 | 0.66 | 0.74 | 0.87 | 2.58 | 2.91 | 3.31 | 2.50 | 3.34 | 3.77 | 4.30 | 3.02 | ns |
| LVCMOS18_S16 | 0.64 | 0.66 | 0.74 | 0.87 | 1.82 | 2.03 | 2.24 | 1.84 | 2.58 | 2.89 | 3.23 | 2.36 | ns |
| LVCMOS18_S24(1) | 0.64 | 0.66 | 0.74 | 0.87 | 1.74 | 1.92 | 2.08 | 1.92 | 2.50 | 2.78 | 3.07 | 2.44 | ns |
| LVCMOS18_F4 | 0.64 | 0.66 | 0.74 | 0.87 | 3.12 | 3.31 | 3.49 | 1.77 | 3.88 | 4.17 | 4.48 | 2.28 | ns |
| LVCMOS18_F8 | 0.64 | 0.66 | 0.74 | 0.87 | 1.91 | 2.13 | 2.36 | 2.00 | 2.67 | 2.99 | 3.35 | 2.52 | ns |
| LVCMOS18_F12 | 0.64 | 0.66 | 0.74 | 0.87 | 1.91 | 2.13 | 2.36 | 2.00 | 2.67 | 2.99 | 3.35 | 2.52 | ns |
| LVCMOS18_F16 | 0.64 | 0.66 | 0.74 | 0.87 | 1.52 | 1.68 | 1.81 | 1.72 | 2.28 | 2.54 | 2.80 | 2.23 | ns |
| LVCMOS18_F24(1) | 0.64 | 0.66 | 0.74 | 0.87 | 1.34 | 1.46 | 1.55 | 1.66 | 2.10 | 2.32 | 2.54 | 2.17 | ns |
| LVCMOS15_S4 | 0.66 | 0.69 | 0.81 | 0.90 | 3.48 | 3.74 | 4.03 | 2.22 | 4.24 | 4.60 | 5.02 | 2.73 | ns |
| LVCMOS15_S8 | 0.66 | 0.69 | 0.81 | 0.90 | 2.37 | 2.67 | 3.01 | 2.41 | 3.13 | 3.53 | 4.00 | 2.92 | ns |
| LVCMOS15_S12 | 0.66 | 0.69 | 0.81 | 0.90 | 1.83 | 2.03 | 2.23 | 1.91 | 2.59 | 2.89 | 3.22 | 2.42 | ns |

*Table 20:* **1.8V IOB High Performance (HP) Switching Characteristics**

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | 1.0V | | | 0.9V | 1.0V | | | 0.9V | 1.0V | | | 0.9V | |
| | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | -3 | -2/-2L | -1 | -2L | |
| LVDS | 0.75 | 0.79 | 0.92 | 0.89 | 1.05 | 1.17 | 1.24 | 1.43 | 1.68 | 1.92 | 2.06 | 2.04 | ns |
| HSUL_12 | 0.69 | 0.72 | 0.82 | 0.95 | 1.65 | 1.84 | 2.05 | 1.80 | 2.29 | 2.59 | 2.87 | 2.41 | ns |
| DIFF_HSUL_12 | 0.69 | 0.72 | 0.82 | 0.92 | 1.65 | 1.84 | 2.05 | 1.47 | 2.29 | 2.59 | 2.87 | 2.08 | ns |
| HSTL_I_S | 0.68 | 0.72 | 0.82 | 0.84 | 1.15 | 1.28 | 1.38 | 1.46 | 1.79 | 2.03 | 2.20 | 2.07 | ns |
| HSTL_II_S | 0.68 | 0.72 | 0.82 | 0.84 | 1.05 | 1.17 | 1.26 | 1.44 | 1.69 | 1.93 | 2.08 | 2.05 | ns |
| HSTL_I_18_S | 0.70 | 0.72 | 0.82 | 0.86 | 1.12 | 1.24 | 1.34 | 1.41 | 1.75 | 2.00 | 2.16 | 2.02 | ns |
| HSTL_II_18_S | 0.70 | 0.72 | 0.82 | 0.86 | 1.06 | 1.18 | 1.26 | 1.44 | 1.70 | 1.94 | 2.08 | 2.05 | ns |
| HSTL_I_12_S | 0.68 | 0.72 | 0.82 | 0.94 | 1.14 | 1.27 | 1.37 | 1.43 | 1.78 | 2.02 | 2.20 | 2.04 | ns |
| HSTL_I_DCI_S | 0.68 | 0.72 | 0.82 | 0.78 | 1.11 | 1.23 | 1.33 | 1.36 | 1.74 | 1.99 | 2.15 | 1.98 | ns |
| HSTL_II_DCI_S | 0.68 | 0.72 | 0.82 | 0.78 | 1.05 | 1.17 | 1.26 | 1.33 | 1.69 | 1.93 | 2.08 | 1.94 | ns |
| HSTL_II_T_DCI_S | 0.70 | 0.72 | 0.82 | 0.76 | 1.15 | 1.28 | 1.38 | 1.40 | 1.78 | 2.03 | 2.20 | 2.01 | ns |
| HSTL_I_DCI_18_S | 0.70 | 0.72 | 0.82 | 0.76 | 1.11 | 1.23 | 1.33 | 1.36 | 1.74 | 1.99 | 2.15 | 1.98 | ns |
| HSTL_II_DCI_18_S | 0.70 | 0.72 | 0.82 | 0.76 | 1.05 | 1.16 | 1.24 | 1.32 | 1.69 | 1.92 | 2.06 | 1.93 | ns |
| HSTL_II _T_DCI_18_S | 0.70 | 0.72 | 0.82 | 0.76 | 1.11 | 1.23 | 1.33 | 1.36 | 1.74 | 1.99 | 2.15 | 1.98 | ns |
| DIFF_HSTL_I_S | 0.75 | 0.79 | 0.92 | 0.89 | 1.15 | 1.28 | 1.38 | 1.47 | 1.79 | 2.03 | 2.20 | 2.08 | ns |
| DIFF_HSTL_II_S | 0.75 | 0.79 | 0.92 | 0.89 | 1.05 | 1.17 | 1.26 | 1.47 | 1.69 | 1.93 | 2.08 | 2.08 | ns |
| DIFF_HSTL_I_DCI_S | 0.75 | 0.79 | 0.92 | 0.76 | 1.15 | 1.28 | 1.38 | 1.47 | 1.78 | 2.03 | 2.20 | 2.08 | ns |
| DIFF_HSTL_II_DCI_S | 0.75 | 0.79 | 0.92 | 0.76 | 1.05 | 1.17 | 1.26 | 1.40 | 1.69 | 1.93 | 2.08 | 2.01 | ns |
| DIFF_HSTL_I_18_S | 0.75 | 0.79 | 0.92 | 0.89 | 1.12 | 1.24 | 1.34 | 1.46 | 1.75 | 2.00 | 2.16 | 2.07 | ns |
| DIFF_HSTL_II_18_S | 0.75 | 0.79 | 0.92 | 0.89 | 1.06 | 1.18 | 1.26 | 1.47 | 1.70 | 1.94 | 2.08 | 2.08 | ns |
| DIFF_HSTL_I_DCI_18_S | 0.75 | 0.79 | 0.92 | 0.75 | 1.11 | 1.23 | 1.33 | 1.46 | 1.74 | 1.99 | 2.15 | 2.07 | ns |
| DIFF_HSTL_II_DCI_18_S | 0.75 | 0.79 | 0.92 | 0.75 | 1.05 | 1.16 | 1.24 | 1.41 | 1.69 | 1.92 | 2.06 | 2.02 | ns |
| DIFF_HSTL_II _T_DCI_18_S | 0.75 | 0.79 | 0.92 | 0.76 | 1.11 | 1.23 | 1.33 | 1.46 | 1.74 | 1.99 | 2.15 | 2.07 | ns |
| HSTL_I_F | 0.68 | 0.72 | 0.82 | 0.84 | 1.02 | 1.14 | 1.22 | 1.26 | 1.66 | 1.90 | 2.04 | 1.87 | ns |
| HSTL_II_F | 0.68 | 0.72 | 0.82 | 0.84 | 0.97 | 1.08 | 1.15 | 1.29 | 1.61 | 1.84 | 1.97 | 1.90 | ns |
| HSTL_I_18_F | 0.70 | 0.72 | 0.82 | 0.86 | 1.04 | 1.16 | 1.24 | 1.32 | 1.68 | 1.91 | 2.06 | 1.93 | ns |
| HSTL_II_18_F | 0.70 | 0.72 | 0.82 | 0.86 | 0.98 | 1.09 | 1.16 | 1.35 | 1.62 | 1.85 | 1.98 | 1.96 | ns |
| HSTL_I_12_F | 0.68 | 0.72 | 0.82 | 0.94 | 1.02 | 1.13 | 1.21 | 1.26 | 1.65 | 1.88 | 2.03 | 1.87 | ns |
| HSTL_I_DCI_F | 0.68 | 0.72 | 0.82 | 0.78 | 1.04 | 1.16 | 1.24 | 1.30 | 1.67 | 1.91 | 2.06 | 1.91 | ns |
| HSTL_II_DCI_F | 0.68 | 0.72 | 0.82 | 0.78 | 0.97 | 1.08 | 1.15 | 1.22 | 1.61 | 1.84 | 1.97 | 1.83 | ns |
| HSTL_II_T_DCI_F | 0.70 | 0.72 | 0.82 | 0.76 | 1.02 | 1.14 | 1.22 | 1.26 | 1.66 | 1.90 | 2.04 | 1.87 | ns |
| HSTL_I_DCI_18_F | 0.70 | 0.72 | 0.82 | 0.76 | 1.04 | 1.16 | 1.24 | 1.30 | 1.67 | 1.91 | 2.06 | 1.91 | ns |
| HSTL_II_DCI_18_F | 0.70 | 0.72 | 0.82 | 0.76 | 0.98 | 1.09 | 1.16 | 1.27 | 1.61 | 1.85 | 1.98 | 1.88 | ns |
| HSTL_II _T_DCI_18_F | 0.70 | 0.72 | 0.82 | 0.76 | 1.04 | 1.16 | 1.24 | 1.30 | 1.67 | 1.91 | 2.06 | 1.91 | ns |
| DIFF_HSTL_I_F | 0.75 | 0.79 | 0.92 | 0.89 | 1.02 | 1.14 | 1.22 | 1.35 | 1.66 | 1.90 | 2.04 | 1.96 | ns |
| DIFF_HSTL_II_F | 0.75 | 0.79 | 0.92 | 0.89 | 0.97 | 1.08 | 1.15 | 1.35 | 1.61 | 1.84 | 1.97 | 1.96 | ns |
| DIFF_HSTL_I_DCI_F | 0.75 | 0.79 | 0.92 | 0.76 | 1.02 | 1.14 | 1.22 | 1.35 | 1.66 | 1.90 | 2.04 | 1.96 | ns |

## Input/Output Logic Switching Characteristics

*Table 22:* **ILOGIC Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Setup/Hold** | | | | | | |
| $T_{ICE1CK}/T_{ICKCE1}$ | CE1 pin Setup/Hold with respect to CLK | 0.42/0.00 | 0.48/0.00 | 0.67/0.00 | 0.56/–0.16 | ns |
| $T_{ISRCK}/T_{ICKSR}$ | SR pin Setup/Hold with respect to CLK | 0.53/0.01 | 0.61/0.01 | 0.99/0.01 | 0.88/–0.30 | ns |
| $T_{IDOCKE2}/T_{IOCKDE2}$ | D pin Setup/Hold with respect to CLK without Delay (HP I/O banks only) | 0.01/0.27 | 0.01/0.29 | 0.01/0.34 | 0.01/0.41 | ns |
| $T_{IDOCKDE2}/T_{IOCKDDE2}$ | DDLY pin Setup/Hold with respect to CLK (using IDELAY) (HP I/O banks only) | 0.01/0.27 | 0.02/0.29 | 0.02/0.34 | 0.01/0.41 | ns |
| $T_{IDOCKE3}/T_{IOCKDE3}$ | D pin Setup/Hold with respect to CLK without Delay (HR I/O banks only) | 0.01/0.27 | 0.01/0.29 | 0.01/0.34 | 0.01/0.41 | ns |
| $T_{IDOCKDE3}/T_{IOCKDDE3}$ | DDLY pin Setup/Hold with respect to CLK (using IDELAY) (HR I/O banks only) | 0.01/0.27 | 0.02/0.29 | 0.02/0.34 | 0.01/0.41 | ns |
| **Combinatorial** | | | | | | |
| $T_{IDIE2}$ | D pin to O pin propagation delay, no Delay (HP I/O banks only) | 0.09 | 0.10 | 0.12 | 0.14 | ns |
| $T_{IDIDE2}$ | DDLY pin to O pin propagation delay (using IDELAY) (HP I/O banks only) | 0.10 | 0.11 | 0.13 | 0.15 | ns |
| $T_{IDIE3}$ | D pin to O pin propagation delay, no Delay (HR I/O banks only) | 0.09 | 0.10 | 0.12 | 0.14 | ns |
| $T_{IDIDE3}$ | DDLY pin to O pin propagation delay (using IDELAY) (HR I/O banks only) | 0.10 | 0.11 | 0.13 | 0.15 | ns |
| **Sequential Delays** | | | | | | |
| $T_{IDLOE2}$ | D pin to Q1 pin using flip-flop as a latch without Delay (HP I/O banks only) | 0.36 | 0.39 | 0.45 | 0.54 | ns |
| $T_{IDLODE2}$ | DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) (HP I/O banks only) | 0.36 | 0.39 | 0.45 | 0.55 | ns |
| $T_{IDLOE3}$ | D pin to Q1 pin using flip-flop as a latch without Delay (HR I/O banks only) | 0.36 | 0.39 | 0.45 | 0.54 | ns |
| $T_{IDLODE3}$ | DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) (HR I/O banks only) | 0.36 | 0.39 | 0.45 | 0.55 | ns |
| $T_{ICKQ}$ | CLK to Q outputs | 0.47 | 0.50 | 0.58 | 0.71 | ns |
| $T_{RQ\_ILOGICE2}$ | SR pin to OQ/TQ out (HP I/O banks only) | 0.84 | 0.94 | 1.16 | 1.32 | ns |
| $T_{GSRQ\_ILOGICE2}$ | Global Set/Reset to Q outputs (HP I/O banks only) | 7.60 | 7.60 | 10.51 | 11.39 | ns |
| $T_{RQ\_ILOGICE3}$ | SR pin to OQ/TQ out (HR I/O banks only) | 0.84 | 0.94 | 1.16 | 1.32 | ns |
| $T_{GSRQ\_ILOGICE3}$ | Global Set/Reset to Q outputs (HR I/O banks only) | 7.60 | 7.60 | 10.51 | 11.39 | ns |
| **Set/Reset** | | | | | | |
| $T_{RPW\_ILOGICE2}$ | Minimum Pulse Width, SR inputs (HP I/O banks only) | 0.54 | 0.63 | 0.63 | 0.68 | ns, Min |
| $T_{RPW\_ILOGICE3}$ | Minimum Pulse Width, SR inputs (HR I/O banks only) | 0.54 | 0.63 | 0.63 | 0.68 | ns, Min |

*Table 23:* **OLOGIC Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Setup/Hold** | | | | | | |
| $T_{ODCK}/T_{OCKD}$ | D1/D2 pins Setup/Hold with respect to CLK | 0.45/–0.13 | 0.50/–0.13 | 0.58/–0.13 | 0.79/–0.18 | ns |
| $T_{OOCECK}/T_{OCKOCE}$ | OCE pin Setup/Hold with respect to CLK | 0.28/0.03 | 0.29/0.03 | 0.45/0.03 | 0.35/–0.10 | ns |
| $T_{OSRCK}/T_{OCKSR}$ | SR pin Setup/Hold with respect to CLK | 0.32/0.18 | 0.38/0.18 | 0.70/0.18 | 0.62/–0.04 | ns |
| $T_{OTCK}/T_{OCKT}$ | T1/T2 pins Setup/Hold with respect to CLK | 0.49/–0.16 | 0.56/–0.16 | 0.68/–0.16 | 0.67/–0.18 | ns |
| $T_{OTCECK}/T_{OCKTCE}$ | TCE pin Setup/Hold with respect to CLK | 0.28/0.01 | 0.30/0.01 | 0.45/0.01 | 0.31/–0.10 | ns |
| **Combinatorial** | | | | | | |
| $T_{ODQ}$ | D1 to OQ out or T1 to TQ out | 0.73 | 0.81 | 0.97 | 1.18 | ns |
| **Sequential Delays** | | | | | | |
| $T_{OCKQ}$ | CLK to OQ/TQ out | 0.41 | 0.43 | 0.49 | 0.63 | ns |
| $T_{RQ\_OLOGICE2}$ | SR pin to OQ/TQ out (HP I/O banks only) | 0.63 | 0.70 | 0.83 | 1.12 | ns |
| $T_{GSRQ\_OLOGICE2}$ | Global Set/Reset to Q outputs (HP I/O banks only) | 7.60 | 7.60 | 10.51 | 11.39 | ns |
| $T_{RQ\_OLOGICE3}$ | SR pin to OQ/TQ out (HR I/O banks only) | 0.63 | 0.70 | 0.83 | 1.12 | ns |
| $T_{GSRQ\_OLOGICE3}$ | Global Set/Reset to Q outputs (HR I/O banks only) | 7.60 | 7.60 | 10.51 | 11.39 | ns |
| **Set/Reset** | | | | | | |
| $T_{RPW\_OLOGICE2}$ | Minimum Pulse Width, SR inputs (HP I/O banks only) | 0.54 | 0.54 | 0.63 | 0.68 | ns, Min |
| $T_{RPW\_OLOGICE3}$ | Minimum Pulse Width, SR inputs (HR I/O banks only) | 0.54 | 0.54 | 0.63 | 0.68 | ns, Min |

## Input Serializer/Deserializer Switching Characteristics

*Table 24:* **ISERDES Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Setup/Hold for Control Lines** | | | | | | |
| $T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$ | BITSLIP pin Setup/Hold with respect to CLKDIV | 0.01/0.12 | 0.02/0.13 | 0.02/0.15 | 0.02/0.21 | ns |
| $T_{ISCCK\_CE}$/ $T_{ISCKC\_CE}$(2) | CE pin Setup/Hold with respect to CLK (for CE1) | 0.39/–0.02 | 0.44/–0.02 | 0.63/–0.02 | 0.51/–0.22 | ns |
| $T_{ISCCK\_CE2}$/ $T_{ISCKC\_CE2}$(2) | CE pin Setup/Hold with respect to CLKDIV (for CE2) | –0.12/0.29 | –0.12/0.31 | –0.12/0.35 | –0.17/0.40 | ns |
| **Setup/Hold for Data Lines** | | | | | | |
| $T_{ISDCK\_D}$/$T_{ISCKD\_D}$ | D pin Setup/Hold with respect to CLK | –0.02/0.11 | –0.02/0.12 | –0.02/0.15 | –0.04/0.19 | ns |
| $T_{ISDCK\_DDLY}$/ $T_{ISCKD\_DDLY}$ | DDLY pin Setup/Hold with respect to CLK (using IDELAY)(1) | –0.02/0.11 | –0.02/0.12 | –0.02/0.15 | –0.03/0.19 | ns |
| $T_{ISDCK\_D\_DDR}$/ $T_{ISCKD\_D\_DDR}$ | D pin Setup/Hold with respect to CLK at DDR mode | –0.02/0.11 | –0.02/0.12 | –0.02/0.15 | –0.04/0.19 | ns |
| $T_{ISDCK\_DDLY\_DDR}$/ $T_{ISCKD\_DDLY\_DDR}$ | D pin Setup/Hold with respect to CLK at DDR mode (using IDELAY)(1) | 0.11/0.11 | 0.12/0.12 | 0.15/0.15 | 0.19/0.19 | ns |
| **Sequential Delays** | | | | | | |
| $T_{ISCKO\_Q}$ | CLKDIV to out at Q pin | 0.46 | 0.47 | 0.58 | 0.67 | ns |
| **Propagation Delays** | | | | | | |
| $T_{ISDO\_DO}$ | D input to DO output pin | 0.09 | 0.10 | 0.12 | 0.14 | ns |

**Notes:**

1. Recorded at 0 tap value.
2. $T_{ISCCK\_CE2}$ and $T_{ISCKC\_CE2}$ are reported as $T_{ISCCK\_CE}$/$T_{ISCKC\_CE}$ in TRACE report.

## CLB Distributed RAM Switching Characteristics (SLICEM Only)

*Table 29:* **CLB Distributed RAM Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Sequential Delays** | | | | | | |
| $T_{SHCKO}$ | Clock to A – B outputs | 0.68 | 0.70 | 0.85 | 1.08 | ns, Max |
| $T_{SHCKO\_1}$ | Clock to AMUX – BMUX outputs | 0.91 | 0.95 | 1.15 | 1.44 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | | |
| $T_{DS\_LRAM}/T_{DH\_LRAM}$ | A – D inputs to CLK | 0.45/0.23 | 0.45/0.24 | 0.54/0.27 | 0.69/0.33 | ns, Min |
| $T_{AS\_LRAM}/T_{AH\_LRAM}$ | Address An inputs to clock | 0.13/0.50 | 0.14/0.50 | 0.17/0.58 | 0.21/0.63 | ns, Min |
| | Address An inputs through MUXs and/or carry logic to clock | 0.40/0.16 | 0.42/0.17 | 0.52/0.23 | 0.63/0.23 | ns, Min |
| $T_{WS\_LRAM}/T_{WH\_LRAM}$ | WE input to clock | 0.29/0.09 | 0.30/0.09 | 0.36/0.09 | 0.46/0.10 | ns, Min |
| $T_{CECK\_LRAM}$/ $T_{CKCE\_LRAM}$ | CE input to CLK | 0.29/0.09 | 0.30/0.09 | 0.37/0.09 | 0.47/0.10 | ns, Min |
| **Clock CLK** | | | | | | |
| $T_{MPW}$ | Minimum pulse width | 0.68 | 0.77 | 0.91 | 1.11 | ns, Min |
| $T_{MCP}$ | Minimum clock period | 1.35 | 1.54 | 1.82 | 2.22 | ns, Min |

**Notes:**

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time.
2. $T_{SHCKO}$ also represents the CLK to XMUX output. Refer to TRACE report for the CLK to XMUX path.

## CLB Shift Register Switching Characteristics (SLICEM Only)

*Table 30:* **CLB Shift Register Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Sequential Delays** | | | | | | |
| $T_{REG}$ | Clock to A – D outputs | 0.96 | 0.98 | 1.20 | 1.35 | ns, Max |
| $T_{REG\_MUX}$ | Clock to AMUX – DMUX output | 1.19 | 1.23 | 1.50 | 1.72 | ns, Max |
| $T_{REG\_M31}$ | Clock to DMUX output via M31 output | 0.89 | 0.91 | 1.10 | 1.25 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | | |
| $T_{WS\_SHFREG}$/ $T_{WH\_SHFREG}$ | WE input | 0.26/0.09 | 0.27/0.09 | 0.33/0.09 | 0.41/0.10 | ns, Min |
| $T_{CECK\_SHFREG}$/ $T_{CKCE\_SHFREG}$ | CE input to CLK | 0.27/0.09 | 0.28/0.09 | 0.33/0.09 | 0.42/0.10 | ns, Min |
| $T_{DS\_SHFREG}$/ $T_{DH\_SHFREG}$ | A – D inputs to CLK | 0.28/0.26 | 0.28/0.26 | 0.33/0.30 | 0.41/0.36 | ns, Min |
| **Clock CLK** | | | | | | |
| $T_{MPW\_SHFREG}$ | Minimum pulse width | 0.55 | 0.65 | 0.78 | 0.91 | ns, Min |

**Notes:**

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time.

*Table 31:* **Block RAM and FIFO Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $T_{RCCK\_RSTRAM}/T_{RCKC\_RSTRAM}$ | Synchronous RSTRAM input | 0.27/0.35 | 0.29/0.37 | 0.31/0.39 | 0.34/0.40 | ns, Min |
| $T_{RCCK\_WEA}/T_{RCKC\_WEA}$ | Write Enable (WE) input (Block RAM only) | 0.38/0.15 | 0.41/0.16 | 0.46/0.17 | 0.54/0.19 | ns, Min |
| $T_{RCCK\_WREN}/T_{RCKC\_WREN}$ | WREN FIFO inputs | 0.39/0.25 | 0.39/0.30 | 0.40/0.37 | 0.65/0.37 | ns, Min |
| $T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$ | RDEN FIFO inputs | 0.36/0.26 | 0.36/0.30 | 0.37/0.37 | 0.60/0.38 | ns, Min |
| **Reset Delays** | | | | | | |
| $T_{RCO\_FLAGS}$ | Reset RST to FIFO flags/pointers(10) | 0.76 | 0.83 | 0.93 | 1.06 | ns, Max |
| $T_{RREC\_RST}/T_{RREM\_RST}$ | FIFO reset recovery and removal timing(11) | 1.59/–0.68 | 1.76/–0.68 | 2.01/–0.68 | 2.07/–0.60 | ns, Max |
| **Maximum Frequency** | | | | | | |
| $F_{MAX\_BRAM\_WF\_NC}$ | Block RAM<br>(Write first and No change modes)<br>When not in SDP RF mode | 601.32 | 543.77 | 458.09 | 372.44 | MHz |
| $F_{MAX\_BRAM\_RF\_PERFORMANCE}$ | Block RAM<br>(Read first, Performance mode)<br>When in SDP RF mode but no address overlap between port A and port B | 601.32 | 543.77 | 458.09 | 372.44 | MHz |
| $F_{MAX\_BRAM\_RF\_DELAYED\_WRITE}$ | Block RAM<br>(Read first, Delayed_write mode)<br>When in SDP RF mode and there is possibility of overlap between port A and port B addresses | 528.26 | 477.33 | 400.80 | 317.36 | MHz |
| $F_{MAX\_CAS\_WF\_NC}$ | Block RAM Cascade<br>(Write first, No change mode)<br>When cascade but not in RF mode | 551.27 | 493.83 | 408.00 | 322.48 | MHz |
| $F_{MAX\_CAS\_RF\_PERFORMANCE}$ | Block RAM Cascade<br>(Read first, Performance mode)<br>When in cascade with RF mode and no possibility of address overlap/one port is disabled | 551.27 | 493.83 | 408.00 | 322.48 | MHz |
| $F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$ | When in cascade RF mode and there is a possibility of address overlap between port A and port B | 478.27 | 427.35 | 350.88 | 267.38 | MHz |
| $F_{MAX\_FIFO}$ | FIFO in all modes without ECC | 601.32 | 543.77 | 458.09 | 372.44 | MHz |
| $F_{MAX\_ECC}$ | Block RAM and FIFO in ECC configuration | 484.26 | 430.85 | 351.12 | 254.13 | MHz |

**Notes:**

1. TRACE will report all of these parameters as $T_{RCKO\_DO}$.
2. $T_{RCKO\_DOR}$ includes $T_{RCKO\_DOW}$, $T_{RCKO\_DOPR}$, and $T_{RCKO\_DOPW}$ as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. $T_{RCKO\_DO}$ includes $T_{RCKO\_DOP}$ as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. $T_{RCKO\_FLAGS}$ includes the following parameters: $T_{RCKO\_AEMPTY}$, $T_{RCKO\_AFULL}$, $T_{RCKO\_EMPTY}$, $T_{RCKO\_FULL}$, $T_{RCKO\_RDERR}$, $T_{RCKO\_WRERR}$.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. These parameters include both A and B inputs as well as the parity inputs of A and B.
10. $T_{RCO\_FLAGS}$ includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

*Table 32:* **DSP48E1 Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| **Clock to Outs from Pipeline Register Clock to Output Pins** | | | | | | |
| $T_{DSPCKO\_P\_MREG}$ | CLK MREG to P output | 1.42 | 1.64 | 1.96 | 2.31 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_MREG}$ | CLK MREG to CARRYCASCOUT output | 1.63 | 1.87 | 2.24 | 2.65 | ns |
| $T_{DSPCKO\_P\_ADREG\_MULT}$ | CLK ADREG to P output using multiplier | 2.30 | 2.63 | 3.13 | 3.90 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_ADREG\_MULT}$ | CLK ADREG to CARRYCASCOUT output using multiplier | 2.51 | 2.87 | 3.41 | 4.23 | ns |
| **Clock to Outs from Input Register Clock to Output Pins** | | | | | | |
| $T_{DSPCKO\_P\_AREG\_MULT}$ | CLK AREG to P output using multiplier | 3.34 | 3.83 | 4.55 | 5.80 | ns |
| $T_{DSPCKO\_P\_BREG}$ | CLK BREG to P output not using multiplier | 1.39 | 1.59 | 1.88 | 2.24 | ns |
| $T_{DSPCKO\_P\_CREG}$ | CLK CREG to P output not using multiplier | 1.43 | 1.64 | 1.95 | 2.32 | ns |
| $T_{DSPCKO\_P\_DREG\_MULT}$ | CLK DREG to P output using multiplier | 3.32 | 3.80 | 4.51 | 5.74 | ns |
| **Clock to Outs from Input Register Clock to Cascading Output Pins** | | | | | | |
| $T_{DSPCKO\_\{ACOUT;\ BCOUT\}\_\{AREG;\ BREG\}}$ | CLK (ACOUT, BCOUT) to {A,B} register output | 0.55 | 0.62 | 0.74 | 0.87 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\{AREG,\ BREG\}\_MULT}$ | CLK (AREG, BREG) to CARRYCASCOUT output using multiplier | 3.55 | 4.06 | 4.84 | 6.13 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\ BREG}$ | CLK BREG to CARRYCASCOUT output not using multiplier | 1.60 | 1.82 | 2.16 | 2.58 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\ DREG\_MULT}$ | CLK DREG to CARRYCASCOUT output using multiplier | 3.52 | 4.03 | 4.79 | 6.07 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\ CREG}$ | CLK CREG to CARRYCASCOUT output | 1.64 | 1.88 | 2.23 | 2.65 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX}$ | With all registers used | 741.84 | 650.20 | 547.95 | 429.37 | MHz |
| $F_{MAX\_PATDET}$ | With pattern detector | 627.35 | 549.75 | 463.61 | 365.90 | MHz |
| $F_{MAX\_MULT\_NOMREG}$ | Two register multiply without MREG | 412.20 | 360.75 | 303.77 | 248.32 | MHz |
| $F_{MAX\_MULT\_NOMREG\_PATDET}$ | Two register multiply without MREG with pattern detect | 374.25 | 327.65 | 276.01 | 225.73 | MHz |
| $F_{MAX\_PREADD\_MULT\_NOADREG}$ | Without ADREG | 468.82 | 408.66 | 342.70 | 263.44 | MHz |
| $F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$ | Without ADREG with pattern detect | 468.82 | 408.66 | 342.70 | 263.44 | MHz |
| $F_{MAX\_NOPIPELINEREG}$ | Without pipeline registers (MREG, ADREG) | 306.84 | 267.81 | 225.02 | 177.15 | MHz |
| $F_{MAX\_NOPIPELINEREG\_PATDET}$ | Without pipeline registers (MREG, ADREG) with pattern detect | 285.23 | 249.13 | 209.38 | 165.32 | MHz |

## MMCM Switching Characteristics

*Table 38:* **MMCM Specification**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $MMCM\_F_{INMAX}$ | Maximum Input Clock Frequency | 1066.00 | 933.00 | 800.00 | 800.00 | MHz |
| $MMCM\_F_{INMIN}$ | Minimum Input Clock Frequency | 10.00 | 10.00 | 10.00 | 10.00 | MHz |
| $MMCM\_F_{INJITTER}$ | Maximum Input Clock Period Jitter | < 20% of clock input period or 1 ns Max | | | | |
| $MMCM\_F_{INDUTY}$ | Allowable Input Duty Cycle: 10—49 MHz | 25.00 | 25.00 | 25.00 | 25.00 | % |
| | Allowable Input Duty Cycle: 50—199 MHz | 30.00 | 30.00 | 30.00 | 30.00 | % |
| | Allowable Input Duty Cycle: 200—399 MHz | 35.00 | 35.00 | 35.00 | 35.00 | % |
| | Allowable Input Duty Cycle: 400—499 MHz | 40.00 | 40.00 | 40.00 | 40.00 | % |
| | Allowable Input Duty Cycle: >500 MHz | 45.00 | 45.00 | 45.00 | 45.00 | % |
| $MMCM\_F_{MIN\_PSCLK}$ | Minimum Dynamic Phase Shift Clock Frequency | 0.01 | 0.01 | 0.01 | 0.01 | MHz |
| $MMCM\_F_{MAX\_PSCLK}$ | Maximum Dynamic Phase Shift Clock Frequency | 550.00 | 500.00 | 450.00 | 450.00 | MHz |
| $MMCM\_F_{VCOMIN}$ | Minimum MMCM VCO Frequency | 600.00 | 600.00 | 600.00 | 600.00 | MHz |
| $MMCM\_F_{VCOMAX}$ | Maximum MMCM VCO Frequency | 1600.00 | 1440.00 | 1200.00 | 1200.00 | MHz |
| $MMCM\_F_{BANDWIDTH}$ | Low MMCM Bandwidth at Typical(1) | 1.00 | 1.00 | 1.00 | 1.00 | MHz |
| | High MMCM Bandwidth at Typical(1) | 4.00 | 4.00 | 4.00 | 4.00 | MHz |
| $MMCM\_T_{STATPHAOFFSET}$ | Static Phase Offset of the MMCM Outputs(2) | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| $MMCM\_T_{OUTJITTER}$ | MMCM Output Jitter | Note 3 | | | | |
| $MMCM\_T_{OUTDUTY}$ | MMCM Output Clock Duty Cycle Precision(4) | 0.20 | 0.20 | 0.20 | 0.25 | ns |
| $MMCM\_T_{LOCKMAX}$ | MMCM Maximum Lock Time | 100.00 | 100.00 | 100.00 | 100.00 | µs |
| $MMCM\_F_{OUTMAX}$ | MMCM Maximum Output Frequency | 1066.00 | 933.00 | 800.00 | 800.00 | MHz |
| $MMCM\_F_{OUTMIN}$ | MMCM Minimum Output Frequency(5)(6) | 4.69 | 4.69 | 4.69 | 4.69 | MHz |
| $MMCM\_T_{EXTFDVAR}$ | External Clock Feedback Variation | < 20% of clock input period or 1 ns Max | | | | |
| $MMCM\_RST_{MINPULSE}$ | Minimum Reset Pulse Width | 5.00 | 5.00 | 5.00 | 5.00 | ns |
| $MMCM\_F_{PFDMAX}$ | Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized | 550.00 | 500.00 | 450.00 | 450.00 | MHz |
| | Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low | 300.00 | 300.00 | 300.00 | 300.00 | MHz |
| $MMCM\_F_{PFDMIN}$ | Minimum Frequency at the Phase Frequency Detector | 10.00 | 10.00 | 10.00 | 10.00 | MHz |
| $MMCM\_T_{FBDELAY}$ | Maximum Delay in the Feedback Path | 3 ns Max or one CLKIN cycle | | | | |
| **MMCM Switching Characteristics Setup and Hold** | | | | | | |
| $T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$ | Setup and Hold of Phase Shift Enable | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |
| $T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$ | Setup and Hold of Phase Shift Increment/Decrement | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |
| $T_{MMCMCKO\_PSDONE}$ | Phase Shift Clock-to-Out of PSDONE | 0.59 | 0.68 | 0.81 | 0.78 | ns |
| **Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK** | | | | | | |
| $T_{MMCMDCK\_DADDR}$/ $T_{MMCMCKD\_DADDR}$ | DADDR Setup/Hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{MMCMDCK\_DI}$/ $T_{MMCMCKD\_DI}$ | DI Setup/Hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |

*Table 39:* **PLL Specification *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| PLL_$F_{PFDMAX}$ | Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized | 550.00 | 500.00 | 450.00 | 450.00 | MHz |
| | Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low | 300.00 | 300.00 | 300.00 | 300.00 | MHz |
| PLL_$F_{PFDMIN}$ | Minimum Frequency at the Phase Frequency Detector | 19.00 | 19.00 | 19.00 | 19.00 | MHz |
| PLL_$T_{FBDELAY}$ | Maximum Delay in the Feedback Path | 3 ns Max or one CLKIN cycle | | | | |
| **Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK** | | | | | | |
| $T_{PLLCCK\_DADDR}$/ $T_{PLLCKC\_DADDR}$ | Setup and hold of D address | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{PLLCCK\_DI}$/ $T_{PLLCKC\_DI}$ | Setup and hold of D input | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{PLLCCK\_DEN}$/ $T_{PLLCKC\_DEN}$ | Setup and hold of D enable | 1.76/0.00 | 1.97/0.00 | 2.29/0.00 | 2.40/0.00 | ns, Min |
| $T_{PLLCCK\_DWE}$/ $T_{PLLCKC\_DWE}$ | Setup and hold of D write enable | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{PLLCKO\_DRDY}$ | CLK to out of DRDY | 0.65 | 0.72 | 0.99 | 0.70 | ns, Max |
| $F_{DCK}$ | DCLK frequency | 200.00 | 200.00 | 200.00 | 100.00 | MHz, Max |

**Notes:**

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}$/128 assuming output duty cycle is 50%.

## Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

*Table 45:* **Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1) | | | | | | | |
| $T_{PSFD}$/ $T_{PHFD}$ | Full Delay (Legacy Delay or Default Delay) Global Clock Input and IFF(2) without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks | XC7K70T | 2.83/–0.29 | 2.95/–0.29 | 3.15/–0.29 | 4.96/–0.33 | ns |
| | | XC7K160T | 3.17/–0.35 | 3.29/–0.35 | 3.55/–0.35 | 5.54/–0.49 | ns |
| | | XC7K325T | 2.83/–0.06 | 2.94/–0.06 | 3.15/–0.06 | 5.18/–0.14 | ns |
| | | XC7K355T | 3.26/–0.32 | 3.41/–0.32 | 3.67/–0.32 | 5.84/–0.49 | ns |
| | | XC7K410T | 3.43/–0.34 | 3.59/–0.34 | 3.88/–0.34 | 6.21/–0.54 | ns |
| | | XC7K420T | 3.37/–0.27 | 3.48/–0.27 | 3.76/–0.27 | 6.00/–0.52 | ns |
| | | XC7K480T | 3.37/–0.27 | 3.48/–0.27 | 3.76/–0.27 | 6.00/–0.52 | ns |

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time.

*Table 46:* **Clock-Capable Clock Input Setup and Hold With MMCM**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3 | -2/-2L | -1 | -2L | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1) | | | | | | | |
| $T_{PSMMCMCC}$/ $T_{PHMMCMCC}$ | No Delay clock-capable clock input and IFF(2) with MMCM | XC7K70T | 2.39/–0.22 | 2.65/–0.22 | 2.94/–0.22 | 2.21/–0.44 | ns |
| | | XC7K160T | 2.49/–0.20 | 2.77/–0.20 | 3.07/–0.20 | 2.38/–0.47 | ns |
| | | XC7K325T | 2.55/–0.16 | 2.85/–0.16 | 3.14/–0.16 | 2.60/–0.47 | ns |
| | | XC7K355T | 2.43/–0.16 | 2.73/–0.16 | 3.00/–0.16 | 2.47/–0.43 | ns |
| | | XC7K410T | 2.55/–0.16 | 2.84/–0.16 | 3.14/–0.16 | 2.58/–0.47 | ns |
| | | XC7K420T | 2.47/–0.09 | 2.73/–0.09 | 3.02/–0.09 | 2.40/–0.41 | ns |
| | | XC7K480T | 2.47/–0.09 | 2.73/–0.09 | 3.02/–0.09 | 2.40/–0.41 | ns |

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

# GTX Transceiver Specifications

## GTX Transceiver DC Input and Output Levels

Table 51 summarizes the DC output specifications of the GTX transceivers in Kintex-7 FPGAs. Consult UG476: *7 Series FPGAs GTX/GTH Transceiver User Guide* for further details.

*Table 51:* **GTX Transceiver DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $DV_{PPOUT}$ | Differential peak-to-peak output voltage(1) | Transmitter output swing is set to maximum setting | – | – | 1000 | mV |
| $V_{CMOUTDC}$ | DC common mode output voltage. | Equation based | $V_{MGTAVTT} - DV_{PPOUT}/4$ | | | mV |
| $R_{OUT}$ | Differential output resistance | | – | 100 | – | Ω |
| $T_{OSKEW}$ | Transmitter output pair (TXP and TXN) intra-pair skew | | – | 2 | 12 | ps |
| $DV_{PPIN}$ | Differential peak-to-peak input voltage (external AC coupled) | >10.3125 Gb/s | 150 | – | 1250 | mV |
| | | 6.6 Gb/s to 10.3125 Gb/s | 150 | – | 1250 | mV |
| | | ≤ 6.6 Gb/s | 150 | – | 2000 | mV |
| $V_{IN}$ | Absolute input voltage | DC coupled $V_{MGTAVTT}$ = 1.2V | –200 | – | $V_{MGTAVTT}$ | mV |
| $V_{CMIN}$ | Common mode input voltage | DC coupled $V_{MGTAVTT}$ = 1.2V | – | 2/3 $V_{MGTAVTT}$ | – | mV |
| $R_{IN}$ | Differential input resistance | | – | 100 | – | Ω |
| $C_{EXT}$ | Recommended external AC coupling capacitor(2) | | – | 100 | – | nF |

**Notes:**

1. The output swing and preemphasis levels are programmable using the attributes discussed in UG476: *7 Series FPGAs GTX/GTH Transceiver User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

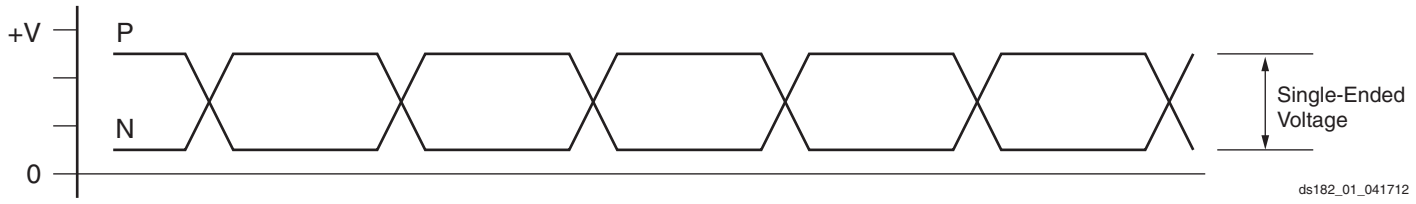


*Figure 1:* **Single-Ended Peak-to-Peak Voltage**

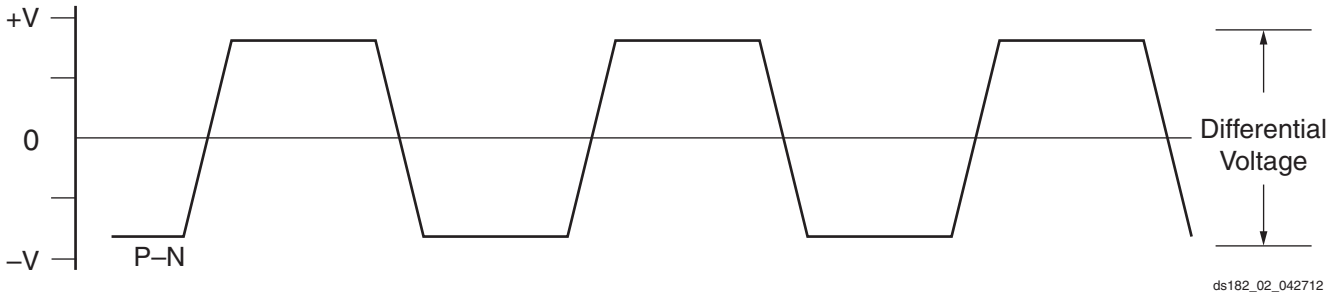


*Figure 2:* **Differential Peak-to-Peak Voltage**

*Table 56:* **GTX Transceiver PLL /Lock Time Adaptation**

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $T_{LOCK}$ | Initial PLL lock | | – | – | 1 | ms |
| $T_{DLOCK}$ | Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE). | After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input. | – | 50,000 | 37 x$10^6$ | UI |
| | Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled. | | – | 50,000 | 2.3 x$10^6$ | UI |

*Table 57:* **GTX Transceiver User Clock Switching Characteristics(1)(2)**

| Symbol | Description | Conditions | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.9V | |
| | | | -3(3) | -2/-2L(3) | -1(4) | -2L(5) | |
| $F_{TXOUT}$ | TXOUTCLK maximum frequency | | 412.54 | 412.54 | 312.50 | 237.53 | MHz |
| $F_{RXOUT}$ | RXOUTCLK maximum frequency | | 412.54 | 412.54 | 312.50 | 237.53 | MHz |
| $F_{TXIN}$ | TXUSRCLK maximum frequency | 16-bit data path | 412.54 | 412.54 | 312.50 | 237.53 | MHz |
| | | 32-bit data path | 391.08 | 322.37 | 250.00 | 206.27 | MHz |
| $F_{RXIN}$ | RXUSRCLK maximum frequency | 16-bit data path | 412.54 | 412.54 | 312.50 | 237.53 | MHz |
| | | 32-bit data path | 391.08 | 322.37 | 250.00 | 206.27 | MHz |
| $F_{TXIN2}$ | TXUSRCLK2 maximum frequency | 16-bit data path | 412.54 | 412.54 | 312.50 | 237.53 | MHz |
| | | 32-bit data path | 391.08 | 322.37 | 250.00 | 206.27 | MHz |
| | | 64-bit data path | 195.54 | 161.19 | 125.00 | 103.14 | MHz |
| $F_{RXIN2}$ | RXUSRCLK2 maximum frequency | 16-bit data path | 412.54 | 412.54 | 312.50 | 237.53 | MHz |
| | | 32-bit data path | 391.08 | 322.37 | 250.00 | 206.27 | MHz |
| | | 64-bit data path | 195.54 | 161.19 | 125.00 | 103.14 | MHz |

**Notes:**

1. Clocking must be implemented as described in UG476: *7 Series FPGAs GTX/GTH Transceiver User Guide*.
2. These frequencies are not supported for all possible transceiver configurations.
3. For speed grades -3, -2, -2L (1.0V), a 16-bit data path can only be used for speeds less than 6.6 Gb/s.
4. For speed grade -1, a 16-bit data path can only be used for speeds less than 5.0 Gb/s.
5. For speed grade -2L (0.9V), a 16-bit data path can only be used for speeds less than 3.8 Gb/s.

*Table 58:* **GTX Transceiver Transmitter Switching Characteristics**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GTXTX}$ | Serial data rate range | | 0.500 | – | $F_{GTXMAX}$ | Gb/s |
| $T_{RTX}$ | TX Rise time | 20%–80% | – | 40 | – | ps |
| $T_{FTX}$ | TX Fall time | 80%–20% | – | 40 | – | ps |
| $T_{LLSKEW}$ | TX lane-to-lane skew(1) | | – | – | 500 | ps |
| $V_{TXOOBVDPP}$ | Electrical idle amplitude | | – | – | 15 | mV |
| $T_{TXOOBTRANSITION}$ | Electrical idle transition time | | – | – | 140 | ns |
| $TJ_{12.5}$ | Total Jitter(2)(4) | 12.5 Gb/s | – | – | 0.28 | UI |
| $DJ_{12.5}$ | Deterministic Jitter(2)(4) | | – | – | 0.17 | UI |
| $TJ_{11.18}$ | Total Jitter(2)(4) | 11.18 Gb/s | – | – | 0.28 | UI |
| $DJ_{11.18}$ | Deterministic Jitter(2)(4) | | – | – | 0.17 | UI |

*Table 59:* **GTX Transceiver Receiver Switching Characteristics**

| Symbol | Description | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GTXRX}$ | Serial data rate | RX oversampler not enabled | 0.500 | – | $F_{GTXMAX}$ | Gb/s |
| $T_{RXELECIDLE}$ | Time for RXELECIDLE to respond to loss or restoration of data | | – | 10 | – | ns |
| $RX_{OOBVDPP}$ | OOB detect threshold peak-to-peak | | 60 | – | 150 | mV |
| $RX_{SST}$ | Receiver spread-spectrum tracking(1) | Modulated @ 33 KHz | –5000 | – | 0 | ppm |
| $RX_{RL}$ | Run length (CID) | | – | – | 512 | UI |
| $RX_{PPMTOL}$ | Data/REFCLK PPM offset tolerance | Bit rates ≤ 6.6 Gb/s | –1250 | – | 1250 | ppm |
| | | Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s | –700 | – | 700 | ppm |
| | | Bit rates > 8.0 Gb/s | –200 | – | 200 | ppm |
| **SJ Jitter Tolerance(2)** | | | | | | |
| $JT\_SJ_{12.5}$ | Sinusoidal Jitter (QPLL)(3) | 12.5 Gb/s | 0.3 | – | – | UI |
| $JT\_SJ_{11.18}$ | Sinusoidal Jitter (QPLL)(3) | 11.18 Gb/s | 0.3 | – | – | UI |
| $JT\_SJ_{10.32}$ | Sinusoidal Jitter (QPLL)(3) | 10.32 Gb/s | 0.3 | – | – | UI |
| $JT\_SJ_{9.95}$ | Sinusoidal Jitter (QPLL)(3) | 9.95 Gb/s | 0.3 | – | – | UI |
| $JT\_SJ_{9.8}$ | Sinusoidal Jitter (QPLL)(3) | 9.8 Gb/s | 0.3 | – | – | UI |
| $JT\_SJ_{8.0}$ | Sinusoidal Jitter (QPLL)(3) | 8.0 Gb/s | 0.44 | – | – | UI |
| $JT\_SJ_{6.6\_QPLL}$ | Sinusoidal Jitter (QPLL)(3) | 6.6 Gb/s | 0.48 | – | – | UI |
| $JT\_SJ_{6.6\_CPLL}$ | Sinusoidal Jitter (CPLL)(3) | 6.6 Gb/s | 0.44 | – | – | UI |
| $JT\_SJ_{5.0}$ | Sinusoidal Jitter (CPLL)(3) | 5.0 Gb/s | 0.44 | – | – | UI |
| $JT\_SJ_{4.25}$ | Sinusoidal Jitter (CPLL)(3) | 4.25 Gb/s | 0.44 | – | – | UI |
| $JT\_SJ_{3.75}$ | Sinusoidal Jitter (CPLL)(3) | 3.75 Gb/s | 0.44 | – | – | UI |
| $JT\_SJ_{3.2}$ | Sinusoidal Jitter (CPLL)(3) | 3.2 Gb/s(4) | 0.45 | – | – | UI |
| $JT\_SJ_{3.2L}$ | Sinusoidal Jitter (CPLL)(3) | 3.2 Gb/s(5) | 0.45 | – | – | UI |
| $JT\_SJ_{2.5}$ | Sinusoidal Jitter (CPLL)(3) | 2.5 Gb/s(6) | 0.5 | – | – | UI |
| $JT\_SJ_{1.25}$ | Sinusoidal Jitter (CPLL)(3) | 1.25 Gb/s(7) | 0.5 | – | – | UI |
| $JT\_SJ_{500}$ | Sinusoidal Jitter (CPLL)(3) | 500 Mb/s | 0.4 | – | – | UI |
| **SJ Jitter Tolerance with Stressed Eye(2)** | | | | | | |
| $JT\_TJSE_{3.2}$ | Total Jitter with Stressed Eye(8) | 3.2 Gb/s | 0.70 | – | – | UI |
| $JT\_TJSE_{6.6}$ | | 6.6 Gb/s | 0.70 | – | – | UI |
| $JT\_SJSE_{3.2}$ | Sinusoidal Jitter with Stressed Eye(8) | 3.2 Gb/s | 0.1 | – | – | UI |
| $JT\_SJSE_{6.6}$ | | 6.6 Gb/s | 0.1 | – | – | UI |

**Notes:**

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 10 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 1.6 GHz and RXOUT_DIV = 1.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
8. Composite jitter with RX and LPM or DFE mode.

*Table 65:* **CPRI Protocol Characteristics**

| Description | Line Rate (Mb/s) | Min | Max | Units |
|---|---|---|---|---|
| **CPRI Transmitter Jitter Generation** | | | | |
| Total transmitter jitter | 614.4 | – | 0.35 | UI |
| | 1228.8 | – | 0.35 | UI |
| | 2457.6 | – | 0.35 | UI |
| | 3072.0 | – | 0.35 | UI |
| | 4915.2 | – | 0.3 | UI |
| | 6144.0 | – | 0.3 | UI |
| | 9830.4 | – | Note 1 | UI |
| **CPRI Receiver Frequency Jitter Tolerance** | | | | |
| Total receiver jitter tolerance | 614.4 | 0.65 | – | UI |
| | 1228.8 | 0.65 | – | UI |
| | 2457.6 | 0.65 | – | UI |
| | 3072.0 | 0.65 | – | UI |
| | 4915.2 | 0.95 | – | UI |
| | 6144.0 | 0.95 | – | UI |
| | 9830.4 | Note 1 | – | UI |

**Notes:**

1. Tested per SFP+ specification, see Table 64.

## Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:
http://www.xilinx.com/technology/protocols/pciexpress.htm

*Table 66:* **Maximum Performance for PCI Express Designs**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.9V | |
| | | -3 | -2/-2L | -1 | -2L | |
| $F_{PIPECLK}$ | Pipe clock maximum frequency | 250.00 | 250.00 | 250.00 | 250.00 | MHz |
| $F_{USERCLK}$ | User clock maximum frequency | 500.00 | 500.00 | 250.00 | 250.00 | MHz |
| $F_{USERCLK2}$ | User clock 2 maximum frequency | 250.00 | 250.00 | 250.00 | 250.00 | MHz |
| $F_{DRPCLK}$ | DRP clock maximum frequency | 250.00 | 250.00 | 250.00 | 250.00 | MHz |

# XADC Specifications

*Table 67:* **XADC Specifications**

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCADC}$ = 1.8V ± 5%, $V_{REFP}$ = 1.25V, $V_{REFN}$ = 0V, ADCCLK = 26 MHz, $T_j$ = –40°C to 100°C, Typical values at $T_j$=+40°C | | | | | | |
| **ADC Accuracy**(1) | | | | | | |
| Resolution | | | 12 | – | – | Bits |
| Integral Nonlinearity(2) | INL | | – | – | ±3 | LSBs |
| Differential Nonlinearity | DNL | No missing codes, guaranteed monotonic | – | – | ±1 | LSBs |
| Offset Error | | Offset calibration enabled | – | – | ±6 | LSBs |
| Gain Error | | Gain calibration disabled | – | – | ±0.5 | % |
| Offset Matching | | Offset calibration enabled | – | – | 4 | LSBs |
| Gain Matching | | Gain calibration disabled | – | – | 0.3 | % |
| Sample Rate | | | 0.1 | – | 1 | MS/s |
| Signal to Noise Ratio(2) | SNR | $F_{SAMPLE}$ = 500KS/s, $F_{IN}$ = 20KHz | 60 | – | – | dB |
| RMS Code Noise | | External 1.25V reference | – | – | 2 | LSBs |
| | | On-chip reference | – | 3 | – | LSBs |
| Total Harmonic Distortion(2) | THD | $F_{SAMPLE}$ = 500KS/s, $F_{IN}$ = 20KHz | – | 70 | – | dB |
| **ADC Accuracy at Extended Temperatures (-55°C to 125°C)** | | | | | | |
| Resolution | | | 10 | – | – | Bits |
| Integral Nonlinearity(2) | INL | | – | – | ±1 | LSB (at 10 bits) |
| Differential Nonlinearity | DNL | No missing codes, guaranteed monotonic | – | – | ±1 | |
| **Analog Inputs**(3) | | | | | | |
| ADC Input Ranges | | Unipolar operation | 0 | – | 1 | V |
| | | Bipolar operation | –0.5 | – | +0.5 | V |
| | | Unipolar common mode range (FS input) | 0 | – | +0.5 | V |
| | | Bipolar common mode range (FS input) | +0.5 | – | +0.6 | V |
| Maximum External Channel Input Ranges | | Adjacent channels set within these ranges should not corrupt measurements on adjacent channels | –0.1 | – | $V_{CCADC}$ | V |
| Auxiliary Channel Full Resolution Bandwidth | FRBW | | 250 | – | – | KHz |
| **On-Chip Sensors** | | | | | | |
| Temperature Sensor Error | | $T_j$ = –40°C to 100°C. | – | – | ±4 | °C |
| | | $T_j$ = –55°C to +125°C | – | – | ±6 | °C |
| Supply Sensor Error | | Measurement range of $V_{CCAUX}$ 1.8V ±5% $T_j$ = –40°C to +100°C | – | – | ±1 | % |
| | | Measurement range of $V_{CCAUX}$ 1.8V ±5% $T_j$ = –55°C to +125°C | – | – | ±2 | % |
| **Conversion Rate**(4) | | | | | | |
| Conversion Time - Continuous | $t_{CONV}$ | Number of ADCCLK cycles | 26 | – | 32 | Cycles |
| Conversion Time - Event | $t_{CONV}$ | Number of CLK cycles | – | – | 21 | Cycles |
| DRP Clock Frequency | DCLK | DRP clock frequency | 8 | – | 250 | MHz |
| ADC Clock Frequency | ADCCLK | Derived from DCLK | 1 | – | 26 | MHz |
| DCLK Duty Cycle | | | 40 | – | 60 | % |