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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	5125
Number of Logic Elements/Cells	65600
Total RAM Bits	4976640
Number of I/O	300
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	676-BBGA, FCBGA
Supplier Device Package	676-FCBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7k70t-3fbg676e

Table 2: Recommended Operating Conditions ⁽¹⁾ (Cont'd)

Symbol	Description	Min	Typ	Max	Units
$V_{MGTAVTTRCAL}$ ⁽⁸⁾	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	1.17	1.2	1.23	V
XADC					
V_{CCADC}	XADC supply relative to GNDADC	1.71	1.80	1.89	V
V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
Temperature					
T_j	Junction temperature operating range for commercial (C) temperature devices	0	–	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	–	100	°C

Notes:

- All voltages are relative to ground.
- V_{CCINT} and V_{CCBRAM} should be connected to the same supply.
- Configuration data is retained even if V_{CCO} drops to 0V.
- Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
- The lower absolute voltage specification always applies.
- A total of 200 mA per bank should not be exceeded.
- V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX} .
- Each voltage listed requires the filter circuit described in [UG476: 7 Series FPGAs GTX/GTH Transceiver User Guide](#).
- For data rates ≤ 10.3125 Gb/s, $V_{MGTAVCC}$ should be 1.0V $\pm 3\%$ for lower power consumption.
- For lower power consumption, $V_{MGTAVCC}$ should be 1.0V $\pm 3\%$ over the entire CPLL frequency range.

Table 3: DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Min	Typ ⁽¹⁾	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	1.5	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	15	μ A
I_L	Input or output leakage current per pin (sample-tested)	–	–	15	μ A
C_{IN} ⁽²⁾	Die input capacitance at the pad	–	–	8	pF
I_{RPU}	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 3.3V$	90	–	330	μ A
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 2.5V$	68	–	250	μ A
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.8V$	34	–	220	μ A
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.5V$	23	–	150	μ A
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.2V$	12	–	120	μ A
I_{RPD}	Pad pull-down (when selected) @ $V_{IN} = 3.3V$	68	–	330	μ A
	Pad pull-down (when selected) @ $V_{IN} = 1.8V$	45	–	180	μ A
I_{CCADC}	Analog supply current, analog circuits in powered up state	–	–	25	mA
I_{BATT} ⁽³⁾	Battery supply current	–	–	150	nA

Table 7 shows the minimum current, in addition to I_{CCQ} , that are required by Kintex-7 devices for proper power-on and configuration. If the current minimums shown in Table 6 and Table 7 are met, the device powers on after all five supplies have passed through their power-on reset threshold voltages. The FPGA must not be configured until after V_{CCINT} is applied.

Once initialized and configured, use the XPower tools to estimate current drain on these supplies.

Table 7: Power-On Current for Kintex-7 Devices

Device	$I_{CCINTMIN}$ Typ ⁽¹⁾	$I_{CCAUXMIN}$ Typ ⁽¹⁾	I_{CCOMIN} Typ ⁽¹⁾	I_{CCAUX_IOMIN} Typ ⁽¹⁾	$I_{CCBRAMMIN}$ Typ ⁽¹⁾	Units
XC7K70T	$I_{CCINTQ} + 450$	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 40$	mA
XC7K160T	$I_{CCINTQ} + 550$	$I_{CCAUXQ} + 50$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 40$	mA
XC7K325T	$I_{CCINTQ} + 600$	$I_{CCAUXQ} + 80$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 40$	mA
XC7K355T	$I_{CCINTQ} + 1450$	$I_{CCAUXQ} + 109$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 81$	mA
XC7K410T	$I_{CCINTQ} + 1500$	$I_{CCAUXQ} + 125$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 90$	mA
XC7K420T	$I_{CCINTQ} + 2200$	$I_{CCAUXQ} + 180$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 108$	mA
XC7K480T	$I_{CCINTQ} + 2200$	$I_{CCAUXQ} + 180$	$I_{CCOQ} + 40$ mA per bank	$I_{CCOAXIOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 108$	mA

Notes:

- Typical values are specified at nominal voltage, 25°C.
- Use the XPower Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate maximum power-on currents.

Table 8: Power Supply Ramp Time

Symbol	Description	Conditions	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}		0.2	50	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO}		0.2	50	ms
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}		0.2	50	ms
T_{VCCAUX_IO}	Ramp time from GND to 90% of V_{CCAUX_IO}		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM}		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$	$T_J = 100^{\circ}C^{(1)}$	–	500	ms
		$T_J = 85^{\circ}C^{(1)}$	–	800	
$T_{MGTAVCC}$	Ramp time from GND to 90% of $V_{MGTAVCC}$		0.2	50	ms
$T_{MGTAVTT}$	Ramp time from GND to 90% of $V_{MGTAVTT}$		0.2	50	ms
$T_{MGTVCCAUX}$	Ramp time from GND to 90% of $V_{MGTVCCAUX}$		0.2	50	ms

Notes:

- Based on 240,000 power cycles with nominal V_{CCO} of 3.3V or 36,500 power cycles with a worst case V_{CCO} of 3.465V.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in ISE® software 14.3 v1.07 for the -3, -2, -2L(1.0V), -1, and v1.06 for -2L(0.9V) speed grades.

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Kintex-7 FPGAs.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. [Table 14](#) correlates the current status of each Kintex-7 device on a per speed grade basis.

Table 14: Kintex-7 Device Speed Grade Designations

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC7K70T			-3, -2, -2L(1.0V), -1, and -2L (0.9V)
XC7K160T			-3, -2, -2L(1.0V), -1, and -2L (0.9V)
XC7K325T			-3, -2, -2L(1.0V), -1, and -2L (0.9V)
XC7K355T			-3, -2, -2L(1.0V), -1, and -2L (0.9V)
XC7K410T			-3, -2, -2L(1.0V), -1, and -2L (0.9V)
XC7K420T			-3, -2, -2L(1.0V), -1, and -2L (0.9V)
XC7K480T			-3, -2, -2L(1.0V), -1, and -2L (0.9V)

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

[Table 15](#) lists the production released Kintex-7 device, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 15: Kintex-7 Device Production Software and Speed Specification Release

Device	Speed Grade Designations			
	1.0V			0.9V
	-3	-2/-2L	-1	-2L
XC7K70T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K160T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K325T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K355T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K410T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K420T	ISE 14.2 v1.06			ISE 14.3 v1.06
XC7K480T	ISE 14.2 v1.06			ISE 14.3 v1.06

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Kintex-7 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the [AC Switching Characteristics, page 11](#). In each table, the I/O bank type is either High Performance (HP) or High Range (HR).

Table 16: Networking Applications Interface Performances

Description	I/O Bank Type	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	HR	710	710	625	625	Mb/s
	HP	710	710	625	625	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	HR	1250	1250	950	950	Mb/s
	HP	1600	1400	1250	1250	Mb/s
SDR LVDS receiver (SFI-4.1) ⁽¹⁾	HR	710	710	625	625	Mb/s
	HP	710	710	625	625	Mb/s
DDR LVDS receiver (SFI-4.2) ⁽¹⁾	HR	1250	1250	950	950	Mb/s
	HP	1600	1400	1250	1250	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 17: Maximum Physical Interface (PHY) Rate for Memory Interfaces (FFG Packages)⁽¹⁾⁽²⁾

Memory Standard	I/O Bank Type	V _{CCAUX_IO}	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
4:1 Memory Controllers							
DDR3	HP	2.0V	1866	1866	1600	1333	Mb/s
	HP	1.8V	1600	1333	1066	1066	Mb/s
	HR	N/A	1066	1066	800	800	Mb/s
DDR3L	HP	2.0V	1600	1600	1333	1066	Mb/s
	HP	1.8V	1333	1066	800	800	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	2.0V	800	800	800	800	Mb/s
	HP	1.8V	800	800	800	800	Mb/s
	HR	N/A	800	800	800	800	Mb/s
RLDRAM III ⁽³⁾	HP	2.0V	800	667	667	533	MHz
	HP	1.8V	550	500	450	450	MHz
	HR	N/A	N/A				
2:1 Memory Controllers							
DDR3	HP	2.0V	1066	1066	800	800	Mb/s
	HP	1.8V	1066	1066	800	800	Mb/s
	HR	N/A	1066	1066	800	800	Mb/s
DDR3L	HP	2.0V	1066	1066	800	800	Mb/s
	HP	1.8V	1066	1066	800	800	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	2.0V	800	800	800	800	Mb/s
	HP	1.8V					
	HR	N/A					
QDR II+ ⁽⁴⁾	HP	2.0V	550	500	450	450	MHz
	HP	1.8V					
	HR	N/A					
RLDRAM II	HP	2.0V	533	500	450	450	MHz
	HP	1.8V					
	HR	N/A					
LPDDR2 ⁽³⁾	HP	2.0V	800	800	800	800	Mb/s
	HP	1.8V	800	800	800	800	Mb/s
	HR	N/A	800	667	667	667	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see [UG586](#), 7 Series FPGAs Memory Interface Solutions User Guide.
2. When using the internal V_{REF} the maximum data rate is 800 Mb/s (400 MHz).
3. RLDRAM III (BL = 4, BL = 8) and LPDDR2 specifications have not been validated with memory IP.
4. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

Table 18: Maximum Physical Interface (PHY) Rate for Memory Interfaces (FBG Packages)⁽¹⁾⁽²⁾

Memory Standard	I/O Bank Type	V _{CCAUX_IO} ⁽³⁾	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
4:1 Memory Controllers							
DDR3	HP	N/A	1333	1066	800	800	Mb/s
	HR	N/A	1066	800	800	800	Mb/s
DDR3L	HP	N/A	1066	800	667	667	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	N/A	800	800	800	800	Mb/s
	HR	N/A	800	667	667	667	Mb/s
RLDRAM III ⁽⁴⁾	HP	N/A	550	500	450	450	MHz
	HR	N/A	N/A				
2:1 Memory Controllers							
DDR3	HP	N/A	1066	1066	800	800	Mb/s
	HR	N/A	1066	800	800	800	Mb/s
DDR3L	HP	N/A	1066	800	667	667	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	N/A	800	800	800	800	Mb/s
	HR	N/A	800	667	667	667	Mb/s
QDR II+ ⁽⁵⁾	HP	N/A	550	500	450	450	MHz
	HR	N/A	450	400	350	350	MHz
RLDRAM II	HP	N/A	533	500	450	450	MHz
	HR	N/A					
LPDDR2 ⁽⁴⁾	HP	N/A	667	667	667	667	Mb/s
	HR	N/A	667	667	533	533	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see [UG586](#), *7 Series FPGAs Memory Interface Solutions User Guide*.
2. When using the internal V_{REF} the maximum data rate is 800 Mb/s (400 MHz).
3. FBG packages do not have separate V_{CCAUX_IO} supply pins to adjust the pre-driver voltage of the HP I/O banks.
4. RLDRAM III (BL = 4, BL = 8) and LPDDR2 specifications have not been validated with memory IP.
5. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standard	T _{IOP1}				T _{IOP0}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVC MOS12_F8	0.64	0.67	0.78	0.95	1.27	1.42	1.55	1.41	1.91	2.18	2.37	2.02	ns
LVDCI_18	0.47	0.50	0.60	0.86	1.99	2.15	2.35	2.44	2.62	2.91	3.17	3.05	ns
LVDCI_15	0.59	0.62	0.73	0.87	1.98	2.23	2.58	2.40	2.62	2.99	3.40	3.01	ns
LVDCI_DV2_18	0.47	0.50	0.60	0.87	1.99	2.15	2.34	1.86	2.62	2.90	3.17	2.48	ns
LVDCI_DV2_15	0.59	0.62	0.73	0.87	1.98	2.23	2.58	1.83	2.62	2.99	3.40	2.44	ns
HSLVDCI_18	0.68	0.72	0.82	0.86	1.99	2.15	2.35	2.43	2.62	2.91	3.17	3.04	ns
HSLVDCI_15	0.68	0.72	0.82	0.84	1.98	2.23	2.58	2.27	2.62	2.99	3.40	2.88	ns
SSTL18_I_S	0.68	0.72	0.82	0.86	1.02	1.15	1.24	1.41	1.66	1.90	2.07	2.02	ns
SSTL18_II_S	0.68	0.72	0.82	0.87	1.17	1.29	1.37	1.55	1.81	2.05	2.19	2.16	ns
SSTL18_I_DCI_S	0.68	0.72	0.82	0.76	0.92	1.06	1.17	1.32	1.56	1.82	1.99	1.93	ns
SSTL18_II_DCI_S	0.68	0.72	0.82	0.78	0.88	0.98	1.08	1.26	1.51	1.74	1.90	1.87	ns
SSTL18_II_T_DCI_S	0.68	0.72	0.82	0.78	0.92	1.06	1.17	1.32	1.56	1.82	1.99	1.93	ns
SSTL15_S	0.68	0.72	0.82	0.81	0.94	1.06	1.15	1.32	1.58	1.82	1.97	1.93	ns
SSTL15_DCI_S	0.68	0.72	0.82	0.78	0.94	1.06	1.15	1.30	1.57	1.82	1.97	1.91	ns
SSTL15_T_DCI_S	0.68	0.72	0.82	0.80	0.94	1.06	1.15	1.30	1.57	1.82	1.97	1.91	ns
SSTL135_S	0.69	0.72	0.82	0.89	0.97	1.10	1.19	1.35	1.60	1.85	2.01	1.96	ns
SSTL135_DCI_S	0.69	0.72	0.82	0.84	0.97	1.09	1.19	1.33	1.60	1.85	2.01	1.94	ns
SSTL135_T_DCI_S	0.69	0.72	0.82	0.84	0.97	1.09	1.19	1.33	1.60	1.85	2.01	1.94	ns
SSTL12_S	0.69	0.72	0.82	0.95	0.96	1.09	1.18	1.33	1.60	1.84	2.00	1.94	ns
SSTL12_DCI_S	0.69	0.72	0.82	0.91	1.03	1.17	1.27	1.33	1.66	1.92	2.09	1.94	ns
SSTL12_T_DCI_S	0.69	0.72	0.82	0.91	1.03	1.17	1.27	1.33	1.66	1.92	2.09	1.94	ns
DIFF_SSTL18_I_S	0.75	0.79	0.92	0.89	1.02	1.15	1.24	1.43	1.66	1.90	2.07	2.04	ns
DIFF_SSTL18_II_S	0.75	0.79	0.92	0.89	1.17	1.29	1.37	1.55	1.81	2.05	2.19	2.16	ns
DIFF_SSTL18_I_DCI_S	0.75	0.79	0.92	0.76	0.92	1.06	1.17	1.40	1.56	1.82	1.99	2.01	ns
DIFF_SSTL18_II_DCI_S	0.75	0.79	0.92	0.75	0.88	0.98	1.08	1.33	1.51	1.74	1.90	1.94	ns
DIFF_SSTL18_II_T_DCI_S	0.75	0.79	0.92	0.76	0.92	1.06	1.17	1.40	1.56	1.82	1.99	2.01	ns
DIFF_SSTL15_S	0.68	0.72	0.82	0.89	0.94	1.06	1.15	1.32	1.58	1.82	1.97	1.93	ns
DIFF_SSTL15_DCI_S	0.68	0.72	0.82	0.75	0.94	1.06	1.15	1.30	1.57	1.82	1.97	1.91	ns
DIFF_SSTL15_T_DCI_S	0.68	0.72	0.82	0.76	0.94	1.06	1.15	1.38	1.57	1.82	1.97	1.99	ns
DIFF_SSTL135_S	0.69	0.72	0.82	0.91	0.97	1.10	1.19	1.35	1.60	1.85	2.01	1.96	ns
DIFF_SSTL135_DCI_S	0.69	0.72	0.82	0.76	0.97	1.09	1.19	1.33	1.60	1.85	2.01	1.94	ns
DIFF_SSTL135_T_DCI_S	0.69	0.72	0.82	0.76	0.97	1.09	1.19	1.43	1.60	1.85	2.01	2.04	ns
DIFF_SSTL12_S	0.69	0.72	0.82	0.91	0.96	1.09	1.18	1.33	1.60	1.84	2.00	1.94	ns
DIFF_SSTL12_DCI_S	0.69	0.72	0.82	0.78	1.03	1.17	1.27	1.33	1.66	1.92	2.09	1.94	ns
DIFF_SSTL12_T_DCI_S	0.69	0.72	0.82	0.80	1.03	1.17	1.27	1.41	1.66	1.92	2.09	2.02	ns

Table 20: 1.8V IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
SSTL18_I_F	0.68	0.72	0.82	0.86	0.94	1.06	1.15	1.32	1.58	1.82	1.97	1.93	ns
SSTL18_II_F	0.68	0.72	0.82	0.87	0.97	1.09	1.16	1.36	1.61	1.84	1.99	1.98	ns
SSTL18_I_DCI_F	0.68	0.72	0.82	0.76	0.89	1.02	1.10	1.30	1.53	1.77	1.92	1.91	ns
SSTL18_II_DCI_F	0.68	0.72	0.82	0.78	0.89	1.02	1.10	1.24	1.53	1.77	1.92	1.85	ns
SSTL18_II_T_DCI_F	0.68	0.72	0.82	0.78	0.89	1.02	1.10	1.27	1.53	1.77	1.92	1.88	ns
SSTL15_F	0.68	0.72	0.82	0.81	0.89	1.01	1.09	1.24	1.53	1.77	1.91	1.85	ns
SSTL15_DCI_F	0.68	0.72	0.82	0.78	0.89	1.01	1.09	1.27	1.53	1.77	1.91	1.88	ns
SSTL15_T_DCI_F	0.68	0.72	0.82	0.80	0.89	1.01	1.09	1.27	1.53	1.77	1.91	1.88	ns
SSTL135_F	0.69	0.72	0.82	0.89	0.88	1.00	1.08	1.27	1.52	1.76	1.90	1.88	ns
SSTL135_DCI_F	0.69	0.72	0.82	0.84	0.89	1.00	1.08	1.27	1.52	1.76	1.90	1.88	ns
SSTL135_T_DCI_F	0.69	0.72	0.82	0.84	0.89	1.00	1.08	1.27	1.52	1.76	1.90	1.88	ns
SSTL12_F	0.69	0.72	0.82	0.95	0.88	1.00	1.08	1.26	1.52	1.76	1.90	1.87	ns
SSTL12_DCI_F	0.69	0.72	0.82	0.91	0.91	1.03	1.11	1.24	1.54	1.79	1.93	1.85	ns
SSTL12_T_DCI_F	0.69	0.72	0.82	0.91	0.91	1.03	1.11	1.26	1.54	1.79	1.93	1.87	ns
DIFF_SSTL18_I_F	0.75	0.79	0.92	0.89	0.94	1.06	1.15	1.38	1.58	1.82	1.97	1.99	ns
DIFF_SSTL18_II_F	0.75	0.79	0.92	0.89	0.97	1.09	1.16	1.40	1.61	1.84	1.99	2.01	ns
DIFF_SSTL18_I_DCI_F	0.75	0.79	0.92	0.76	0.89	1.02	1.10	1.36	1.53	1.77	1.92	1.98	ns
DIFF_SSTL18_II_DCI_F	0.75	0.79	0.92	0.75	0.89	1.02	1.10	1.32	1.53	1.77	1.92	1.93	ns
DIFF_SSTL18_II_T_DCI_F	0.75	0.79	0.92	0.76	0.89	1.02	1.10	1.38	1.53	1.77	1.92	1.99	ns
DIFF_SSTL15_F	0.68	0.72	0.82	0.89	0.89	1.01	1.09	1.24	1.53	1.77	1.91	1.85	ns
DIFF_SSTL15_DCI_F	0.68	0.72	0.82	0.75	0.89	1.01	1.09	1.27	1.53	1.77	1.91	1.88	ns
DIFF_SSTL15_T_DCI_F	0.68	0.72	0.82	0.76	0.89	1.01	1.09	1.35	1.53	1.77	1.91	1.96	ns
DIFF_SSTL135_F	0.69	0.72	0.82	0.91	0.88	1.00	1.08	1.27	1.52	1.76	1.90	1.88	ns
DIFF_SSTL135_DCI_F	0.69	0.72	0.82	0.76	0.89	1.00	1.08	1.27	1.52	1.76	1.90	1.88	ns
DIFF_SSTL135_T_DCI_F	0.69	0.72	0.82	0.76	0.89	1.00	1.08	1.35	1.52	1.76	1.90	1.96	ns
DIFF_SSTL12_F	0.69	0.72	0.82	0.91	0.88	1.00	1.08	1.26	1.52	1.76	1.90	1.87	ns
DIFF_SSTL12_DCI_F	0.69	0.72	0.82	0.78	0.91	1.03	1.11	1.24	1.54	1.79	1.93	1.85	ns
DIFF_SSTL12_T_DCI_F	0.69	0.72	0.82	0.80	0.91	1.03	1.11	1.33	1.54	1.79	1.93	1.94	ns

Notes:

1. This I/O standard is only available in the 1.8V high-performance (HP) banks.

CLB Switching Characteristics

Table 28: CLB Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Combinatorial Delays						
T _{ILO}	An – Dn LUT address to A	0.05	0.05	0.06	0.07	ns, Max
T _{ILO_2}	An – Dn LUT address to AMUX/CMUX	0.15	0.16	0.19	0.22	ns, Max
T _{ILO_3}	An – Dn LUT address to BMUX_A	0.24	0.25	0.30	0.37	ns, Max
T _{ITO}	An – Dn inputs to A – D Q outputs	0.58	0.61	0.74	0.91	ns, Max
T _{AXA}	AX inputs to AMUX output	0.38	0.40	0.49	0.62	ns, Max
T _{AXB}	AX inputs to BMUX output	0.40	0.42	0.52	0.66	ns, Max
T _{AXC}	AX inputs to CMUX output	0.39	0.41	0.50	0.62	ns, Max
T _{AXD}	AX inputs to DMUX output	0.43	0.44	0.52	0.67	ns, Max
T _{BXB}	BX inputs to BMUX output	0.31	0.33	0.40	0.51	ns, Max
T _{BXD}	BX inputs to DMUX output	0.38	0.39	0.47	0.62	ns, Max
T _{CXC}	CX inputs to CMUX output	0.27	0.28	0.34	0.43	ns, Max
T _{CXD}	CX inputs to DMUX output	0.33	0.34	0.41	0.54	ns, Max
T _{DXD}	DX inputs to DMUX output	0.32	0.33	0.40	0.52	ns, Max
Sequential Delays						
T _{CKO}	Clock to AQ – DQ outputs	0.26	0.27	0.32	0.40	ns, Max
T _{SHCKO}	Clock to AMUX – DMUX outputs	0.32	0.32	0.39	0.46	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T _{AS} /T _{AH}	A _N – D _N input to CLK on A – D Flip Flops	0.01/0.12	0.02/0.13	0.03/0.18	0.02/0.18	ns, Min
T _{DICK} /T _{CKDI}	A _X – D _X input to CLK on A – D Flip Flops	0.04/0.14	0.04/0.14	0.05/0.20	0.05/0.21	ns, Min
	A _X – D _X input through MUXs and/or carry logic to CLK on A – D Flip Flops	0.36/0.10	0.37/0.11	0.46/0.16	0.56/0.15	ns, Min
T _{CECK_CLB} /T _{CKCE_CLB}	CE input to CLK on A – D Flip Flops	0.19/0.05	0.20/0.05	0.25/0.05	0.24/0.04	ns, Min
T _{SRCK} /T _{CKSR}	SR input to CLK on A – D Flip Flops	0.30/0.05	0.31/0.07	0.37/0.09	0.48/0.05	ns, Min
Set/Reset						
T _{SRMIN}	SR input minimum pulse width	0.52	0.78	1.04	0.95	ns, Min
T _{RQ}	Delay from SR input to AQ – DQ flip-flops	0.38	0.38	0.46	0.59	ns, Max
T _{CEO}	Delay from CE input to AQ – DQ flip-flops	0.34	0.35	0.43	0.54	ns, Max
F _{TOG}	Toggle frequency (for export control)	1818	1818	1818	1286	MHz

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 29: CLB Distributed RAM Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Sequential Delays						
T _{SHCKO}	Clock to A – B outputs	0.68	0.70	0.85	1.08	ns, Max
T _{SHCKO_1}	Clock to AMUX – BMUX outputs	0.91	0.95	1.15	1.44	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{DS_LRAM} /T _{DH_LRAM}	A – D inputs to CLK	0.45/0.23	0.45/0.24	0.54/0.27	0.69/0.33	ns, Min
T _{AS_LRAM} /T _{AH_LRAM}	Address An inputs to clock	0.13/0.50	0.14/0.50	0.17/0.58	0.21/0.63	ns, Min
	Address An inputs through MUXs and/or carry logic to clock	0.40/0.16	0.42/0.17	0.52/0.23	0.63/0.23	ns, Min
T _{WS_LRAM} /T _{WH_LRAM}	WE input to clock	0.29/0.09	0.30/0.09	0.36/0.09	0.46/0.10	ns, Min
T _{CECK_LRAM} / T _{CKCE_LRAM}	CE input to CLK	0.29/0.09	0.30/0.09	0.37/0.09	0.47/0.10	ns, Min
Clock CLK						
T _{MPW}	Minimum pulse width	0.68	0.77	0.91	1.11	ns, Min
T _{MCP}	Minimum clock period	1.35	1.54	1.82	2.22	ns, Min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time.
2. T_{SHCKO} also represents the CLK to XMUX output. Refer to TRACE report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 30: CLB Shift Register Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Sequential Delays						
T _{REG}	Clock to A – D outputs	0.96	0.98	1.20	1.35	ns, Max
T _{REG_MUX}	Clock to AMUX – DMUX output	1.19	1.23	1.50	1.72	ns, Max
T _{REG_M31}	Clock to DMUX output via M31 output	0.89	0.91	1.10	1.25	ns, Max
Setup and Hold Times Before/After Clock CLK						
T _{WS_SHFREG} / T _{WH_SHFREG}	WE input	0.26/0.09	0.27/0.09	0.33/0.09	0.41/0.10	ns, Min
T _{CECK_SHFREG} / T _{CKCE_SHFREG}	CE input to CLK	0.27/0.09	0.28/0.09	0.33/0.09	0.42/0.10	ns, Min
T _{DS_SHFREG} / T _{DH_SHFREG}	A – D inputs to CLK	0.28/0.26	0.28/0.26	0.33/0.30	0.41/0.36	ns, Min
Clock CLK						
T _{MPW_SHFREG}	Minimum pulse width	0.55	0.65	0.78	0.91	ns, Min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time.

Block RAM and FIFO Switching Characteristics

Table 31: Block RAM and FIFO Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Block RAM and FIFO Clock-to-Out Delays						
T_{RCKO_DO} and $T_{RCKO_DO_REG}^{(1)}$	Clock CLK to DOUT output (without output register) ⁽²⁾⁽³⁾	1.57	1.80	2.08	2.44	ns, Max
	Clock CLK to DOUT output (with output register) ⁽⁴⁾⁽⁵⁾	0.54	0.63	0.75	0.86	ns, Max
$T_{RCKO_DO_ECC}$ and $T_{RCKO_DO_ECC_REG}$	Clock CLK to DOUT output with ECC (without output register) ⁽²⁾⁽³⁾	2.35	2.58	3.26	4.49	ns, Max
	Clock CLK to DOUT output with ECC (with output register) ⁽⁴⁾⁽⁵⁾	0.62	0.69	0.80	0.94	ns, Max
$T_{RCKO_DO_CASCOUT}$ and $T_{RCKO_DO_CASCOUT_REG}$	Clock CLK to DOUT output with Cascade (without output register) ⁽²⁾	2.21	2.45	2.80	3.19	ns, Max
	Clock CLK to DOUT output with Cascade (with output register) ⁽⁴⁾	0.98	1.08	1.24	1.32	ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs ⁽⁶⁾	0.65	0.74	0.89	0.97	ns, Max
$T_{RCKO_POINTERS}$	Clock CLK to FIFO pointers outputs ⁽⁷⁾	0.79	0.87	0.98	1.10	ns, Max
$T_{RCKO_PARITY_ECC}$	Clock CLK to ECCPARITY in ECC encode only mode	0.66	0.72	0.80	0.93	ns, Max
$T_{RCKO_SDBIT_ECC}$ and $T_{RCKO_SDBIT_ECC_REG}$	Clock CLK to BITERR (without output register)	2.17	2.38	3.01	4.15	ns, Max
	Clock CLK to BITERR (with output register)	0.57	0.65	0.76	0.89	ns, Max
$T_{RCKO_RDADDR_ECC}$ and $T_{RCKO_RDADDR_ECC_REG}$	Clock CLK to RDADDR output with ECC (without output register)	0.64	0.74	0.90	0.98	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.71	0.79	0.92	1.10	ns, Max
Setup and Hold Times Before/After Clock CLK						
$T_{RCKCK_ADDR}/T_{RCKC_ADDR}$	ADDR inputs ⁽⁸⁾	0.38/0.27	0.42/0.28	0.48/0.31	0.65/0.38	ns, Min
$T_{RDCK_DI_WF_NC}/T_{RCKD_DI_WF_NC}$	Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode ⁽⁹⁾	0.49/0.51	0.55/0.53	0.63/0.57	0.78/0.64	ns, Min
$T_{RDCK_DI_RF}/T_{RCKD_DI_RF}$	Data input setup/hold time when block RAM is configured in READ_FIRST mode ⁽⁹⁾	0.17/0.25	0.19/0.29	0.21/0.35	0.25/0.32	ns, Min
$T_{RDCK_DI_ECC}/T_{RCKD_DI_ECC}$	DIN inputs with block RAM ECC in standard mode ⁽⁹⁾	0.42/0.37	0.47/0.39	0.53/0.43	0.66/0.46	ns, Min
$T_{RDCK_DI_ECCW}/T_{RCKD_DI_ECCW}$	DIN inputs with block RAM ECC encode only ⁽⁹⁾	0.79/0.37	0.87/0.39	0.99/0.43	1.17/0.41	ns, Min
$T_{RDCK_DI_ECC_FIFO}/T_{RCKD_DI_ECC_FIFO}$	DIN inputs with FIFO ECC in standard mode ⁽⁹⁾	0.89/0.47	0.98/0.50	1.12/0.54	1.32/0.65	ns, Min
$T_{RCKCK_INJECTBITERR}/T_{RCKC_INJECTBITERR}$	Inject single/double bit error in ECC mode	0.49/0.30	0.55/0.31	0.63/0.34	0.78/0.41	ns, Min
T_{RCKCK_EN}/T_{RCKC_EN}	Block RAM Enable (EN) input	0.30/0.17	0.33/0.18	0.38/0.20	0.48/0.22	ns, Min
$T_{RCKCK_REGCE}/T_{RCKC_REGCE}$	CE input of output register	0.21/0.13	0.25/0.13	0.31/0.14	0.34/0.16	ns, Min
$T_{RCKCK_RSTREG}/T_{RCKC_RSTREG}$	Synchronous RSTREG input	0.25/0.06	0.27/0.06	0.29/0.06	0.35/0.06	ns, Min

DSP48E1 Switching Characteristics

Table 32: DSP48E1 Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock						
T _{DSPDCK_A_AREG} /T _{DSPCKD_A_AREG}	A input to A register CLK	0.24/ 0.12	0.27/ 0.14	0.31/ 0.16	0.38/ 0.12	ns
T _{DSPDCK_B_BREG} /T _{DSPCKD_B_BREG}	B input to B register CLK	0.28/ 0.13	0.32/ 0.14	0.39/ 0.15	0.51/ 0.16	ns
T _{DSPDCK_C_CREG} /T _{DSPCKD_C_CREG}	C input to C register CLK	0.15/ 0.15	0.17/ 0.17	0.20/ 0.20	0.31/ 0.21	ns
T _{DSPDCK_D_DREG} /T _{DSPCKD_D_DREG}	D input to D register CLK	0.21/ 0.19	0.27/ 0.22	0.35/ 0.26	0.46/ 0.20	ns
T _{DSPDCK_ACIN_AREG} /T _{DSPCKD_ACIN_AREG}	ACIN input to A register CLK	0.21/ 0.12	0.24/ 0.14	0.27/ 0.16	0.31/ 0.12	ns
T _{DSPDCK_BCIN_BREG} /T _{DSPCKD_BCIN_BREG}	BCIN input to B register CLK	0.22/ 0.13	0.25/ 0.14	0.30/ 0.15	0.34/ 0.16	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock						
T _{DSPDCK_{A, B}_MREG_MULT} / T _{DSPCKD_B_MREG_MULT}	{A, B,} input to M register CLK using multiplier	2.04/ −0.01	2.34/ −0.01	2.79/ −0.01	3.66/ −0.06	ns
T _{DSPDCK_{A, B}_ADREG} / T _{DSPCKD_D_ADREG}	{A, D} input to AD register CLK	1.09/ −0.02	1.25/ −0.02	1.49/ −0.02	1.94/ −0.23	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock						
T _{DSPDCK_{A, B}_PREG_MULT} / T _{DSPCKD_{A, B}_PREG_MULT}	{A, B,} input to P register CLK using multiplier	3.41/ −0.24	3.90/ −0.24	4.64/ −0.24	5.89/ −0.41	ns
T _{DSPDCK_D_PREG_MULT} / T _{DSPCKD_D_PREG_MULT}	D input to P register CLK using multiplier	3.33/ −0.62	3.81/ −0.62	4.53/ −0.62	5.70/ −1.42	ns
T _{DSPDCK_{A, B}_PREG} / T _{DSPCKD_{A, B}_PREG}	A or B input to P register CLK not using multiplier	1.47/ −0.24	1.68/ −0.24	2.00/ −0.24	2.37/ −0.41	ns
T _{DSPDCK_C_PREG} / T _{DSPCKD_C_PREG}	C input to P register CLK not using multiplier	1.30/ −0.22	1.49/ −0.22	1.78/ −0.22	2.11/ −0.36	ns
T _{DSPDCK_PCIN_PREG} / T _{DSPCKD_PCIN_PREG}	PCIN input to P register CLK	1.12/ −0.13	1.28/ −0.13	1.52/ −0.13	1.81/ −0.21	ns
Setup and Hold Times of the CE Pins						
T _{DSPDCK_{CEA;CEB}_{AREG;BREG}} / T _{DSPCKD_{CEA;CEB}_{AREG;BREG}}	{CEA; CEB} input to {A; B} register CLK	0.30/ 0.05	0.36/ 0.06	0.44/ 0.09	0.55/ 0.09	ns
T _{DSPDCK_CEC_CREG} / T _{DSPCKD_CEC_CREG}	CEC input to C register CLK	0.24/ 0.08	0.29/ 0.09	0.36/ 0.11	0.43/ 0.11	ns
T _{DSPDCK_CED_DREG} / T _{DSPCKD_CED_DREG}	CED input to D register CLK	0.31/ −0.02	0.36/ −0.02	0.44/ −0.02	0.58/ 0.12	ns
T _{DSPDCK_CEM_MREG} / T _{DSPCKD_CEM_MREG}	CEM input to M register CLK	0.26/ 0.15	0.29/ 0.17	0.33/ 0.20	0.39/ 0.25	ns
T _{DSPDCK_CEP_PREG} / T _{DSPCKD_CEP_PREG}	CEP input to P register CLK	0.31/ 0.01	0.36/ 0.01	0.45/ 0.01	0.54/ 0.00	ns

Table 32: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup and Hold Times of the RST Pins						
T _{DSPDCK_{RSTA; RSTB}_{AREG; BREG}/T_{DSPCKD_{RSTA; RSTB}_{AREG; BREG}}}	{RSTA, RSTB} input to {A, B} register CLK	0.34/ 0.10	0.39/ 0.11	0.47/ 0.13	0.53/ 0.34	ns
T _{DSPDCK_RSTC_CREG/ T_{DSPCKD_RSTC_CREG}}	RSTC input to C register CLK	0.06/ 0.22	0.07/ 0.24	0.08/ 0.26	0.08/ 0.31	ns
T _{DSPDCK_RSTD_DREG/ T_{DSPCKD_RSTD_DREG}}	RSTD input to D register CLK	0.37/ 0.06	0.42/ 0.06	0.50/ 0.07	0.57/ 0.07	ns
T _{DSPDCK_RSTM_MREG/ T_{DSPCKD_RSTM_MREG}}	RSTM input to M register CLK	0.18/ 0.18	0.20/ 0.21	0.23/ 0.24	0.24/ 0.29	ns
T _{DSPDCK_RSTP_PREG/ T_{DSPCKD_RSTP_PREG}}	RSTP input to P register CLK	0.24/ 0.01	0.26/ 0.01	0.30/ 0.01	0.37/ 0.00	ns
Combinatorial Delays from Input Pins to Output Pins						
T _{DSPDO_A_CARRYOUT_MULT}	A input to CARRYOUT output using multiplier	3.21	3.69	4.39	5.60	ns
T _{DSPDO_D_P_MULT}	D input to P output using multiplier	3.15	3.61	4.30	5.44	ns
T _{DSPDO_A_P}	A input to P output not using multiplier	1.30	1.48	1.76	2.10	ns
T _{DSPDO_C_P}	C input to P output	1.13	1.30	1.55	1.84	ns
Combinatorial Delays from Input Pins to Cascading Output Pins						
T _{DSPDO_{A; B}_{ACOUT; BCOUT}}	{A, B} input to {ACOUT, BCOUT} output	0.47	0.53	0.63	0.75	ns
T _{DSPDO_{A, B}_CARRYCASCOUT_MULT}	{A, B} input to CARRYCASCOUT output using multiplier	3.44	3.94	4.69	5.96	ns
T _{DSPDO_D_CARRYCASCOUT_MULT}	D input to CARRYCASCOUT output using multiplier	3.36	3.85	4.58	5.77	ns
T _{DSPDO_{A, B}_CARRYCASCOUT}	{A, B} input to CARRYCASCOUT output not using multiplier	1.50	1.72	2.04	2.44	ns
T _{DSPDO_C_CARRYCASCOUT}	C input to CARRYCASCOUT output	1.34	1.53	1.83	2.18	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins						
T _{DSPDO_ACIN_P_MULT}	ACIN input to P output using multiplier	3.09	3.55	4.24	5.42	ns
T _{DSPDO_ACIN_P}	ACIN input to P output not using multiplier	1.16	1.33	1.59	2.07	ns
T _{DSPDO_ACIN_ACOUT}	ACIN input to ACOUT output	0.32	0.37	0.45	0.53	ns
T _{DSPDO_ACIN_CARRYCASCOUT_MULT}	ACIN input to CARRYCASCOUT output using multiplier	3.30	3.79	4.52	5.76	ns
T _{DSPDO_ACIN_CARRYCASCOUT}	ACIN input to CARRYCASCOUT output not using multiplier	1.37	1.57	1.87	2.40	ns
T _{DSPDO_PCIN_P}	PCIN input to P output	0.94	1.08	1.29	1.54	ns
T _{DSPDO_PCIN_CARRYCASCOUT}	PCIN input to CARRYCASCOUT output	1.15	1.32	1.57	1.88	ns
Clock to Outs from Output Register Clock to Output Pins						
T _{DSPCKO_P_PREG}	CLK PREG to P output	0.33	0.35	0.39	0.45	ns
T _{DSPCKO_CARRYCASCOUT_PREG}	CLK PREG to CARRYCASCOUT output	0.44	0.50	0.59	0.71	ns

Table 32: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Clock to Outs from Pipeline Register Clock to Output Pins						
T_DSPCKO_P_MREG	CLK MREG to P output	1.42	1.64	1.96	2.31	ns
T_DSPCKO_CARRYCASCOUT_MREG	CLK MREG to CARRYCASCOUT output	1.63	1.87	2.24	2.65	ns
T_DSPCKO_P_ADREG_MULT	CLK ADREG to P output using multiplier	2.30	2.63	3.13	3.90	ns
T_DSPCKO_CARRYCASCOUT_ADREG_MULT	CLK ADREG to CARRYCASCOUT output using multiplier	2.51	2.87	3.41	4.23	ns
Clock to Outs from Input Register Clock to Output Pins						
T_DSPCKO_P_AREG_MULT	CLK AREG to P output using multiplier	3.34	3.83	4.55	5.80	ns
T_DSPCKO_P_BREG	CLK BREG to P output not using multiplier	1.39	1.59	1.88	2.24	ns
T_DSPCKO_P_CREG	CLK CREG to P output not using multiplier	1.43	1.64	1.95	2.32	ns
T_DSPCKO_P_DREG_MULT	CLK DREG to P output using multiplier	3.32	3.80	4.51	5.74	ns
Clock to Outs from Input Register Clock to Cascading Output Pins						
T_DSPCKO_{ACOUT; BCOUT}_{AREG; BREG}	CLK (ACOUT, BCOUT) to {A,B} register output	0.55	0.62	0.74	0.87	ns
T_DSPCKO_CARRYCASCOUT_{AREG, BREG}_MULT	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier	3.55	4.06	4.84	6.13	ns
T_DSPCKO_CARRYCASCOUT_ BREG	CLK BREG to CARRYCASCOUT output not using multiplier	1.60	1.82	2.16	2.58	ns
T_DSPCKO_CARRYCASCOUT_ DREG_MULT	CLK DREG to CARRYCASCOUT output using multiplier	3.52	4.03	4.79	6.07	ns
T_DSPCKO_CARRYCASCOUT_ CREG	CLK CREG to CARRYCASCOUT output	1.64	1.88	2.23	2.65	ns
Maximum Frequency						
F_MAX	With all registers used	741.84	650.20	547.95	429.37	MHz
F_MAX_PATDET	With pattern detector	627.35	549.75	463.61	365.90	MHz
F_MAX_MULT_NOMREG	Two register multiply without MREG	412.20	360.75	303.77	248.32	MHz
F_MAX_MULT_NOMREG_PATDET	Two register multiply without MREG with pattern detect	374.25	327.65	276.01	225.73	MHz
F_MAX_PREADD_MULT_NOADREG	Without ADREG	468.82	408.66	342.70	263.44	MHz
F_MAX_PREADD_MULT_NOADREG_PATDET	Without ADREG with pattern detect	468.82	408.66	342.70	263.44	MHz
F_MAX_NOPIPELINEREG	Without pipeline registers (MREG, ADREG)	306.84	267.81	225.02	177.15	MHz
F_MAX_NOPIPELINEREG_PATDET	Without pipeline registers (MREG, ADREG) with pattern detect	285.23	249.13	209.38	165.32	MHz

MMCM Switching Characteristics

Table 38: MMCM Specification

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
MMCM_F _{INMAX}	Maximum Input Clock Frequency	1066.00	933.00	800.00	800.00	MHz
MMCM_F _{INMIN}	Minimum Input Clock Frequency	10.00	10.00	10.00	10.00	MHz
MMCM_F _{INJITTER}	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max				
MMCM_F _{INDUTY}	Allowable Input Duty Cycle: 10—49 MHz	25.00	25.00	25.00	25.00	%
	Allowable Input Duty Cycle: 50—199 MHz	30.00	30.00	30.00	30.00	%
	Allowable Input Duty Cycle: 200—399 MHz	35.00	35.00	35.00	35.00	%
	Allowable Input Duty Cycle: 400—499 MHz	40.00	40.00	40.00	40.00	%
	Allowable Input Duty Cycle: >500 MHz	45.00	45.00	45.00	45.00	%
MMCM_F _{MIN_PSCLK}	Minimum Dynamic Phase Shift Clock Frequency	0.01	0.01	0.01	0.01	MHz
MMCM_F _{MAX_PSCLK}	Maximum Dynamic Phase Shift Clock Frequency	550.00	500.00	450.00	450.00	MHz
MMCM_F _{VCOMIN}	Minimum MMCM VCO Frequency	600.00	600.00	600.00	600.00	MHz
MMCM_F _{VCOMAX}	Maximum MMCM VCO Frequency	1600.00	1440.00	1200.00	1200.00	MHz
MMCM_F _{BANDWIDTH}	Low MMCM Bandwidth at Typical ⁽¹⁾	1.00	1.00	1.00	1.00	MHz
	High MMCM Bandwidth at Typical ⁽¹⁾	4.00	4.00	4.00	4.00	MHz
MMCM_T _{STATPHAOFFSET}	Static Phase Offset of the MMCM Outputs ⁽²⁾	0.12	0.12	0.12	0.12	ns
MMCM_T _{OUTJITTER}	MMCM Output Jitter	Note 3				
MMCM_T _{OUTDUTY}	MMCM Output Clock Duty Cycle Precision ⁽⁴⁾	0.20	0.20	0.20	0.25	ns
MMCM_T _{LOCKMAX}	MMCM Maximum Lock Time	100.00	100.00	100.00	100.00	μs
MMCM_F _{OUTMAX}	MMCM Maximum Output Frequency	1066.00	933.00	800.00	800.00	MHz
MMCM_F _{OUTMIN}	MMCM Minimum Output Frequency ⁽⁵⁾⁽⁶⁾	4.69	4.69	4.69	4.69	MHz
MMCM_T _{EXTFDVAR}	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max				
MMCM_RST _{MINPULSE}	Minimum Reset Pulse Width	5.00	5.00	5.00	5.00	ns
MMCM_F _{PFDMAX}	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized	550.00	500.00	450.00	450.00	MHz
	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	300.00	300.00	300.00	300.00	MHz
MMCM_F _{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	10.00	10.00	10.00	10.00	MHz
MMCM_T _{FBDELAY}	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle				
MMCM Switching Characteristics Setup and Hold						
T _{MMCMDCK_PSEN} / T _{MMCMCKD_PSEN}	Setup and Hold of Phase Shift Enable	1.04/0.00	1.04/0.00	1.04/0.00	1.04/0.00	ns
T _{MMCMDCK_PSINCDEC} / T _{MMCMCKD_PSINCDEC}	Setup and Hold of Phase Shift Increment/Decrement	1.04/0.00	1.04/0.00	1.04/0.00	1.04/0.00	ns
T _{MMCMCKO_PSDONE}	Phase Shift Clock-to-Out of PSDONE	0.59	0.68	0.81	0.78	ns
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK						
T _{MMCMDCK_DADDR} / T _{MMCMCKD_DADDR}	DADDR Setup/Hold	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
T _{MMCMDCK_DI} / T _{MMCMCKD_DI}	DI Setup/Hold	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min

Table 42: Clock-Capable Clock Input to Output Delay With MMCM

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> MMCM.							
T _{ICKOFMMCMCC}	Clock-capable clock input and OUTFF <i>with</i> MMCM	XC7K70T	0.95	0.95	0.95	1.74	ns
		XC7K160T	0.96	0.96	0.96	1.78	ns
		XC7K325T	1.00	1.00	1.00	1.82	ns
		XC7K355T	1.00	1.00	1.00	1.78	ns
		XC7K410T	1.00	1.00	1.00	1.82	ns
		XC7K420T	1.07	1.07	1.07	1.82	ns
		XC7K480T	1.07	1.07	1.07	1.82	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 43: Clock-Capable Clock Input to Output Delay With PLL

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> PLL.							
T _{ICKOFPLLCC}	Clock-capable clock input and OUTFF <i>with</i> PLL	XC7K70T	0.84	0.84	0.84	1.45	ns
		XC7K160T	0.89	0.89	0.89	1.54	ns
		XC7K325T	0.89	0.89	0.89	1.54	ns
		XC7K355T	0.89	0.89	0.89	1.50	ns
		XC7K410T	0.89	0.89	0.89	1.54	ns
		XC7K420T	0.96	0.96	0.96	1.54	ns
		XC7K480T	0.96	0.96	0.96	1.54	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Table 44: Pin-to-Pin, Clock-to-Out using BUFIO

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> BUFIO.						
T _{ICKOFCS}	Clock-to-Out of I/O clock for HR I/O banks	4.93	5.52	6.20	6.97	ns
	Clock-to-Out of I/O clock for HP I/O banks	4.85	5.44	6.11	6.90	ns

Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 45: Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾							
T _{PSFD} / T _{PHFD}	Full Delay (Legacy Delay or Default Delay) Global Clock Input and IFF ⁽²⁾ without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks	XC7K70T	2.83/−0.29	2.95/−0.29	3.15/−0.29	4.96/−0.33	ns
		XC7K160T	3.17/−0.35	3.29/−0.35	3.55/−0.35	5.54/−0.49	ns
		XC7K325T	2.83/−0.06	2.94/−0.06	3.15/−0.06	5.18/−0.14	ns
		XC7K355T	3.26/−0.32	3.41/−0.32	3.67/−0.32	5.84/−0.49	ns
		XC7K410T	3.43/−0.34	3.59/−0.34	3.88/−0.34	6.21/−0.54	ns
		XC7K420T	3.37/−0.27	3.48/−0.27	3.76/−0.27	6.00/−0.52	ns
		XC7K480T	3.37/−0.27	3.48/−0.27	3.76/−0.27	6.00/−0.52	ns

Notes:

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input Flip-Flop or Latch
- A Zero "0" Hold Time listing indicates no hold time or a negative hold time.

Table 46: Clock-Capable Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. ⁽¹⁾							
T _{PSMMCMCC} / T _{PHMMCMCC}	No Delay clock-capable clock input and IFF ⁽²⁾ with MMCM	XC7K70T	2.39/−0.22	2.65/−0.22	2.94/−0.22	2.21/−0.44	ns
		XC7K160T	2.49/−0.20	2.77/−0.20	3.07/−0.20	2.38/−0.47	ns
		XC7K325T	2.55/−0.16	2.85/−0.16	3.14/−0.16	2.60/−0.47	ns
		XC7K355T	2.43/−0.16	2.73/−0.16	3.00/−0.16	2.47/−0.43	ns
		XC7K410T	2.55/−0.16	2.84/−0.16	3.14/−0.16	2.58/−0.47	ns
		XC7K420T	2.47/−0.09	2.73/−0.09	3.02/−0.09	2.40/−0.41	ns
		XC7K480T	2.47/−0.09	2.73/−0.09	3.02/−0.09	2.40/−0.41	ns

Notes:

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input Flip-Flop or Latch
- Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 53: GTX Transceiver Performance (Cont'd)

Symbol	Description	Output Divider	Speed Grade								Units
			1.0V						0.9V		
			-3		-2/-2L		-1 ⁽¹⁾		-2L ⁽²⁾		
			Package Type								
			FF	FB	FF	FB	FF	FB	FF	FB	
F _{GQPLL} RANGE2	GTX transceiver QPLL frequency range 2		9.8–12.5		9.8–10.3125		N/A		N/A		GHz

Notes:

1. The -1 speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s.
2. The -2L (0.9V) speed grade requires a 4-byte internal data width for operation above 3.8 Gb/s.
3. Data rates between 8.0 Gb/s and 9.8 Gb/s are not available.
4. For QPLL line rate range 2, the maximum line rate with the divider N set to 66 is 10.3125Gb/s.

Table 54: GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
F _{GTXDRPCLK}	GTXDRPCLK maximum frequency	175.01	175.01	156.25	125.00	MHz

Table 55: GTX Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F _{GCLK}	Reference clock frequency range	-3 speed grade	60	–	700	MHz
		All other speed grades	60	–	670	MHz
T _{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T _{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T _{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

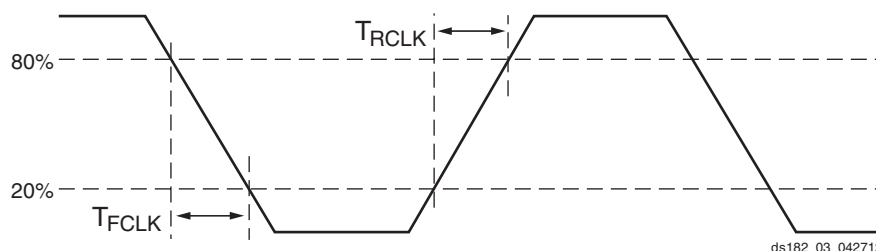


Figure 3: Reference Clock Timing Parameters

GTX Transceiver Protocol Jitter Characteristics

For Table 60 through Table 65, the [UG476: 7 Series FPGAs GTX/GTH Transceiver User Guide](#) contains recommended settings for optimal usage of protocol specific characteristics.

Table 60: Gigabit Ethernet Protocol Characteristics

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 61: XAUI Protocol Characteristics

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T _{TJ})	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 62: PCI Express Protocol Characteristics⁽¹⁾

Standard	Description		Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation						
PCI Express Gen 1	Total transmitter jitter		2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter		5000	–	0.25	UI
PCI Express Gen 3 ⁽²⁾	Total transmitter jitter uncorrelated		8000	–	31.25	ps
	Deterministic transmitter jitter uncorrelated			–	12	ps
PCI Express Receiver High Frequency Jitter Tolerance						
PCI Express Gen 1	Total receiver jitter tolerance		2500	0.65	–	UI
PCI Express Gen 2 ⁽³⁾	Receiver inherent timing error		5000	0.40	–	UI
	Receiver inherent deterministic timing error			0.30	–	UI
PCI Express Gen 3 ⁽²⁾	Receiver sinusoidal jitter tolerance	0.03 MHz–1.0 MHz	8000	1.00	–	UI
		1.0 MHz–10 MHz		Note 4	–	UI
		10 MHz–100 MHz		0.10	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. PCI-SIG 3.0 certification and compliance test boards are currently not available.
3. Using common REFCLK.
4. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20dB/decade.

Table 63: CEI-6G and CEI-11G Protocol Characteristics

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter ⁽¹⁾	4976–6375	CEI-6G-SR	–	0.3	UI
		CEI-6G-LR	–	0.3	UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance ⁽¹⁾	4976–6375	CEI-6G-SR	0.6	–	UI
		CEI-6G-LR	0.95	–	UI
CEI-11G Transmitter Jitter Generation					
Total transmitter jitter ⁽²⁾	9950–11100	CEI-11G-SR	–	0.3	UI
		CEI-11G-LR/MR	–	0.3	UI
CEI-11G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance ⁽²⁾	9950–11100	CEI-11G-SR	0.65	–	UI
		CEI-11G-MR	0.65	–	UI
		CEI-11G-LR	0.825	–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.
2. Tested at line rate of 9950 Mb/s using 155.46875 MHz reference clock and 11100 Mb/s using 173.4375 MHz reference clock.

Table 64: SFP+ Protocol Characteristics

Description	Line Rate (Mb/s)	Min	Max	Units
SFP+ Transmitter Jitter Generation				
Total transmitter jitter	9830.40 ⁽¹⁾	–	0.28	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			
SFP+ Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	9830.40 ⁽¹⁾	0.7	–	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			

Notes:

1. Line rated used for CPRI over SFP+ applications.