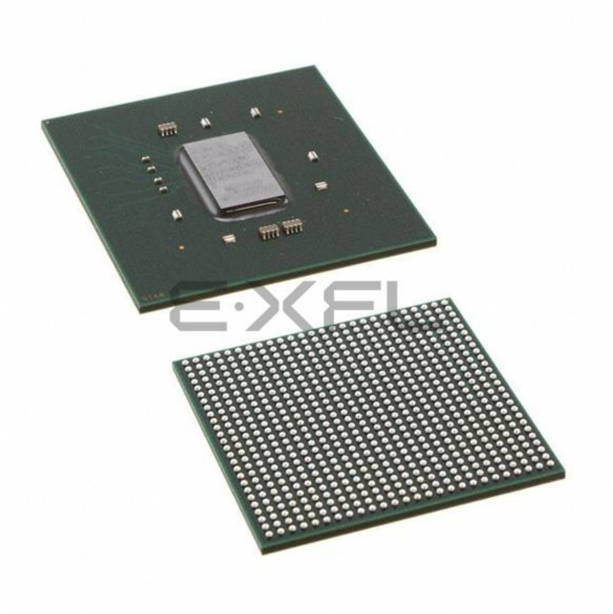
AMD Xilinx - XC7K70T-L2FBG676E Datasheet



Welcome to **E-XFL.COM**

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	5125
Number of Logic Elements/Cells	65600
Total RAM Bits	4976640
Number of I/O	300
Number of Gates	-
Voltage - Supply	0.97V ~ 1.03V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	676-BBGA, FCBGA
Supplier Device Package	676-FCBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7k70t-l2fbg676e

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Table 5: **Maximum Allowed AC Voltage Overshoot and Undershoot for 1.8V HP I/O Banks**[1][2] ***(Cont'd)***

AC Voltage Overshoot	% of UI @–40°C to 100°C	AC Voltage Undershoot	% of UI @–40°C to 100°C
V_{CCO} + 0.80	9.71	–0.80	50.0
V_{CCO} + 0.85	4.51	–0.85	28.4
V_{CCO} + 0.90	2.12	–0.90	12.7
V_{CCO} + 0.95	1.01	–0.95	5.79

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.

Table 6: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC7K70T	241	241	241	187	mA
		XC7K160T	474	474	474	368	mA
		XC7K325T	810	810	810	629	mA
		XC7K355T	993	993	993	771	mA
		XC7K410T	1080	1080	1080	838	mA
		XC7K420T	1313	1313	1313	1019	mA
		XC7K480T	1313	1313	1313	1019	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC7K70T	1	1	1	1	mA
		XC7K160T	1	1	1	1	mA
		XC7K325T	1	1	1	1	mA
		XC7K355T	1	1	1	1	mA
		XC7K410T	1	1	1	1	mA
		XC7K420T	1	1	1	1	mA
		XC7K480T	1	1	1	1	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC7K70T	21	21	21	21	mA
		XC7K160T	40	40	40	40	mA
		XC7K325T	68	68	68	68	mA
		XC7K355T	75	75	75	75	mA
		XC7K410T	85	85	85	85	mA
		XC7K420T	99	99	99	99	mA
		XC7K480T	99	99	99	99	mA
I_{CCAUX_IOQ}	Quiescent V_{CCAUX_IO} supply current	XC7K70T	N/A	N/A	N/A	N/A	mA
		XC7K160T	2	2	2	2	mA
		XC7K325T	2	2	2	2	mA
		XC7K355T	N/A	N/A	N/A	N/A	mA
		XC7K410T	2	2	2	2	mA
		XC7K420T	N/A	N/A	N/A	N/A	mA
		XC7K480T	N/A	N/A	N/A	N/A	mA

Table 6: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current	XC7K70T	6	6	6	6	mA
		XC7K160T	14	14	14	14	mA
		XC7K325T	19	19	19	19	mA
		XC7K355T	31	31	31	31	mA
		XC7K410T	34	34	34	34	mA
		XC7K420T	41	41	41	41	mA
		XC7K480T	41	41	41	41	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the XPower™ Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} have the same recommended voltage levels then they can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTX transceivers is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} – V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to 0.3 x $T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before V_{CCINT} and $V_{MGTAVTT} – V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to 0.3 x T_{VCCINT} (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

Table 17: **Maximum Physical Interface (PHY) Rate for Memory Interfaces (FFG Packages)(1)(2)**

Memory Standard	I/O Bank Type	V_{CCAUX_IO}	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
4:1 Memory Controllers							
DDR3	HP	2.0V	1866	1866	1600	1333	Mb/s
	HP	1.8V	1600	1333	1066	1066	Mb/s
	HR	N/A	1066	1066	800	800	Mb/s
DDR3L	HP	2.0V	1600	1600	1333	1066	Mb/s
	HP	1.8V	1333	1066	800	800	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	2.0V	800	800	800	800	Mb/s
	HP	1.8V	800	800	800	800	Mb/s
	HR	N/A	800	800	800	800	Mb/s
RLDRAM III(3)	HP	2.0V	800	667	667	533	MHz
	HP	1.8V	550	500	450	450	MHz
	HR	N/A	N/A				
2:1 Memory Controllers							
DDR3	HP	2.0V	1066	1066	800	800	Mb/s
	HP	1.8V	1066	1066	800	800	Mb/s
	HR	N/A	1066	1066	800	800	Mb/s
DDR3L	HP	2.0V	1066	1066	800	800	Mb/s
	HP	1.8V	1066	1066	800	800	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	2.0V	800	800	800	800	Mb/s
	HP	1.8V					
	HR	N/A					
QDR II+(4)	HP	2.0V	550	500	450	450	MHz
	HP	1.8V					
	HR	N/A	500	450	400	400	MHz
RLDRAM II	HP	2.0V	533	500	450	450	MHz
	HP	1.8V					
	HR	N/A					
LPDDR2(3)	HP	2.0V	800	800	800	800	Mb/s
	HP	1.8V	800	800	800	800	Mb/s
	HR	N/A	800	667	667	667	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see UG586, *7 Series FPGAs Memory Interface Solutions User Guide*.
2. When using the internal V_{REF}, the maximum data rate is 800 Mb/s (400 MHz).
3. RLDRAM III (BL = 4, BL = 8) and LPDDR2 specifications have not been validated with memory IP.
4. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

Table 18: **Maximum Physical Interface (PHY) Rate for Memory Interfaces (FBG Packages)(1)(2)**

Memory Standard	I/O Bank Type	V_{CCAUX_IO}(3)	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
4:1 Memory Controllers							
DDR3	HP	N/A	1333	1066	800	800	Mb/s
	HR	N/A	1066	800	800	800	Mb/s
DDR3L	HP	N/A	1066	800	667	667	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	N/A	800	800	800	800	Mb/s
	HR	N/A	800	667	667	667	Mb/s
RLDRAM III(4)	HP	N/A	550	500	450	450	MHz
	HR	N/A	N/A				
2:1 Memory Controllers							
DDR3	HP	N/A	1066	1066	800	800	Mb/s
	HR	N/A	1066	800	800	800	Mb/s
DDR3L	HP	N/A	1066	800	667	667	Mb/s
	HR	N/A	800	800	667	667	Mb/s
DDR2	HP	N/A	800	800	800	800	Mb/s
	HR	N/A	800	667	667	667	Mb/s
QDR II+(5)	HP	N/A	550	500	450	450	MHz
	HR	N/A	450	400	350	350	MHz
RLDRAM II	HP	N/A	533	500	450	450	MHz
	HR	N/A					
LPDDR2(4)	HP	N/A	667	667	667	667	Mb/s
	HR	N/A	667	667	533	533	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see UG586, *7 Series FPGAs Memory Interface Solutions User Guide*.
2. When using the internal V_{REF}, the maximum data rate is 800 Mb/s (400 MHz).
3. FBG packages do not have separate V_{CCAUX_IO} supply pins to adjust the pre-driver voltage of the HP I/O banks.
4. RLDRAM III (BL = 4, BL = 8) and LPDDR2 specifications have not been validated with memory IP.
5. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

Table 20: **1.8V IOB High Performance (HP) Switching Characteristics**

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVDS	0.75	0.79	0.92	0.89	1.05	1.17	1.24	1.43	1.68	1.92	2.06	2.04	ns
HSUL_12	0.69	0.72	0.82	0.95	1.65	1.84	2.05	1.80	2.29	2.59	2.87	2.41	ns
DIFF_HSUL_12	0.69	0.72	0.82	0.92	1.65	1.84	2.05	1.47	2.29	2.59	2.87	2.08	ns
HSTL_I_S	0.68	0.72	0.82	0.84	1.15	1.28	1.38	1.46	1.79	2.03	2.20	2.07	ns
HSTL_II_S	0.68	0.72	0.82	0.84	1.05	1.17	1.26	1.44	1.69	1.93	2.08	2.05	ns
HSTL_I_18_S	0.70	0.72	0.82	0.86	1.12	1.24	1.34	1.41	1.75	2.00	2.16	2.02	ns
HSTL_II_18_S	0.70	0.72	0.82	0.86	1.06	1.18	1.26	1.44	1.70	1.94	2.08	2.05	ns
HSTL_I_12_S	0.68	0.72	0.82	0.94	1.14	1.27	1.37	1.43	1.78	2.02	2.20	2.04	ns
HSTL_I_DCI_S	0.68	0.72	0.82	0.78	1.11	1.23	1.33	1.36	1.74	1.99	2.15	1.98	ns
HSTL_II_DCI_S	0.68	0.72	0.82	0.78	1.05	1.17	1.26	1.33	1.69	1.93	2.08	1.94	ns
HSTL_II_T_DCI_S	0.70	0.72	0.82	0.76	1.15	1.28	1.38	1.40	1.78	2.03	2.20	2.01	ns
HSTL_I_DCI_18_S	0.70	0.72	0.82	0.76	1.11	1.23	1.33	1.36	1.74	1.99	2.15	1.98	ns
HSTL_II_DCI_18_S	0.70	0.72	0.82	0.76	1.05	1.16	1.24	1.32	1.69	1.92	2.06	1.93	ns
HSTL_II _T_DCI_18_S	0.70	0.72	0.82	0.76	1.11	1.23	1.33	1.36	1.74	1.99	2.15	1.98	ns
DIFF_HSTL_I_S	0.75	0.79	0.92	0.89	1.15	1.28	1.38	1.47	1.79	2.03	2.20	2.08	ns
DIFF_HSTL_II_S	0.75	0.79	0.92	0.89	1.05	1.17	1.26	1.47	1.69	1.93	2.08	2.08	ns
DIFF_HSTL_I_DCI_S	0.75	0.79	0.92	0.76	1.15	1.28	1.38	1.47	1.78	2.03	2.20	2.08	ns
DIFF_HSTL_II_DCI_S	0.75	0.79	0.92	0.76	1.05	1.17	1.26	1.40	1.69	1.93	2.08	2.01	ns
DIFF_HSTL_I_18_S	0.75	0.79	0.92	0.89	1.12	1.24	1.34	1.46	1.75	2.00	2.16	2.07	ns
DIFF_HSTL_II_18_S	0.75	0.79	0.92	0.89	1.06	1.18	1.26	1.47	1.70	1.94	2.08	2.08	ns
DIFF_HSTL_I_DCI_18_S	0.75	0.79	0.92	0.75	1.11	1.23	1.33	1.46	1.74	1.99	2.15	2.07	ns
DIFF_HSTL_II_DCI_18_S	0.75	0.79	0.92	0.75	1.05	1.16	1.24	1.41	1.69	1.92	2.06	2.02	ns
DIFF_HSTL_II _T_DCI_18_S	0.75	0.79	0.92	0.76	1.11	1.23	1.33	1.46	1.74	1.99	2.15	2.07	ns
HSTL_I_F	0.68	0.72	0.82	0.84	1.02	1.14	1.22	1.26	1.66	1.90	2.04	1.87	ns
HSTL_II_F	0.68	0.72	0.82	0.84	0.97	1.08	1.15	1.29	1.61	1.84	1.97	1.90	ns
HSTL_I_18_F	0.70	0.72	0.82	0.86	1.04	1.16	1.24	1.32	1.68	1.91	2.06	1.93	ns
HSTL_II_18_F	0.70	0.72	0.82	0.86	0.98	1.09	1.16	1.35	1.62	1.85	1.98	1.96	ns
HSTL_I_12_F	0.68	0.72	0.82	0.94	1.02	1.13	1.21	1.26	1.65	1.88	2.03	1.87	ns
HSTL_I_DCI_F	0.68	0.72	0.82	0.78	1.04	1.16	1.24	1.30	1.67	1.91	2.06	1.91	ns
HSTL_II_DCI_F	0.68	0.72	0.82	0.78	0.97	1.08	1.15	1.22	1.61	1.84	1.97	1.83	ns
HSTL_II_T_DCI_F	0.70	0.72	0.82	0.76	1.02	1.14	1.22	1.26	1.66	1.90	2.04	1.87	ns
HSTL_I_DCI_18_F	0.70	0.72	0.82	0.76	1.04	1.16	1.24	1.30	1.67	1.91	2.06	1.91	ns
HSTL_II_DCI_18_F	0.70	0.72	0.82	0.76	0.98	1.09	1.16	1.27	1.61	1.85	1.98	1.88	ns
HSTL_II _T_DCI_18_F	0.70	0.72	0.82	0.76	1.04	1.16	1.24	1.30	1.67	1.91	2.06	1.91	ns
DIFF_HSTL_I_F	0.75	0.79	0.92	0.89	1.02	1.14	1.22	1.35	1.66	1.90	2.04	1.96	ns
DIFF_HSTL_II_F	0.75	0.79	0.92	0.89	0.97	1.08	1.15	1.35	1.61	1.84	1.97	1.96	ns
DIFF_HSTL_I_DCI_F	0.75	0.79	0.92	0.76	1.02	1.14	1.22	1.35	1.66	1.90	2.04	1.96	ns

Table 20: **1.8V IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	1.0V			0.9V	1.0V			0.9V	1.0V			0.9V	
	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	-3	-2/-2L	-1	-2L	
LVCMOS12_F8	0.64	0.67	0.78	0.95	1.27	1.42	1.55	1.41	1.91	2.18	2.37	2.02	ns
LVDCI_18	0.47	0.50	0.60	0.86	1.99	2.15	2.35	2.44	2.62	2.91	3.17	3.05	ns
LVDCI_15	0.59	0.62	0.73	0.87	1.98	2.23	2.58	2.40	2.62	2.99	3.40	3.01	ns
LVDCI_DV2_18	0.47	0.50	0.60	0.87	1.99	2.15	2.34	1.86	2.62	2.90	3.17	2.48	ns
LVDCI_DV2_15	0.59	0.62	0.73	0.87	1.98	2.23	2.58	1.83	2.62	2.99	3.40	2.44	ns
HSLVDCI_18	0.68	0.72	0.82	0.86	1.99	2.15	2.35	2.43	2.62	2.91	3.17	3.04	ns
HSLVDCI_15	0.68	0.72	0.82	0.84	1.98	2.23	2.58	2.27	2.62	2.99	3.40	2.88	ns
SSTL18_I_S	0.68	0.72	0.82	0.86	1.02	1.15	1.24	1.41	1.66	1.90	2.07	2.02	ns
SSTL18_II_S	0.68	0.72	0.82	0.87	1.17	1.29	1.37	1.55	1.81	2.05	2.19	2.16	ns
SSTL18_I_DCI_S	0.68	0.72	0.82	0.76	0.92	1.06	1.17	1.32	1.56	1.82	1.99	1.93	ns
SSTL18_II_DCI_S	0.68	0.72	0.82	0.78	0.88	0.98	1.08	1.26	1.51	1.74	1.90	1.87	ns
SSTL18_II_T_DCI_S	0.68	0.72	0.82	0.78	0.92	1.06	1.17	1.32	1.56	1.82	1.99	1.93	ns
SSTL15_S	0.68	0.72	0.82	0.81	0.94	1.06	1.15	1.32	1.58	1.82	1.97	1.93	ns
SSTL15_DCI_S	0.68	0.72	0.82	0.78	0.94	1.06	1.15	1.30	1.57	1.82	1.97	1.91	ns
SSTL15_T_DCI_S	0.68	0.72	0.82	0.80	0.94	1.06	1.15	1.30	1.57	1.82	1.97	1.91	ns
SSTL135_S	0.69	0.72	0.82	0.89	0.97	1.10	1.19	1.35	1.60	1.85	2.01	1.96	ns
SSTL135_DCI_S	0.69	0.72	0.82	0.84	0.97	1.09	1.19	1.33	1.60	1.85	2.01	1.94	ns
SSTL135_T_DCI_S	0.69	0.72	0.82	0.84	0.97	1.09	1.19	1.33	1.60	1.85	2.01	1.94	ns
SSTL12_S	0.69	0.72	0.82	0.95	0.96	1.09	1.18	1.33	1.60	1.84	2.00	1.94	ns
SSTL12_DCI_S	0.69	0.72	0.82	0.91	1.03	1.17	1.27	1.33	1.66	1.92	2.09	1.94	ns
SSTL12_T_DCI_S	0.69	0.72	0.82	0.91	1.03	1.17	1.27	1.33	1.66	1.92	2.09	1.94	ns
DIFF_SSTL18_I_S	0.75	0.79	0.92	0.89	1.02	1.15	1.24	1.43	1.66	1.90	2.07	2.04	ns
DIFF_SSTL18_II_S	0.75	0.79	0.92	0.89	1.17	1.29	1.37	1.55	1.81	2.05	2.19	2.16	ns
DIFF_SSTL18_I_DCI_S	0.75	0.79	0.92	0.76	0.92	1.06	1.17	1.40	1.56	1.82	1.99	2.01	ns
DIFF_SSTL18_II_DCI_S	0.75	0.79	0.92	0.75	0.88	0.98	1.08	1.33	1.51	1.74	1.90	1.94	ns
DIFF_SSTL18_II_T_DCI_S	0.75	0.79	0.92	0.76	0.92	1.06	1.17	1.40	1.56	1.82	1.99	2.01	ns
DIFF_SSTL15_S	0.68	0.72	0.82	0.89	0.94	1.06	1.15	1.32	1.58	1.82	1.97	1.93	ns
DIFF_SSTL15_DCI_S	0.68	0.72	0.82	0.75	0.94	1.06	1.15	1.30	1.57	1.82	1.97	1.91	ns
DIFF_SSTL15_T_DCI_S	0.68	0.72	0.82	0.76	0.94	1.06	1.15	1.38	1.57	1.82	1.97	1.99	ns
DIFF_SSTL135_S	0.69	0.72	0.82	0.91	0.97	1.10	1.19	1.35	1.60	1.85	2.01	1.96	ns
DIFF_SSTL135_DCI_S	0.69	0.72	0.82	0.76	0.97	1.09	1.19	1.33	1.60	1.85	2.01	1.94	ns
DIFF_SSTL135_T_DCI_S	0.69	0.72	0.82	0.76	0.97	1.09	1.19	1.43	1.60	1.85	2.01	2.04	ns
DIFF_SSTL12_S	0.69	0.72	0.82	0.91	0.96	1.09	1.18	1.33	1.60	1.84	2.00	1.94	ns
DIFF_SSTL12_DCI_S	0.69	0.72	0.82	0.78	1.03	1.17	1.27	1.33	1.66	1.92	2.09	1.94	ns
DIFF_SSTL12_T_DCI_S	0.69	0.72	0.82	0.80	1.03	1.17	1.27	1.41	1.66	1.92	2.09	2.02	ns

Input/Output Logic Switching Characteristics

Table 22: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T_{ICE1CK}/T_{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.42/0.00	0.48/0.00	0.67/0.00	0.56/–0.16	ns
T_{ISRCK}/T_{ICKSR}	SR pin Setup/Hold with respect to CLK	0.53/0.01	0.61/0.01	0.99/0.01	0.88/–0.30	ns
$T_{IDOCKE2}/T_{IOCKDE2}$	D pin Setup/Hold with respect to CLK without Delay (HP I/O banks only)	0.01/0.27	0.01/0.29	0.01/0.34	0.01/0.41	ns
$T_{IDOCKDE2}/T_{IOCKDDE2}$	DDLY pin Setup/Hold with respect to CLK (using IDELAY) (HP I/O banks only)	0.01/0.27	0.02/0.29	0.02/0.34	0.01/0.41	ns
$T_{IDOCKE3}/T_{IOCKDE3}$	D pin Setup/Hold with respect to CLK without Delay (HR I/O banks only)	0.01/0.27	0.01/0.29	0.01/0.34	0.01/0.41	ns
$T_{IDOCKDE3}/T_{IOCKDDE3}$	DDLY pin Setup/Hold with respect to CLK (using IDELAY) (HR I/O banks only)	0.01/0.27	0.02/0.29	0.02/0.34	0.01/0.41	ns
Combinatorial						
T_{IDIE2}	D pin to O pin propagation delay, no Delay (HP I/O banks only)	0.09	0.10	0.12	0.14	ns
T_{IDIDE2}	DDLY pin to O pin propagation delay (using IDELAY) (HP I/O banks only)	0.10	0.11	0.13	0.15	ns
T_{IDIE3}	D pin to O pin propagation delay, no Delay (HR I/O banks only)	0.09	0.10	0.12	0.14	ns
T_{IDIDE3}	DDLY pin to O pin propagation delay (using IDELAY) (HR I/O banks only)	0.10	0.11	0.13	0.15	ns
Sequential Delays						
T_{IDLOE2}	D pin to Q1 pin using flip-flop as a latch without Delay (HP I/O banks only)	0.36	0.39	0.45	0.54	ns
$T_{IDLODE2}$	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) (HP I/O banks only)	0.36	0.39	0.45	0.55	ns
T_{IDLOE3}	D pin to Q1 pin using flip-flop as a latch without Delay (HR I/O banks only)	0.36	0.39	0.45	0.54	ns
$T_{IDLODE3}$	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) (HR I/O banks only)	0.36	0.39	0.45	0.55	ns
T_{ICKQ}	CLK to Q outputs	0.47	0.50	0.58	0.71	ns
$T_{RQ\_ILOGICE2}$	SR pin to OQ/TQ out (HP I/O banks only)	0.84	0.94	1.16	1.32	ns
$T_{GSRQ\_ILOGICE2}$	Global Set/Reset to Q outputs (HP I/O banks only)	7.60	7.60	10.51	11.39	ns
$T_{RQ\_ILOGICE3}$	SR pin to OQ/TQ out (HR I/O banks only)	0.84	0.94	1.16	1.32	ns
$T_{GSRQ\_ILOGICE3}$	Global Set/Reset to Q outputs (HR I/O banks only)	7.60	7.60	10.51	11.39	ns
Set/Reset						
$T_{RPW\_ILOGICE2}$	Minimum Pulse Width, SR inputs (HP I/O banks only)	0.54	0.63	0.63	0.68	ns, Min
$T_{RPW\_ILOGICE3}$	Minimum Pulse Width, SR inputs (HR I/O banks only)	0.54	0.63	0.63	0.68	ns, Min

Table 23: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T_{ODCK}/T_{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.45/–0.13	0.50/–0.13	0.58/–0.13	0.79/–0.18	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	0.35/–0.10	ns
T_{OSRCK}/T_{OCKSR}	SR pin Setup/Hold with respect to CLK	0.32/0.18	0.38/0.18	0.70/0.18	0.62/–0.04	ns
T_{OTCK}/T_{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.49/–0.16	0.56/–0.16	0.68/–0.16	0.67/–0.18	ns
T_{OTCECK}/T_{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	0.31/–0.10	ns
Combinatorial						
T_{ODQ}	D1 to OQ out or T1 to TQ out	0.73	0.81	0.97	1.18	ns
Sequential Delays						
T_{OCKQ}	CLK to OQ/TQ out	0.41	0.43	0.49	0.63	ns
$T_{RQ\_OLOGICE2}$	SR pin to OQ/TQ out (HP I/O banks only)	0.63	0.70	0.83	1.12	ns
$T_{GSRQ\_OLOGICE2}$	Global Set/Reset to Q outputs (HP I/O banks only)	7.60	7.60	10.51	11.39	ns
$T_{RQ\_OLOGICE3}$	SR pin to OQ/TQ out (HR I/O banks only)	0.63	0.70	0.83	1.12	ns
$T_{GSRQ\_OLOGICE3}$	Global Set/Reset to Q outputs (HR I/O banks only)	7.60	7.60	10.51	11.39	ns
Set/Reset						
$T_{RPW\_OLOGICE2}$	Minimum Pulse Width, SR inputs (HP I/O banks only)	0.54	0.54	0.63	0.68	ns, Min
$T_{RPW\_OLOGICE3}$	Minimum Pulse Width, SR inputs (HR I/O banks only)	0.54	0.54	0.63	0.68	ns, Min

Output Serializer/Deserializer Switching Characteristics

Table 25: **OSERDES Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Setup/Hold						
T_{OSDCK_D}/T_{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	0.37/0.02	0.40/0.02	0.55/0.02	0.44/–0.24	ns
T_{OSDCK_T}/T_{OSCKD_T}(1)	T input Setup/Hold with respect to CLK	0.49/–0.15	0.56/–0.15	0.68/–0.15	0.67/–0.25	ns
$T_{OSDCK\_T2}/T_{OSCKD\_T2}$(1)	T input Setup/Hold with respect to CLKDIV	0.27/–0.15	0.30/–0.15	0.34/–0.15	0.46/–0.25	ns
$T_{OSCCK\_OCE}/T_{OSCKC\_OCE}$	OCE input Setup/Hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	0.35/–0.15	ns
T_{OSCCK_S}	SR (Reset) input Setup with respect to CLKDIV	0.41	0.46	0.75	0.70	ns
$T_{OSCCK\_TCE}/T_{OSCKC\_TCE}$	TCE input Setup/Hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	0.31/–0.15	ns
Sequential Delays						
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.35	0.37	0.42	0.54	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.41	0.43	0.49	0.63	ns
Combinatorial						
T_{OSDO_TTQ}	T input to TQ Out	0.73	0.81	0.97	1.18	ns

Notes:

1. T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in TRACE report.

Input/Output Delay Switching Characteristics

Table 26: **Input/Output Delay Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
IDELAYCTRL						
T_{DLYCCO_RDY}	Reset to Ready for IDELAYCTRL	3.22	3.22	3.22	3.22	µs
$F_{IDELAYCTRL\_REF}$	Attribute REFCLK frequency = 200.00(1)	200.00	200.00	200.00	200.00	MHz
	Attribute REFCLK frequency = 300.00(1)	300.00	300.00	N/A	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	±10	MHz
$T_{IDELAYCTRL\_RPW}$	Minimum Reset pulse width	52.00	52.00	52.00	52.00	ns
IDELAY/ODELAY						
$T_{IDELAYRESOLUTION}$	IDELAY/ODELAY chain delay resolution	1/(32 x 2 x F_{REF})				ps
$T_{IDELAYPAT\_JIT}$ and $T_{ODELAYPAT\_JIT}$	Pattern dependent period jitter in delay chain for clock pattern.(2)	0	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(3)	±5	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(4)	±9	±9	±9	±9	ps per tap
$T_{IDELAY\_CLK\_MAX}$/ $T_{ODELAY\_CLK\_MAX}$	Maximum frequency of CLK input to IDELAY/ODELAY	800.00	800.00	710.00	710.00	MHz
T_{IDCCK_CE} / T_{IDCKC_CE}	CE pin Setup/Hold with respect to C for IDELAY	0.11/0.10	0.14/0.12	0.18/0.14	0.14/0.16	ns
T_{ODCCK_CE} / T_{ODCKC_CE}	CE pin Setup/Hold with respect to C for ODELAY	0.14/0.03	0.16/0.04	0.19/0.05	0.28/0.06	ns
T_{IDCCK_INC}/ T_{IDCKC_INC}	INC pin Setup/Hold with respect to C for IDELAY	0.10/0.14	0.12/0.16	0.14/0.20	0.10/0.23	ns
T_{ODCCK_INC}/ T_{ODCKC_INC}	INC pin Setup/Hold with respect to C for ODELAY	0.10/0.07	0.12/0.08	0.13/0.09	0.19/0.16	ns
T_{IDCCK_RST}/ T_{IDCKC_RST}	RST pin Setup/Hold with respect to C for IDELAY	0.13/0.08	0.14/0.10	0.16/0.12	0.22/0.19	ns
T_{ODCCK_RST}/ T_{ODCKC_RST}	RST pin Setup/Hold with respect to C for ODELAY	0.16/0.04	0.19/0.06	0.24/0.08	0.32/0.11	ns
$T_{IDDO\_IDATAIN}$	Propagation delay through IDELAY	Note 5	Note 5	Note 5	Note 5	ps
$T_{ODDO\_ODATAIN}$	Propagation delay through ODELAY	Note 5	Note 5	Note 5	Note 5	ps

Notes:

1. Average Tap Delay at 200 MHz = 78 ps, at 300 MHz = 52 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY/ODELAY tap setting. See TRACE report for actual values.

Table 27: **IO_FIFO Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
IO_FIFO Clock to Out Delays						
T_{OFFCKO_DO}	RDCLK to Q outputs	0.51	0.56	0.63	0.81	ns
T_{CKO_FLAGS}	Clock to IO_FIFO Flags	0.59	0.62	0.81	0.77	ns
Setup/Hold						
T_{CCK_D}/T_{CKC_D}	D inputs to WRCLK	0.43/–0.01	0.47/–0.01	0.53/–0.01	0.76/–0.05	ns
$T_{IFFCCK\_WREN}/T_{IFFCKC\_WREN}$	WREN to WRCLK	0.39/–0.01	0.43/–0.01	0.50/–0.01	0.70/–0.05	ns
$T_{OFFCCK\_RDEN}/T_{OFFCKC\_RDEN}$	RDEN to RDCLK	0.49/0.01	0.53/0.02	0.61/0.02	0.79/–0.02	ns
Minimum Pulse Width						
$T_{PWH\_IO\_FIFO}$	RESET, RDCLK, WRCLK	0.81	0.92	1.08	1.29	ns
$T_{PWL\_IO\_FIFO}$	RESET, RDCLK, WRCLK	0.81	0.92	1.08	1.29	ns
Maximum Frequency						
F_{MAX}	RDCLK and WRCLK	533.05	470.37	400.00	333.33	MHz

Block RAM and FIFO Switching Characteristics

Table 31: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
Block RAM and FIFO Clock-to-Out Delays						
T_{RCKO_DO} and $T_{RCKO\_DO\_REG}$(1)	Clock CLK to DOUT output (without output register)(2)(3)	1.57	1.80	2.08	2.44	ns, Max
	Clock CLK to DOUT output (with output register)(4)(5)	0.54	0.63	0.75	0.86	ns, Max
$T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$	Clock CLK to DOUT output with ECC (without output register)(2)(3)	2.35	2.58	3.26	4.49	ns, Max
	Clock CLK to DOUT output with ECC (with output register)(4)(5)	0.62	0.69	0.80	0.94	ns, Max
$T_{RCKO\_DO\_CASCOUT}$ and $T_{RCKO\_DO\_CASCOUT\_REG}$	Clock CLK to DOUT output with Cascade (without output register)(2)	2.21	2.45	2.80	3.19	ns, Max
	Clock CLK to DOUT output with Cascade (with output register)(4)	0.98	1.08	1.24	1.32	ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs(6)	0.65	0.74	0.89	0.97	ns, Max
$T_{RCKO\_POINTERS}$	Clock CLK to FIFO pointers outputs(7)	0.79	0.87	0.98	1.10	ns, Max
$T_{RCKO\_PARITY\_ECC}$	Clock CLK to ECCPARITY in ECC encode only mode	0.66	0.72	0.80	0.93	ns, Max
$T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$	Clock CLK to BITERR (without output register)	2.17	2.38	3.01	4.15	ns, Max
	Clock CLK to BITERR (with output register)	0.57	0.65	0.76	0.89	ns, Max
$T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$	Clock CLK to RDADDR output with ECC (without output register)	0.64	0.74	0.90	0.98	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.71	0.79	0.92	1.10	ns, Max
Setup and Hold Times Before/After Clock CLK						
T_{RCCK_ADDRA}/T_{RCKC_ADDRA}	ADDR inputs(8)	0.38/0.27	0.42/0.28	0.48/0.31	0.65/0.38	ns, Min
$T_{RDCK\_DI\_WF\_NC}$/ $T_{RCKD\_DI\_WF\_NC}$	Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode(9)	0.49/0.51	0.55/0.53	0.63/0.57	0.78/0.64	ns, Min
$T_{RDCK\_DI\_RF}$/$T_{RCKD\_DI\_RF}$	Data input setup/hold time when block RAM is configured in READ_FIRST mode(9)	0.17/0.25	0.19/0.29	0.21/0.35	0.25/0.32	ns, Min
$T_{RDCK\_DI\_ECC}$/ $T_{RCKD\_DI\_ECC}$	DIN inputs with block RAM ECC in standard mode(9)	0.42/0.37	0.47/0.39	0.53/0.43	0.66/0.46	ns, Min
$T_{RDCK\_DI\_ECCW}$/ $T_{RCKD\_DI\_ECCW}$	DIN inputs with block RAM ECC encode only(9)	0.79/0.37	0.87/0.39	0.99/0.43	1.17/0.41	ns, Min
$T_{RDCK\_DI\_ECC\_FIFO}$/ $T_{RCKD\_DI\_ECC\_FIFO}$	DIN inputs with FIFO ECC in standard mode(9)	0.89/0.47	0.98/0.50	1.12/0.54	1.32/0.65	ns, Min
$T_{RCCK\_INJECTBITERR}$/ $T_{RCKC\_INJECTBITERR}$	Inject single/double bit error in ECC mode	0.49/0.30	0.55/0.31	0.63/0.34	0.78/0.41	ns, Min
T_{RCCK_EN}/T_{RCKC_EN}	Block RAM Enable (EN) input	0.30/0.17	0.33/0.18	0.38/0.20	0.48/0.22	ns, Min
T_{RCCK_REGCE}/T_{RCKC_REGCE}	CE input of output register	0.21/0.13	0.25/0.13	0.31/0.14	0.34/0.16	ns, Min
T_{RCCK_RSTREG}/T_{RCKC_RSTREG}	Synchronous RSTREG input	0.25/0.06	0.27/0.06	0.29/0.06	0.35/0.06	ns, Min

Clock Buffers and Networks

Table 33: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BCCCK_CE}/T_{BCCKC_CE}(1)	CE pins Setup/Hold	0.12/0.30	0.14/0.38	0.26/0.38	0.23/0.40	ns
T_{BCCCK_S}/T_{BCCKC_S}(1)	S pins Setup/Hold	0.12/0.30	0.14/0.38	0.26/0.38	0.23/0.40	ns
T_{BCCKO_O}(2)	BUFGCTRL delay from I0/I1 to O	0.08	0.10	0.12	0.10	ns
Maximum Frequency						
F_{MAX_BUFG}	Global clock tree (BUFG)	741.00	710.00	625.00	560.00	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCKO_O} values.

Table 34: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BIOCKO_O}	Clock to out delay from I to O	1.04	1.14	1.32	1.48	ns
Maximum Frequency						
F_{MAX_BUFIO}	I/O clock tree (BUFIO)	800.00	800.00	710.00	710.00	MHz

Table 35: **Regional Clock Buffer Switching Characteristics (BUFR)**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
T_{BRCKO_O}	Clock to out delay from I to O	0.60	0.65	0.77	1.06	ns
$T_{BRCKO\_O\_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.30	0.32	0.38	0.57	ns
T_{BRDO_O}	Propagation delay from CLR to O	0.71	0.75	0.96	0.93	ns
Maximum Frequency						
F_{MAX_BUFR}(1)	Regional clock tree (BUFR)	600.00	540.00	450.00	450.00	MHz

Notes:

1. The maximum input frequency to the BUFR is the BUFIO F_{MAX} frequency.

MMCM Switching Characteristics

Table 38: **MMCM Specification**

Symbol	Description	Speed Grade				Units
		1.0V			0.9V	
		-3	-2/-2L	-1	-2L	
MMCM_F$_{\text{INMAX}}$	Maximum Input Clock Frequency	1066.00	933.00	800.00	800.00	MHz
MMCM_F$_{\text{INMIN}}$	Minimum Input Clock Frequency	10.00	10.00	10.00	10.00	MHz
MMCM_F$_{\text{INJITTER}}$	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max				
MMCM_F$_{\text{INDUTY}}$	Allowable Input Duty Cycle: 10—49 MHz	25.00	25.00	25.00	25.00	%
	Allowable Input Duty Cycle: 50—199 MHz	30.00	30.00	30.00	30.00	%
	Allowable Input Duty Cycle: 200—399 MHz	35.00	35.00	35.00	35.00	%
	Allowable Input Duty Cycle: 400—499 MHz	40.00	40.00	40.00	40.00	%
	Allowable Input Duty Cycle: >500 MHz	45.00	45.00	45.00	45.00	%
MMCM_F$_{\text{MIN\_PSCLK}}$	Minimum Dynamic Phase Shift Clock Frequency	0.01	0.01	0.01	0.01	MHz
MMCM_F$_{\text{MAX\_PSCLK}}$	Maximum Dynamic Phase Shift Clock Frequency	550.00	500.00	450.00	450.00	MHz
MMCM_F$_{\text{VCOMIN}}$	Minimum MMCM VCO Frequency	600.00	600.00	600.00	600.00	MHz
MMCM_F$_{\text{VCOMAX}}$	Maximum MMCM VCO Frequency	1600.00	1440.00	1200.00	1200.00	MHz
MMCM_F$_{\text{BANDWIDTH}}$	Low MMCM Bandwidth at Typical(1)	1.00	1.00	1.00	1.00	MHz
	High MMCM Bandwidth at Typical(1)	4.00	4.00	4.00	4.00	MHz
MMCM_T$_{\text{STATPHAOFFSET}}$	Static Phase Offset of the MMCM Outputs(2)	0.12	0.12	0.12	0.12	ns
MMCM_T$_{\text{OUTJITTER}}$	MMCM Output Jitter	Note 3				
MMCM_T$_{\text{OUTDUTY}}$	MMCM Output Clock Duty Cycle Precision(4)	0.20	0.20	0.20	0.25	ns
MMCM_T$_{\text{LOCKMAX}}$	MMCM Maximum Lock Time	100.00	100.00	100.00	100.00	µs
MMCM_F$_{\text{OUTMAX}}$	MMCM Maximum Output Frequency	1066.00	933.00	800.00	800.00	MHz
MMCM_F$_{\text{OUTMIN}}$	MMCM Minimum Output Frequency(5)(6)	4.69	4.69	4.69	4.69	MHz
MMCM_T$_{\text{EXTFDVAR}}$	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max				
MMCM_RST$_{\text{MINPULSE}}$	Minimum Reset Pulse Width	5.00	5.00	5.00	5.00	ns
MMCM_F$_{\text{PFDMAX}}$	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized	550.00	500.00	450.00	450.00	MHz
	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	300.00	300.00	300.00	300.00	MHz
MMCM_F$_{\text{PFDMIN}}$	Minimum Frequency at the Phase Frequency Detector	10.00	10.00	10.00	10.00	MHz
MMCM_T$_{\text{FBDELAY}}$	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle				
MMCM Switching Characteristics Setup and Hold						
$T_{\text{MMCMDCK\_PSEN}}$/ $T_{\text{MMCMCKD\_PSEN}}$	Setup and Hold of Phase Shift Enable	1.04/0.00	1.04/0.00	1.04/0.00	1.04/0.00	ns
$T_{\text{MMCMDCK\_PSINCDEC}}$/ $T_{\text{MMCMCKD\_PSINCDEC}}$	Setup and Hold of Phase Shift Increment/Decrement	1.04/0.00	1.04/0.00	1.04/0.00	1.04/0.00	ns
$T_{\text{MMCMCKO\_PSDONE}}$	Phase Shift Clock-to-Out of PSDONE	0.59	0.68	0.81	0.78	ns
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK						
$T_{\text{MMCMDCK\_DADDR}}$/ $T_{\text{MMCMCKD\_DADDR}}$	DADDR Setup/Hold	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min
$T_{\text{MMCMDCK\_DI}}$/ $T_{\text{MMCMCKD\_DI}}$	DI Setup/Hold	1.25/0.15	1.40/0.15	1.63/0.15	1.43/0.00	ns, Min

Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 40: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL.							
T_{ICKOF}	Clock-capable clock input and OUTFF *without* MMCM/PLL (near clock region)	XC7K70T	4.98	5.49	6.17	7.04	ns
		XC7K160T	5.23	5.77	6.48	7.38	ns
		XC7K325T	5.72	6.31	7.09	8.07	ns
		XC7K355T	5.34	5.87	6.57	7.51	ns
		XC7K410T	5.84	6.44	7.22	8.21	ns
		XC7K420T	5.50	6.04	6.77	7.73	ns
		XC7K480T	5.50	6.04	6.77	7.73	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 41: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)**

Symbol	Description	Device	Speed Grade				Units
			1.0V			0.9V	
			-3	-2/-2L	-1	-2L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL.							
$T_{ICKOFFAR}$	Clock-capable clock input and OUTFF *without* MMCM/PLL (far clock region)	XC7K70T	5.29	5.83	6.55	7.47	ns
		XC7K160T	5.84	6.45	7.24	8.24	ns
		XC7K325T	6.33	6.99	7.84	8.92	ns
		XC7K355T	5.95	6.55	7.32	8.36	ns
		XC7K410T	6.45	7.12	7.97	9.07	ns
		XC7K420T	6.41	7.06	7.90	9.01	ns
		XC7K480T	6.41	7.06	7.90	9.01	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

GTX Transceiver Specifications

GTX Transceiver DC Input and Output Levels

Table 51 summarizes the DC output specifications of the GTX transceivers in Kintex-7 FPGAs. Consult UG476: *7 Series FPGAs GTX/GTH Transceiver User Guide* for further details.

Table 51: **GTX Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPOUT}	Differential peak-to-peak output voltage(1)	Transmitter output swing is set to maximum setting	–	–	1000	mV
$V_{CMOUTDC}$	DC common mode output voltage.	Equation based	$V_{MGTAVTT} – DV_{PPOUT}/4$			mV
R_{OUT}	Differential output resistance		–	100	–	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	12	ps
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V_{IN}	Absolute input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–200	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–	2/3 $V_{MGTAVTT}$	–	mV
R_{IN}	Differential input resistance		–	100	–	Ω
C_{EXT}	Recommended external AC coupling capacitor(2)		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in UG476: *7 Series FPGAs GTX/GTH Transceiver User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

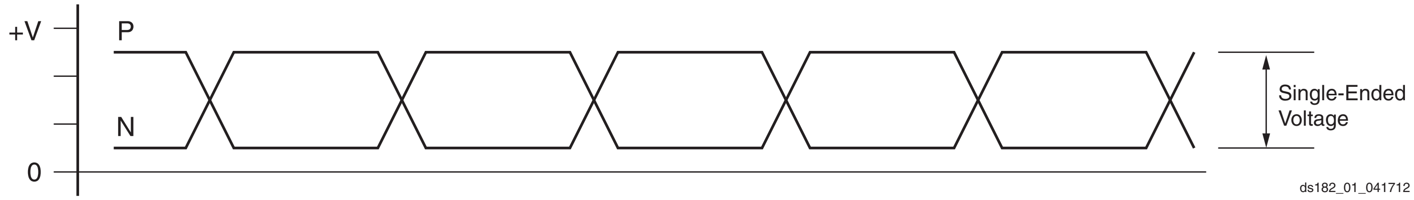


Figure 1: **Single-Ended Peak-to-Peak Voltage**

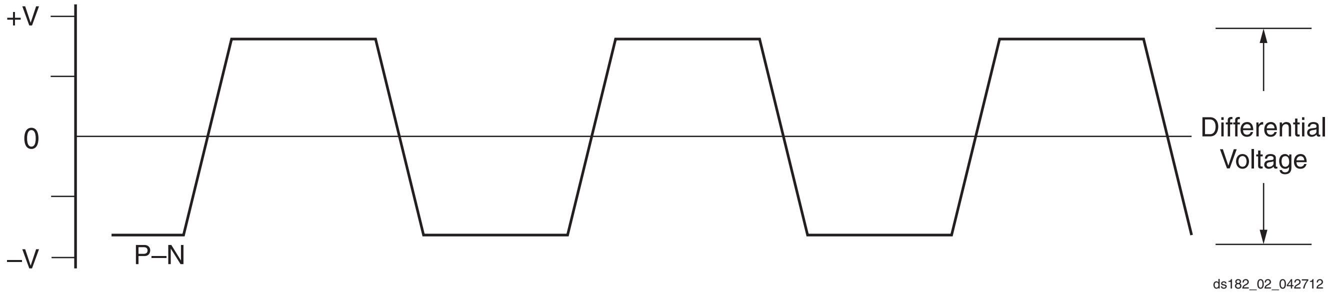


Figure 2: **Differential Peak-to-Peak Voltage**

Table 52 summarizes the DC specifications of the clock input of the GTX transceiver. Consult UG476: *7 Series FPGAs GTX/GTH Transceiver User Guide* for further details.

Table 52: **GTX Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTX Transceiver Switching Characteristics

Consult UG476: *7 Series FPGAs GTX/GTH Transceiver User Guide* for further information.

Table 53: **GTX Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade								Units
			1.0V						0.9V		
			-3		-2/-2L		-1[1]		-2L[2]		
			Package Type								
			FF	FB	FF	FB	FF	FB	FF	FB	
F_{GTXMAX}[3]	Maximum GTX transceiver data rate		12.5	6.6	10.3125	6.6	8.0	6.6	6.6	6.6	Gb/s
F_{GTXMIN}[3]	Minimum GTX transceiver data rate		0.500	0.500	0.500	0.500	0.500	0.500	0.500	0.500	Gb/s
$F_{GTXCRANGE}$	CPLL line rate range	1	3.2–6.6								Gb/s
		2	1.6–3.3								Gb/s
		4	0.8–1.65								Gb/s
		8	0.5–0.825								Gb/s
		16	N/A								Gb/s
$F_{GTXQRANGE1}$	QPLL line rate range 1	1	5.93–8.0	5.93–6.6	5.93–8.0	5.93–6.6	5.93–8.0	5.93–6.6	5.93–6.6		Gb/s
		2	2.965–4.0		2.965–4.0		2.965–4.0		2.965–3.3		Gb/s
		4	1.4825–2.0		1.4825–2.0		1.4825–2.0		1.4825–1.65		Gb/s
		8	0.74125–1.0		0.74125–1.0		0.74125–1.0		0.74125–0.825		Gb/s
		16	N/A		N/A		N/A		N/A		Gb/s
$F_{GTXQRANGE2}$	QPLL line rate range 2[4]	1	9.8–12.5	N/A	9.8–10.3125	N/A	N/A		N/A		Gb/s
		2	4.9–6.25		4.9–5.15625		N/A		N/A		Gb/s
		4	2.45–3.125		2.45–2.578125		N/A		N/A		Gb/s
		8	1.225–1.5625		1.225–1.2890625		N/A		N/A		Gb/s
		16	0.6125–0.78125		0.6125–0.64453125		N/A		N/A		Gb/s
$F_{GCPLLRANGE}$	GTX transceiver CPLL frequency range		1.6–3.3		1.6–3.3		1.6–3.3		1.6–3.3		GHz
$F_{GQPLLRANGE1}$	GTX transceiver QPLL frequency range 1		5.93–8.0		5.93–8.0		5.93–8.0		5.93–6.6		GHz

Table 58: **GTX Transceiver Transmitter Switching Characteristics *(Cont'd)***

Symbol	Description	Condition	Min	Typ	Max	Units
$TJ_{10.3125}$	Total Jitter(2)(4)	10.3125 Gb/s	–	–	0.28	UI
$DJ_{10.3125}$	Deterministic Jitter(2)(4)		–	–	0.17	UI
$TJ_{9.953}$	Total Jitter(2)(4)	9.953 Gb/s	–	–	0.28	UI
$DJ_{9.953}$	Deterministic Jitter(2)(4)		–	–	0.17	UI
$TJ_{9.8}$	Total Jitter(2)(4)	9.8 Gb/s	–	–	0.28	UI
$DJ_{9.8}$	Deterministic Jitter(2)(4)		–	–	0.17	UI
$TJ_{8.0}$	Total Jitter(2)(4)	8.0 Gb/s	–	–	0.30	UI
$DJ_{8.0}$	Deterministic Jitter(2)(4)		–	–	0.15	UI
$TJ_{6.6\_QPLL}$	Total Jitter(2)(4)	6.6 Gb/s	–	–	0.28	UI
$DJ_{6.6\_QPLL}$	Deterministic Jitter(2)(4)		–	–	0.17	UI
$TJ_{6.6\_CPLL}$	Total Jitter(3)(4)	6.6 Gb/s	–	–	0.30	UI
$DJ_{6.6\_CPLL}$	Deterministic Jitter(3)(4)		–	–	0.15	UI
$TJ_{5.0}$	Total Jitter(3)(4)	5.0 Gb/s	–	–	0.30	UI
$DJ_{5.0}$	Deterministic Jitter(3)(4)		–	–	0.15	UI
$TJ_{4.25}$	Total Jitter(3)(4)	4.25 Gb/s	–	–	0.30	UI
$DJ_{4.25}$	Deterministic Jitter(3)(4)		–	–	0.15	UI
$TJ_{3.75}$	Total Jitter(3)(4)	3.75 Gb/s	–	–	0.30	UI
$DJ_{3.75}$	Deterministic Jitter(3)(4)		–	–	0.15	UI
$TJ_{3.2}$	Total Jitter(3)(4)	3.20 Gb/s(5)	–	–	0.2	UI
$DJ_{3.2}$	Deterministic Jitter(3)(4)		–	–	0.1	UI
$TJ_{3.2L}$	Total Jitter(3)(4)	3.20 Gb/s(6)	–	–	0.32	UI
$DJ_{3.2L}$	Deterministic Jitter(3)(4)		–	–	0.16	UI
$TJ_{2.5}$	Total Jitter(3)(4)	2.5 Gb/s(7)	–	–	0.20	UI
$DJ_{2.5}$	Deterministic Jitter(3)(4)		–	–	0.08	UI
$TJ_{1.25}$	Total Jitter(3)(4)	1.25 Gb/s(8)	–	–	0.15	UI
$DJ_{1.25}$	Deterministic Jitter(3)(4)		–	–	0.06	UI
TJ_{500}	Total Jitter(3)(4)	500 Mb/s	–	–	0.1	UI
DJ_{500}	Deterministic Jitter(3)(4)		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to 12 consecutive transmitters (three fully populated GTX Quads).
2. Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
4. All jitter values are based on a bit-error ratio of $1e^{-12}$.
5. CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
6. CPLL frequency at 1.6 GHz and TXOUT_DIV = 1.
7. CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
8. CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.

GTX Transceiver Protocol Jitter Characteristics

For Table 60 through Table 65, the UG476: *7 Series FPGAs GTX/GTH Transceiver User Guide* contains recommended settings for optimal usage of protocol specific characteristics.

Table 60: **Gigabit Ethernet Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 61: **XAUI Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 62: **PCI Express Protocol Characteristics(1)**

Standard	Description		Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation						
PCI Express Gen 1	Total transmitter jitter		2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter		5000	–	0.25	UI
PCI Express Gen 3(2)	Total transmitter jitter uncorrelated		8000	–	31.25	ps
	Deterministic transmitter jitter uncorrelated			–	12	ps
PCI Express Receiver High Frequency Jitter Tolerance						
PCI Express Gen 1	Total receiver jitter tolerance		2500	0.65	–	UI
PCI Express Gen 2(3)	Receiver inherent timing error		5000	0.40	–	UI
	Receiver inherent deterministic timing error			0.30	–	UI
PCI Express Gen 3(2)	Receiver sinusoidal jitter tolerance	0.03 MHz–1.0 MHz	8000	1.00	–	UI
		1.0 MHz–10 MHz		Note 4	–	UI
		10 MHz–100 MHz		0.10	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. PCI-SIG 3.0 certification and compliance test boards are currently not available.
3. Using common REFCLK.
4. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20dB/decade.

Notice of Disclaimer

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials, or to advise you of any corrections or update. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of the Limited Warranties which can be viewed at http://www.xilinx.com/warranty.htm; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in Critical Applications: http://www.xilinx.com/warranty.htm#critapps.

AUTOMOTIVE APPLICATIONS DISCLAIMER

XILINX PRODUCTS ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE, OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS APPLICATIONS RELATED TO: (I) THE DEPLOYMENT OF AIRBAGS, (II) CONTROL OF A VEHICLE, UNLESS THERE IS A FAIL-SAFE OR REDUNDANCY FEATURE (WHICH DOES NOT INCLUDE USE OF SOFTWARE IN THE XILINX DEVICE TO IMPLEMENT THE REDUNDANCY) AND A WARNING SIGNAL UPON FAILURE TO THE OPERATOR, OR (III) USES THAT COULD LEAD TO DEATH OR PERSONAL INJURY. CUSTOMER ASSUMES THE SOLE RISK AND LIABILITY OF ANY USE OF XILINX PRODUCTS IN SUCH APPLICATIONS.