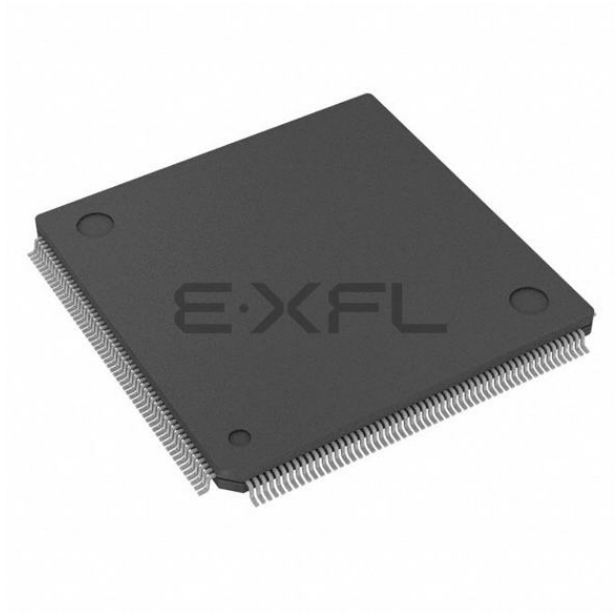
Infineon Technologies - MB91F467MAPMC-GSK5E2 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR60 RISC
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, I²S, LVD, WDT
Number of I/O	175
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	216-LQFP
Supplier Device Package	216-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f467mapmc-gsk5e2

Contents

Pin no.	Pin name	I/O	I/O circuit type*	Function
188	P15_1	I/O	D	General-purpose input/output ports.
	OCU1			Waveform output pin of output compare OCU 1.
	TOT1			Output pin of reload timer RLT 1.
189	P15_2	I/O	D	General-purpose input/output ports.
	OCU2			Waveform output pin of output compare OCU 2.
	TOT2			Output pin of reload timer RLT 2.
190	P15_3	I/O	D	General-purpose input/output ports.
	OCU3			Waveform output pin of output compare OCU 3.
	TOT3			Output pin of reload timer RLT 3.
193	P24_6	I/O	D	General-purpose input/output ports.
	INT6			Request input pin of external interrupt ch.6.
	SDA3			Serial data input/output pin of I^2C 3.
194	P24_7	I/O	D	General-purpose input/output ports.
	INT7			Request input pin of external interrupt ch.7.
	SCL3			Serial clock input/output pin of I^2C 3.
195	P40_0	I/O	C	General-purpose input/output ports.
	SDA4			Serial data input/output pin of I^2C 4.
196	P40_1	I/O	C	General-purpose input/output ports.
	SCL4			Serial clock input/output pin of I^2C 4.
197	P40_2	I/O	C	General-purpose input/output ports.
	SDA5			Serial data input/output pin of I^2C 5.
198	P40_3	I/O	C	General-purpose input/output ports.
	SCL5			Serial clock input/output pin of I^2C 5.
199	P40_4	I/O	C	General-purpose input/output ports.
	SDA6			Serial data input/output pin of I^2C 6.
200	P40_5	I/O	C	General-purpose input/output ports.
	SCL6			Serial clock input/output pin of I^2C 6.
201	P23_4	I/O	D	General-purpose input/output ports.
	INT10			Request input pin of external interrupt ch.10.
202	P23_6	I/O	D	General-purpose input/output ports.
	INT11			Request input pin of external interrupt ch.11.
203	P22_0	I/O	D	General-purpose input/output ports.
	INT12			Request input pin of external interrupt ch.12.
204	P22_1	I/O	D	General-purpose input/output ports.
	INT14			Request input pin of external interrupt ch.14. Exclusive from P22_4.

(Continued)

5. Handling Devices

Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage higher than V_{CC} or less than V_{SS} is applied to an input or output pin or if a voltage exceeding the rating is applied between VCC and VSS pins.
If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Therefore, be very careful not to apply voltages in excess of the absolute maximum ratings.

Handling of unused input pins

If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistor (2 KΩ or more) or enable internal pull up or pull down resistors before setting the global port enable bit.
Unused input and output pins need to leave open at the output state, or treat the same as for the input pin when they are at the input state.

Power supply pins

The MB91460M series has multiple of VCC and VSS pins.
The device is designed such that pins necessary to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. However, all of these pins must be connected externally to the power supply or ground in order to minimize undesired electromagnetic radiation, prevent strobe signal malfunctions due to the rise in ground level, and conform to the total output current rating.
Moreover, connect the current supply source with the VCC and VSS pins of this device at the low impedance.
It is also recommended that a ceramic capacitor of around 0.1 µF be connected as a bypass capacitor between the VCC and VSS pins at a location close to the device.
This series has a built-in regulator. Connect a bypass capacitor of 4.7 µF to C_1 and C_2 pins for the regulator.

Crystal oscillator circuit

Noise in proximity to the X0 (X0A) and X1 (X1A) pins can cause the device to operate abnormally. Printed circuit boards should be designed so that the X0 (X0A) and X1 (X1A) pins, and crystal oscillator (or ceramic oscillator), as well as bypass capacitors connected to ground, are placed as close together as possible. When the signal wires for transmitting from X0 and X1 pins are pulled along, use the circuit with them shielded on board. Be careful especially when a pin next to X0 pin is used.
It is recommended that the printed circuit board layout be designed such that the X0 and X1 pins or X0A and X1A pins are surrounded by ground plane for the stable operation. Sub clock is also needed when dual clock product is used as single clock product.
Please request the oscillator manufacturer to evaluate the oscillational characteristics of the crystal and this device.

Treatment of NC and OPEN pins

Pins marked as NC and OPEN must be left open-circuit.

Mode pins (MD0 to MD4)

These pins should be connected directly to Vcc or Vss. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and Vcc or Vss on the printed circuit board as possible and connect them with low impedance.
Especially, MD3 must be directly connected to Vss with 0 Ω.

Operation at Start-up

Be sure to execute the setting initialized reset (INIT) with INITX pin immediately after start-up.
Hold the “L” level input to the INITX pin during the stabilization wait time immediately after the power on to ensure the stabilization wait time as required by the oscillator circuit (the stabilization wait time is initialized to the minimum value when INIT is asserted to reset using the INITX pin).

Note on oscillator input at power-on

At power-on, ensure that the clock is input until the oscillator stabilization wait time has elapsed.

Notes on operating in PLL clock mode

If the oscillator is disconnected or the clock input stops when the PLL clock is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit of the PLL. However, this self-running operation cannot be guaranteed.

Notes on PS register

As the PS register is processed in advance by some instructions, when the debugger is being used, the exception handling described below may result in execution breaking in an interrupt handling routine or the displayed values of the flags in the PS register being updated.
As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event, the operation before and after the EIT always proceeds according to specification.

■ The following behavior may occur if any of the following occurs in the instruction immediately after a DIV0U/DIV0S instruction:

- a user interrupt is accepted;
- single-step execution is performed;
- or execution breaks due to a data event or from the emulator menu.

1. D0 and D1 flags are updated in advance.
2. An EIT handling routine (user interrupt or emulator) is executed.
3. Upon returning from the EIT, the DIV0U/DIV0S instruction is executed and the D0 and D1 flags are updated to the same values as those in 1).

■ The following behavior occurs when an ORCCR, STILM, MOV Ri or PS instruction is executed to enable a user interrupt while that interrupt is in the active state.

4. The PS register is updated in advance.
5. An EIT handling routine (user interrupt) is executed.
6. Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in 4.

Watchdog timer

The watchdog timer built in this model monitors a program and resets the CPU if the reset defer function is not executed within a certain period of time or the program runs out of control. Once the function of the watchdog timer is enabled, the watchdog timer keeps on operating program until it resets the CPU.
As an exception, the watchdog timer defers a reset automatically under the condition in which the CPU stops executing the program. For those conditions to which this exception applies, see “Chapter 20 Watch dog timer in Hardware manual”.

Frequency fluctuation

This chip which contains PLL can switch divide-by-two external clock to PLL output fast clock. The clock gear function which is built in this model prevents consumption power from increasing rapidly at this time.

Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise.
Consider receiving of wrong data when designing the system. For example, apply a checksum to detect an error. If an error is detected, retransmit the data.

Write to registers which include a status flag (1)

Be careful not to accidentally clear a status flag, when writing into registers which include a status flag (especially the interrupt request flag).
Take notice that a flag of a status bit is not cleared and the control bit is set to the expected value at writing.
When overwriting the control bit structured by multiple bits simultaneously, it is not possible to use the bit manipulation instruction. As a result, it is necessary to access data with usual byte/half word/word when writing to both a control bit and a status flag simultaneously. At this time, be careful not to accidentally clear other bits (bits in a status flag).

Almost all registers shown below include multiple control bits and status flags.

- TBCR
- OSCR
- TCCS0, TCCS1
- ICS01
- TMCSR0, TMCSR1, TMCSR2, TMCSR3
- PCN0, PCN1, PCN2, PCN3, PCN4, PCN5
- ADCSL0, ADCSL1

Note: It is not necessary to take special care when overwriting a single bit by the bit manipulation instruction.

6. Notes On Debugger

Execution of the RETI Command

If an interrupt occurs frequently during step execution, the corresponding interrupt handling routine is executed repeatedly after step execution. As the result of that, the main routine and low-interrupt-level programs will not be executed.
Do not perform the step execution of RETI instruction to prevent this issue.
Disable the corresponding interrupt and execute debugger when the corresponding interrupt routine no longer needs debugging.

Operand break

Do not set the access to the areas containing the address of system stack pointer as a target of data event break.

Flash security

DSU4 will not be available due to security issues when Flash security is used.

Shutdown mode

It is impossible to execute debugger in the shutdown mode.

8. Embedded Program/Data Memory (Flash)

8.1 Flash features

- MB91F467MA: 1088 Kbytes (16 × 64 Kbytes + 8 × 8 Kbytes = 8.7 Mbits)
- Programmable wait state for read/write access
- Flash and Boot security with security vector at $0014:8000_H$ to $0014:800F_H$
- Basic specification: Same as MBM29LV400TC (except size and part of sector configuration)

8.2 Operation modes

1. 64-bit CPU mode
   - CPU reads and executes programs in word (32-bit) length units.
   - Flash writing is not possible.
   - Actual Flash Memory access is performed in d-word (64-bit) length units.
2. 32-bit CPU mode :
   - Actual Flash Memory access is performed in word (32-bit) length units.
3. 16-bit CPU mode :
   - CPU reads and writes in half-word (16-bit) length units.
   - Program execution from the Flash is not possible.
   - Actual Flash Memory access is performed in half-word (16-bit) length units.

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000090_H to $0000CC_H$	Reserved				Reserved
$0000D0_H$	IBCR0 [R/W] 00000000	IBSR0 [R] 00000000	ITBAH0 [R/W] ------00	ITBAL0 [R/W] 00000000	I^2C 0
$0000D4_H$	ITMKH0 [R/W] 00----11	ITMKL0 [R/W] 11111111	ISMK0 [R/W] 01111111	ISBA0 [R/W] -0000000	
$0000D8_H$	Reserved	IDAR0 [R/W] 00000000	ICCR0 [R/W] -0011111	Reserved	
$0000DC_H$	IBCR1 [R/W] 00000000	IBSR1 [R] 00000000	ITBAH1 [R/W] ------00	ITBAL1 [R/W] 00000000	I^2C 1
$0000E0_H$	ITMKH1 [R/W] 00----11	ITMKL1 [R/W] 11111111	ISMK1 [R/W] 01111111	ISBA1 [R/W] -0000000	
$0000E4_H$	Reserved	IDAR1 [R/W] 00000000	ICCR1 [R/W] -0011111	Reserved	
$0000E8_H$ to $0000FC_H$	Reserved				Reserved
000100_H	GCN10 [R/W] 00110010 00010000		Reserved	GCN20 [R/W] ----0000	PPG Control 0-3
000104_H	GCN11 [R/W] 00110010 00010000		Reserved	GCN21 [R/W] ----0000	PPG Control 4-7
000108_H, $00010C_H$	Reserved				Reserved
000110_H	PTMR00 [R] 11111111 11111111		PCSR00 [W] XXXXXXXX XXXXXXXX		PPG 0
000114_H	PDUT00 [W] XXXXXXXX XXXXXXXX		PCNH00 [R/W] 0000000-	PCNL00 [R/W] 000000-0	
000118_H	PTMR01 [R] 11111111 11111111		PCSR01 [W] XXXXXXXX XXXXXXXX		PPG 1
$00011C_H$	PDUT01 [W] XXXXXXXX XXXXXXXX		PCNH01 [R/W] 0000000-	PCNL01 [R/W] 000000-0	
000120_H	PTMR02 [R] 11111111 11111111		PCSR02 [W] XXXXXXXX XXXXXXXX		PPG 2
000124_H	PDUT02 [W] XXXXXXXX XXXXXXXX		PCNH02 [R/W] 0000000-	PCNL02 [R/W] 000000-0	
000128_H	PTMR03 [R] 11111111 11111111		PCSR03 [W] XXXXXXXX XXXXXXXX		PPG 3
$00012C_H$	PDUT03 [W] XXXXXXXX XXXXXXXX		PCNH03 [R/W] 0000000-	PCNL03 [R/W] 000000-0	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$000D00_H$	PDRD00 [R] XXXXXXXX	PDRD01 [R] XXXXXXXX	Reserved		Port Data Direct Read Register [R-bus]
$000D04_H$	Reserved	PDRD05 [R] XXXXXXXX	PDRD06 [R] XXXXXXXX	PDRD07 [R] XXXXXXXX	
$000D08_H$	PDRD08 [R] XXXX--XX	PDRD09 [R] -XXXXXXX	PDRD10 [R] -XXXXXXX	PDRD11 [R] ------XX	
$000D0C_H$	Reserved	PDRD13 [R] -----XXX	PDRD14 [R] ----XXXX	PDRD15 [R] XX--XXXX	
$000D10_H$	PDRD16 [R] XXXXXXXX	PDRD17 [R] XXXXXXXX	PDRD18 [R] -XXX-XXX	PDRD19 [R] -XXX-XXX	
$000D14_H$	PDRD20 [R] -XXX-XXX	PDRD21 [R] -XXX-XXX	PDRD22 [R] XXXXXXXX	PDRD23 [R] -X-XXXXX	
$000D18_H$	PDRD24 [R] XXXXXXXX	Reserved			
$000D1C_H$	PDRD28 [R] ----XXXX	PDRD29 [R] XXXXXXXX	Reserved		
$000D20_H$	Reserved			PDRD35 [R] -----XXX	
$000D24_H$	PDRD36 [R] XXX-XX--	Reserved	PDRD38 [R] ------XX	PDRD39 [R] XXXXXXXX	
$000D28_H$	PDRD40 [R] XXXXXXXX	Reserved			
$000D2C_H$ to $000D3C_H$	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$000D80_H$	PFR00 [R/W] 11111111	PFR01 [R/W] 11111111	Reserved		Port Function Register [R-bus]
$000D84_H$	Reserved	PFR05 [R/W] 11111111	PFR06 [R/W] 11111111	PFR07 [R/W] 11111111	
$000D88_H$	PFR08 [R/W] 1111--11	PFR09 [R/W] -1111111	PFR10 [R/W] -1111111	PFR11 [R/W] ------00	
$000D8C_H$	Reserved	PFR13 [R/W] -----000	PFR14 [R/W] ----0000	PFR15 [R/W] 00--0000	
$000D90_H$	PFR16 [R/W] 0-------	PFR17 [R/W] 00000000	PFR18 [R/W] -000-000	PFR19 [R/W] -000-000	
$000D94_H$	PFR20 [R/W] -000-000	PFR21 [R/W] -000-000	PFR22 [R/W] 00000000	PFR23 [R/W] -0-00000	
$000D98_H$	PFR24 [R/W] 00000000	Reserved			
$000D9C_H$	PFR28 [R/W] ----0000	PFR29 [R/W] 00000000	Reserved		
$000DA0_H$	Reserved			PFR35 [R/W] -----000	
$000DA4_H$	PFR36 [R/W] 000-00--	Reserved	PFR38 [R/W] ------00	PFR39 [R/W] 00000000	
$000DA8_H$	PFR40 [R/W] 00000000	Reserved			
$000DAC_H$ to $000DBC_H$	Reserved				Reserved
$000DC0_H$, $000DC4_H$	Reserved				Port Expansion Function Register [R-bus]
$000DC8_H$	Reserved		EPFR10 [R/W] --00---0	Reserved	
$000DCC_H$	Reserved	EPFR13 [R/W] ----0--	EPFR14 [R/W] ----0000	EPFR15 [R/W] ----0000	
$000DD0_H$	EPFR16 [R/W] 0-------	Reserved	EPFR18 [R/W] -00--00-	EPFR19 [R/W] -0---0--	
$000DD4_H$	EPFR20 [R/W] -0---0--	EPFR21 [R/W] -0---0--	EPFR22 [R/W] ----0-0-	Reserved	
$000DD8_H$, $000DDC_H$	Reserved				
$000DE0_H$	Reserved			EPFR35 [R/W] -----000	
$000DE4_H$ to $000DFC_H$	Reserved				Reserved

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
006034_H to $00603C_H$	Reserved				MediaLB
006040_H	CECR0 [R/W] 0000000- 00000000 00000000 00000000				
006044_H	CSCR0 [R/W] 10------ ----0000 00000000 00000000				
006048_H	CCBCR0 [R] 00000000 00000000 00000000 00000000				
$00604C_H$	CNBCR0 [R/W] 00000000 00000000 00000000 00000000				
006050_H	CECR1 [R/W] 0000000- 00000000 00000000 00000000				
006054_H	CSCR1 [R/W] 10------ ----0000 00000000 00000000				
006058_H	CCBCR1 [R] 00000000 00000000 00000000 00000000				
$00605C_H$	CNBCR1 [R/W] 00000000 00000000 00000000 00000000				
006060_H	CECR2 [R/W] 0000000- 00000000 00000000 00000000				
006064_H	CSCR2 [R/W] 10------ ----0000 00000000 00000000				
006068_H	CCBCR2 [R] 00000000 00000000 00000000 00000000				
$00606C_H$	CNBCR2 [R/W] 00000000 00000000 00000000 00000000				
006070_H	CECR3 [R/W] 0000000- 00000000 00000000 00000000				
006074_H	CSCR3 [R/W] 10------ ----0000 00000000 00000000				
006078_H	CCBCR3 [R] 00000000 00000000 00000000 00000000				
$00607C_H$	CNBCR3 [R/W] 00000000 00000000 00000000 00000000				

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$00C100_H$	CTRLR1 [R/W] 00000000 00000001		STATR1 [R/W] 00000000 00000000		CAN1 Control Register
$00C104_H$	ERRCNT1 [R] 00000000 00000000		BTR1 [R/W] 00100011 00000001		
$00C108_H$	INTR1 [R] 00000000 00000000		TESTR1 [R/W] 00000000 X0000000		
$00C10C_H$	BRPE1 [R/W] 00000000 00000000		CBSYNC1 [R] XXXXXXXX XXXXXXXX		
$00C110_H$	IF1CREQ1 [R/W] 00000000 00000001		IF1CMSK1 [R/W] 00000000 00000000		CAN1 IF 1 Register
$00C114_H$	IF1MSK21 [R/W] 11111111 11111111		IF1MSK11 [R/W] 11111111 11111111		
$00C118_H$	IF1ARB21 [R/W] 00000000 00000000		IF1ARB11 [R/W] 00000000 00000000		
$00C11C_H$	IF1MCTR1 [R/W] 00000000 00000000		Reserved		
$00C120_H$	IF1DTA11 [R/W] 00000000 00000000		IF1DTA21 [R/W] 00000000 00000000		
$00C124_H$	IF1DTB11 [R/W] 00000000 00000000		IF1DTB21 [R/W] 00000000 00000000		
$00C128_H$, $00C12C_H$	Reserved				
$00C130_H$	IF1DTA21 [R/W] 00000000 00000000		IF1DTA11 [R/W] 00000000 00000000		
$00C134_H$	IF1DTB21 [R/W] 00000000 00000000		IF1DTB11 [R/W] 00000000 00000000		
$00C138_H$, $00C13C_H$	Reserved				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$00C1B8_H$ to $00C1FC_H$	Reserved				CAN1 Status Flags
$00C200_H$ to $00EFFC_H$	Reserved				Reserved
$00F000_H$	BCTRL [R/W] -------- -------- 11111100 00000000				EDSU / MPU
$00F004_H$	BSTAT [R/W] -------- -----000 00000000 10--0000				
$00F008_H$	BIAC [R] -------- -------- 00000000 00000000				
$00F00C_H$	BOAC [R] -------- -------- 00000000 00000000				
$00F010_H$	BIRQ [R/W] -------- -------- 00000000 00000000				
$00F014_H$ to $00F01C_H$	Reserved				
$00F020_H$	BCR0 [R/W] -------- 00000000 00000000 00000000				
$00F024_H$	BCR1 [R/W] -------- 00000000 00000000 00000000				
$00F028_H$	BCR2 [R/W] -------- 00000000 00000000 00000000				
$00F02C_H$	BCR3 [R/W] -------- 00000000 00000000 00000000				
$00F030_H$ to $00F07C_H$	Reserved				

(Continued)

Interrupt	Interrupt number		Interrupt level*1		Interrupt vector*2		RN
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
System reserved *3	64	40_H	(ICR24)	(458_H)	$2FC_H$	$000FFEFC_H$	
System reserved *3	65	41_H			$2F8_H$	$000FFEF8_H$	
LIN-USART (FIFO) 4 RX	66	42_H	ICR25	459_H	$2F4_H$	$000FFEF4_H$	10, 56
LIN-USART (FIFO) 4 TX	67	43_H			$2F0_H$	$000FFEF0_H$	11, 57
LIN-USART (FIFO) 5 RX	68	44_H	ICR26	$45A_H$	$2EC_H$	$000FFEEC_H$	12, 58
LIN-USART (FIFO) 5 TX	69	45_H			$2E8_H$	$000FFEE8_H$	13, 59
LIN-USART (FIFO) 6 RX	70	46_H	ICR27	$45B_H$	$2E4_H$	$000FFEE4_H$	60
LIN-USART (FIFO) 6 TX	71	47_H			$2E0_H$	$000FFEE0_H$	61
LIN-USART (FIFO) 7 RX	72	48_H	ICR28	$45C_H$	$2DC_H$	$000FFEDC_H$	62
LIN-USART (FIFO) 7 TX	73	49_H			$2D8_H$	$000FFED8_H$	63
I^2C 0 / I^2C 2	74	$4A_H$	ICR29	$45D_H$	$2D4_H$	$000FFED4_H$	
I^2C 1 / I^2C 3	75	$4B_H$			$2D0_H$	$000FFED0_H$	
LIN-USART (LIN) 8 RX	76	$4C_H$	ICR30	$45E_H$	$2CC_H$	$000FFECC_H$	64
LIN-USART (LIN) 8 TX	77	$4D_H$			$2C8_H$	$000FFEC8_H$	65
I^2C 4 / I^2C 6	78	$4E_H$	ICR31	$45F_H$	$2C4_H$	$000FFEC4_H$	
I^2C 5 / I^2C 7	79	$4F_H$			$2C0_H$	$000FFEC0_H$	
Reserved	80	50_H	ICR32	460_H	$2BC_H$	$000FFEBC_H$	
Reserved	81	51_H			$2B8_H$	$000FFEB8_H$	
FIFO buffer	82	52_H	ICR33	461_H	$2B4_H$	$000FFEB4_H$	
Reserved	83	53_H			$2B0_H$	$000FFEB0_H$	
Reserved	84	54_H	ICR34	462_H	$2AC_H$	$000FFEAC_H$	
Reserved	85	55_H			$2A8_H$	$000FFEA8_H$	
Reserved	86	56_H	ICR35	463_H	$2A4_H$	$000FFEA4_H$	
Reserved	87	57_H			$2A0_H$	$000FFEA0_H$	
MediaLB	88	58_H	ICR36	464_H	$29C_H$	$000FFE9C_H$	
I^2S ERROR	89	59_H			298_H	$000FFE98_H$	
I^2S EVEN	90	$5A_H$	ICR37	465_H	294_H	$000FFE94_H$	125
I^2S ODD	91	$5B_H$			290_H	$000FFE90_H$	126
Input Capture 0	92	$5C_H$	ICR38	466_H	$28C_H$	$000FFE8C_H$	80
Input Capture 1	93	$5D_H$			288_H	$000FFE88_H$	81
Input Capture 2	94	$5E_H$	ICR39	467_H	284_H	$000FFE84_H$	82
Input Capture 3	95	$5F_H$			280_H	$000FFE80_H$	83

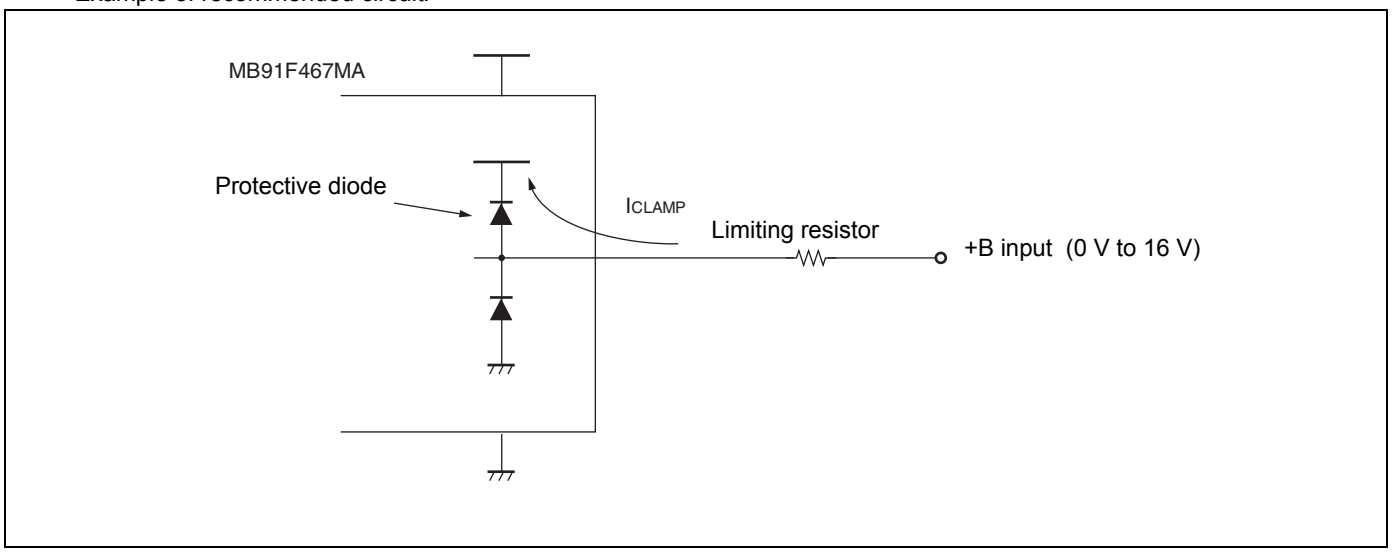
(Continued)

Modulation Degree (k)	Random No (N)	CMPR [hex]	center clk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
1	7	$02ED_H$	48	39.6	60.9	
1	9	$032C_H$	48	37.7	66.1	
1	11	$036B_H$	48	35.9	72.3	
1	13	$03AA_H$	48	34.3	79.9	
2	3	$046E_H$	48	41.8	56.4	
2	5	$04AC_H$	48	37.7	66.1	
2	7	$04EA_H$	48	34.3	79.9	
3	3	$066D_H$	48	39.6	60.9	
3	5	$06AA_H$	48	34.3	79.9	
4	3	$086C_H$	48	37.7	66.1	
5	3	$0A6B_H$	48	35.9	72.3	
6	3	$0C6A_H$	48	34.3	79.9	
1	3	$026F_H$	44	40.6	48.1	
1	5	$02AE_H$	44	38.4	51.6	
1	7	$02ED_H$	44	36.4	55.7	
1	9	$032C_H$	44	34.6	60.4	
1	11	$036B_H$	44	33	66.1	
1	13	$03AA_H$	44	31.5	73	
2	3	$046E_H$	44	38.4	51.6	
2	5	$04AC_H$	44	34.6	60.4	
2	7	$04EA_H$	44	31.5	73	
3	3	$066D_H$	44	36.4	55.7	
3	5	$06AA_H$	44	31.5	73	
4	3	$086C_H$	44	34.6	60.4	
5	3	$0A6B_H$	44	33	66.1	
6	3	$0C6A_H$	44	31.5	73	
1	3	$026F_H$	40	37	43.6	
1	5	$02AE_H$	40	34.9	46.8	
1	7	$02ED_H$	40	33.1	50.5	
1	9	$032C_H$	40	31.5	54.8	
1	11	$036B_H$	40	30	59.9	
1	13	$03AA_H$	40	28.7	66.1	
1	15	$03E9_H$	40	27.4	73.7	
2	3	$046E_H$	40	34.9	46.8	

(Continued)

(Continued)

- Note that if the +B signal is input when the microcontroller is off (not fixed at 0 V), power is supplied through the +B input pin; therefore, the microcontroller may partially operate.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave +B input pins open.
- Example of recommended circuit:



*3 : Maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*4 : Average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 100 ms period. The average value is the operation current × the operation ratio.

*5 : Total average output current is defined as the value of the average current flowing through all of the corresponding pins for a 100 ms period. The average value is the operation current × the operation ratio.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

(Continued)

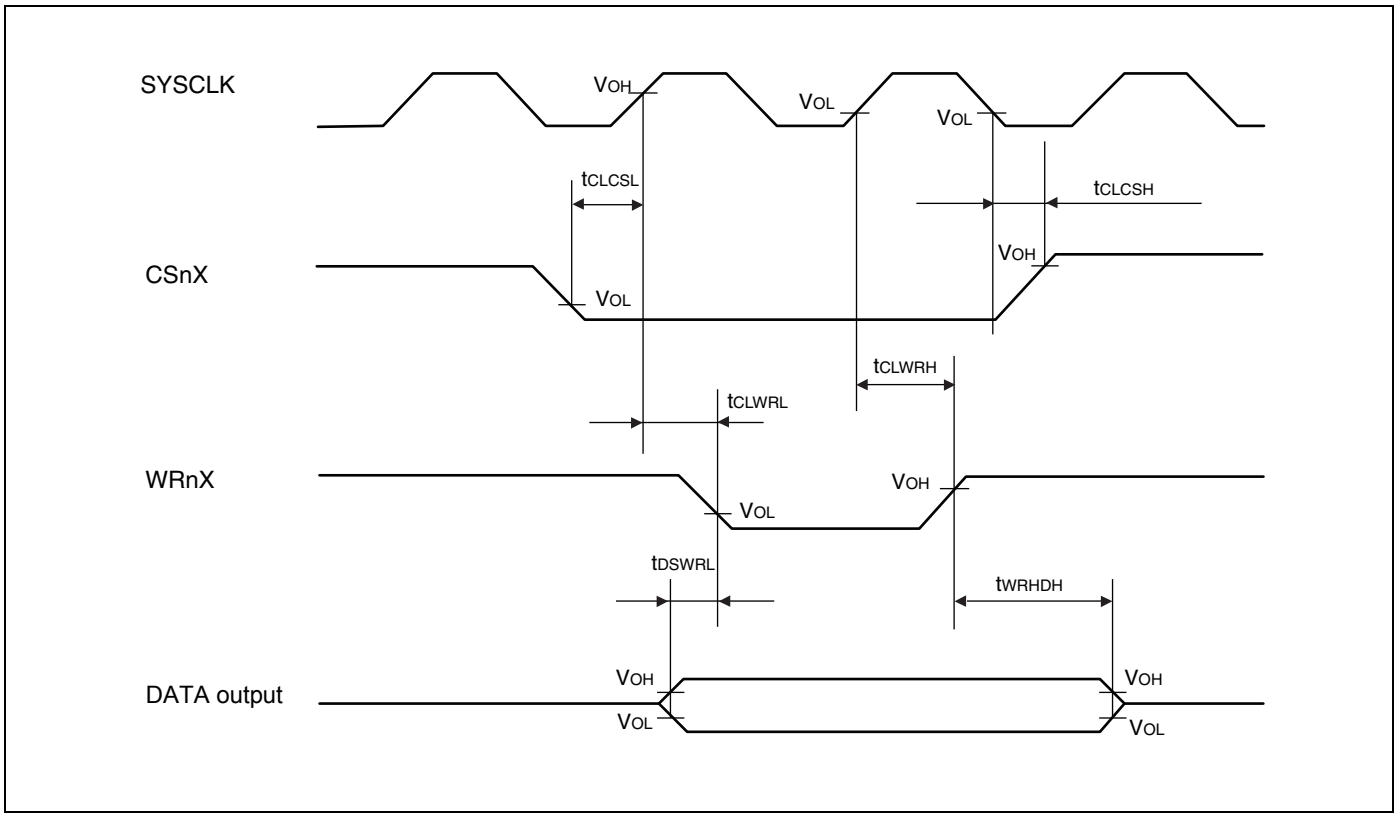
(T_A = –40°C to + 105°C, $V_{CC}5$ = 5.0 V ± 10%, $V_{CC}3$ = 3.3 V ±10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leakage current	I_{IL}	All input pins	$V_{CC}5$ = 5 V $V_{CC}3$ = $AV_{CC}3$ = 3.3 V $V_{SS} < V_I < V_{CC}5/3$	–5	—	+ 5	µA	
Input capacitance 1	C_{IN}	Other than VCC5, VCC3, VSS, AVCC3, AVSS, AVRH, C_1, C_2	—	—	5	15	pF	
Pull-up resistance	R_{UP}	INITX, Pins with pull-up resistance	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	Pins with pull-down resistance	—	25	50	100	kΩ	
Output “H” voltage	V_{OH1}	5/3 V pin	$V_{CC}5$ = 5.0 V, I_{OH} = –5.0 mA $V_{CC}5$ = 3.3 V, I_{OH} = –2.0 mA	$V_{CC}5$ − 0.5	—	—	V	
	V_{OH2}	3 V pin	$V_{CC}3$ = 3.3 V, I_{OH} = –4.0 mA	$V_{CC}3$ − 0.5	—	—	V	
	V_{OH3}	MediaLB pin	$V_{CC}3$ = 3.3 V, I_{OH} = –6.0 mA	2.0	—	—	V	
Output “L” voltage	V_{OL1}	5/3 Vpin	$V_{CC}5$ = 5.0 V, I_{OL} = 5.0 mA $V_{CC}5$ = 3.3 V, I_{OL} = 2.0 mA	—	—	0.4	V	
	V_{OL2}	3 Vpin	$V_{CC}3$ = 3.3 V, I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL3}	MediaLB pin	$V_{CC}3$ = 3.3 V, I_{OL} = 6.0 mA	—	—	0.4	V	

Synchronous write access − Non-byte control type

(Vcc3 = 3.3 V ±10%, Vss = 0.0 V, T_A = −40°C to + 105°C)

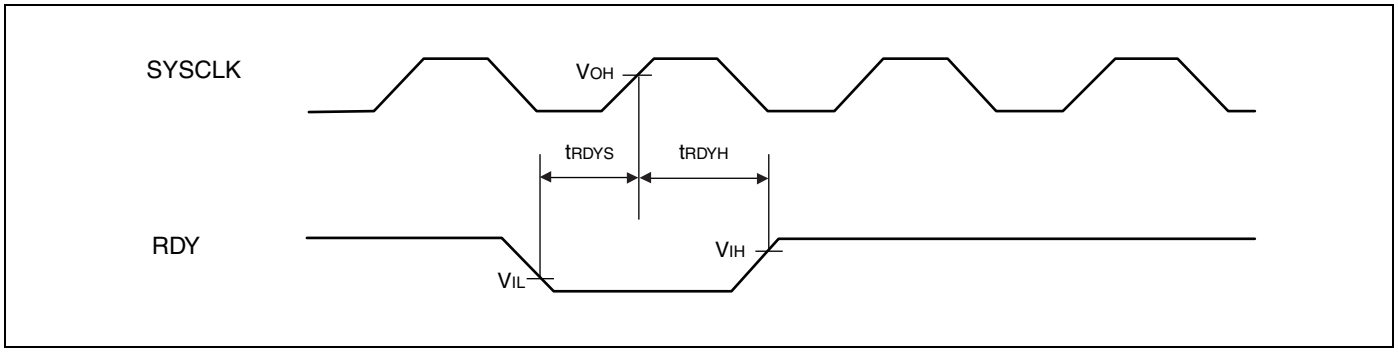
Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
SYSCLK ↑ →WRnX delay	t_{CLWRL}	SYSCLK WEX	—	− 6	—	+ 6	ns
	t_{CLWRH}			− 6	—	+ 6	
Data Valid →WRnX ↓ setup	t_{DSWRL}	WEX D31 to D16		—	0	—	
WRnX ↑ →Valid data hold	t_{WRHDH}	WEX D31 to D16		—	t_{CLKT}	—	
SYSCLK ↓ →CSnX delay	t_{CLCSL}	SYSCLK CSnX		− 6	—	+ 6	
	t_{CLCSH}			− 6	—	+ 6	



RDY wait cycle insertion

(Vcc3 = 3.3 V ±10%, Vss = 0.0 V, T_A = −40°C to + 105°C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
RDY setup time	t_{RDYS}	SYSCLK RDY	40	—	ns
RDY hold time	t_{RDYH}	SYSCLK RDY	0	—	ns

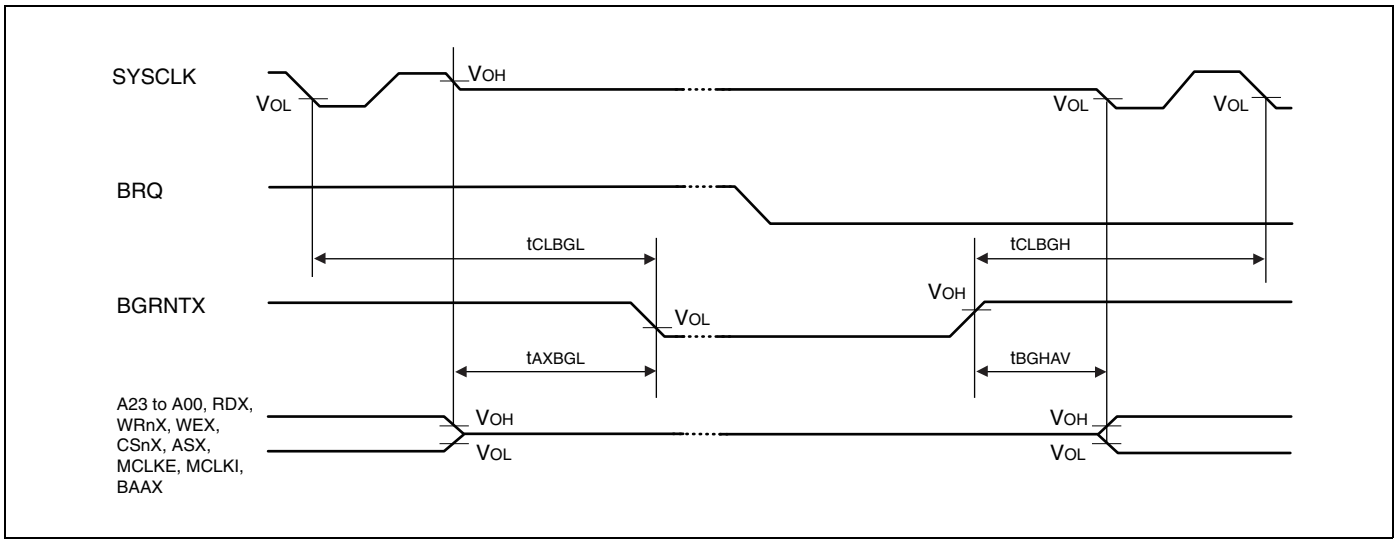


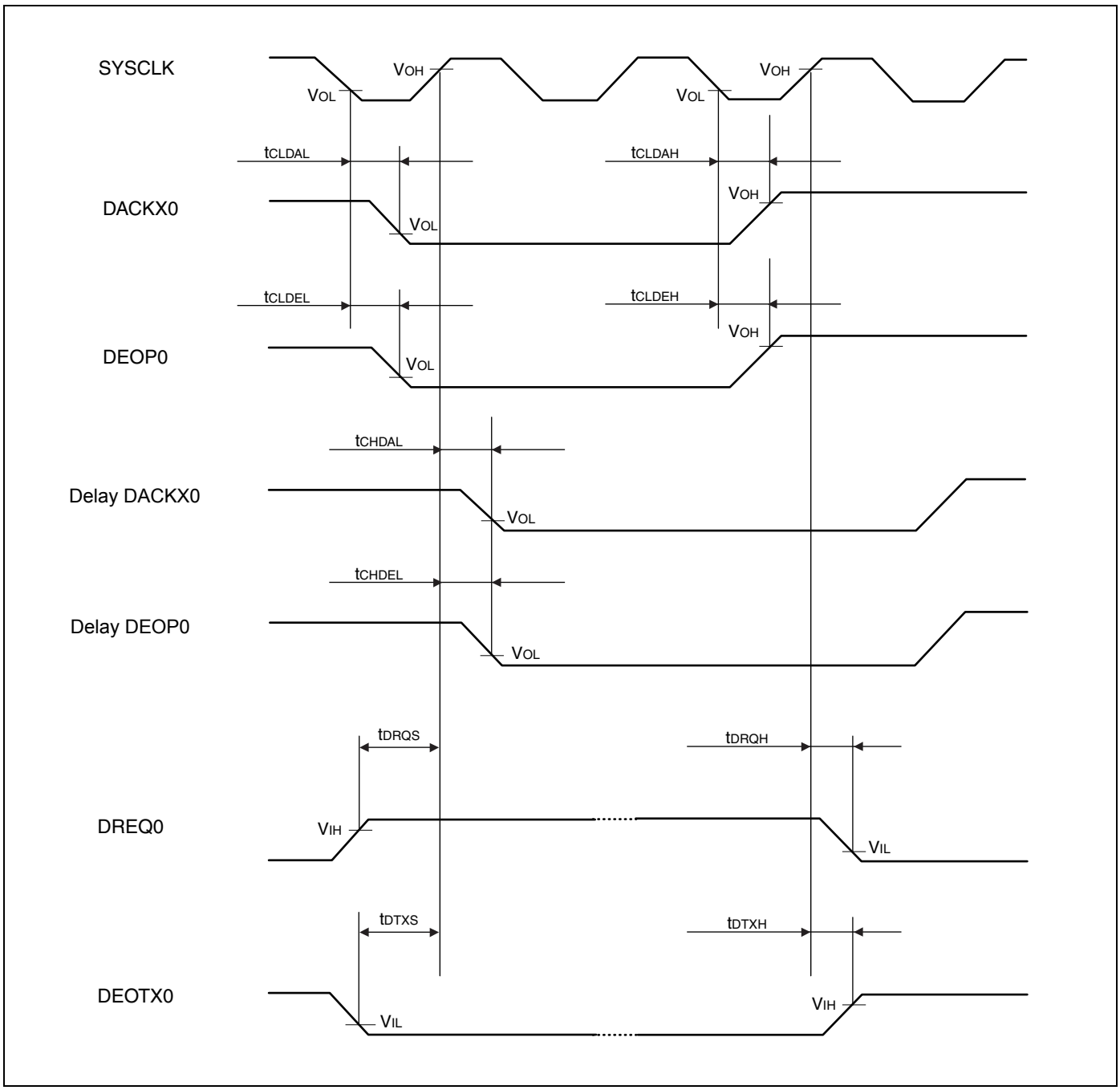
Bus hold timing

(Vcc3 = 3.3 V ±10%, Vss = 0.0 V, T_A = −40°C to + 105°C)

Parameter	Symbol	Pin name	Condition	Value			Unit
				Min	Typ	Max	
SYSCLK ↓ →BGRNTX delay	t_{CLBGL}	SYSCLK BGRNTX	—	—	2 × t_{CLKT}	—	ns
	t_{CLBGH}				2 × t_{CLKT}		
Bus High-Z→BGRNTX ↓	t_{AXBGL}	BGRNTX MCLKE, MCLKI A23 to A00 RDX, ASX WRnX, WEX CSnX, BAAX		—	t_{CLKT}	—	
	t_{BGHAV}			—	t_{CLKT}		

Note: Keep BRQ high until bus is enabled (recognized by the falling edge of BGRNTX). Keep BRQ high during the bus retention period.
The rising edge of BGRNTX recognizes whether bus is enabled after releasing the bus (setting BRQ to Low).




SYSCLK
VOH
VOL
VOH
VOL
tCLDAL
tCLDAH
DACKX0
VOH
VOL
tCLDEL
tCLDEH
DEOP0
VOH
VOL
tCHDAL
Delay DACKX0
VOL
tCHDEL
Delay DEOP0
VOL
tDRQS
tDRQH
DREQ0
VIH
VIL
tDTXS
tDTXH
DEOTX0
VIH
VIL