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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I <sup>2</sup> C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I <sup>2</sup> S, LVD, POR, PWM, WDT
Number of I/O	100
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64К х 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 42x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	121-LFBGA
Supplier Device Package	121-MAPBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk60dn256vmc10

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



- Communication interfaces
  - Ethernet controller with MII and RMII interface to external PHY and hardware IEEE 1588 capability
  - USB full-/low-speed On-the-Go controller with on-chip transceiver
  - Two Controller Area Network (CAN) modules
  - Three SPI modules
  - Two I2C modules
  - Six UART modules
  - Secure Digital host controller (SDHC)
  - I2S module



#### reminology and guidelines

Field	Description	Values
FFF	Program flash memory size	<ul> <li>32 = 32 KB</li> <li>64 = 64 KB</li> <li>128 = 128 KB</li> <li>256 = 256 KB</li> <li>512 = 512 KB</li> <li>1M0 = 1 MB</li> <li>2M0 = 2 MB</li> </ul>
R	Silicon revision	<ul> <li>Z = Initial</li> <li>(Blank) = Main</li> <li>A = Revision after main</li> </ul>
Т	Temperature range (°C)	<ul> <li>V = -40 to 105</li> <li>C = -40 to 85</li> </ul>
PP	Package identifier	<ul> <li>FM = 32 QFN (5 mm x 5 mm)</li> <li>FT = 48 QFN (7 mm x 7 mm)</li> <li>LF = 48 LQFP (7 mm x 7 mm)</li> <li>LH = 64 LQFP (10 mm x 10 mm)</li> <li>MP = 64 MAPBGA (5 mm x 5 mm)</li> <li>LK = 80 LQFP (12 mm x 12 mm)</li> <li>LL = 100 LQFP (14 mm x 14 mm)</li> <li>MC = 121 MAPBGA (8 mm x 8 mm)</li> <li>LQ = 144 LQFP (20 mm x 20 mm)</li> <li>MD = 144 MAPBGA (13 mm x 13 mm)</li> <li>MJ = 256 MAPBGA (17 mm x 17 mm)</li> </ul>
CC	Maximum CPU frequency (MHz)	<ul> <li>5 = 50 MHz</li> <li>7 = 72 MHz</li> <li>10 = 100 MHz</li> <li>12 = 120 MHz</li> <li>15 = 150 MHz</li> </ul>
N	Packaging type	<ul> <li>R = Tape and reel</li> <li>(Blank) = Trays</li> </ul>

### 2.4 Example

This is an example part number:

MK60DN512ZVMD10

# 3 Terminology and guidelines

## 3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.



# 5.2 Nonswitching electrical specifications

### 5.2.1 Voltage and current operating requirements Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>DD</sub>	Supply voltage	1.71	3.6	V	
V <sub>DDA</sub>	Analog supply voltage	1.71	3.6	V	
V <sub>DD</sub> – V <sub>DDA</sub>	V <sub>DD</sub> -to-V <sub>DDA</sub> differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	V <sub>SS</sub> -to-V <sub>SSA</sub> differential voltage	-0.1	0.1	V	
V <sub>BAT</sub>	RTC battery supply voltage	1.71	3.6	V	
V <sub>IH</sub>	Input high voltage				
	• $2.7 \text{ V} \le \text{V}_{\text{DD}} \le 3.6 \text{ V}$	$0.7 \times V_{DD}$	_	V	
	• $1.7 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}$	$0.75 \times V_{DD}$	_	V	
V <sub>IL</sub>	Input low voltage				
	• $2.7 \text{ V} \le \text{V}_{\text{DD}} \le 3.6 \text{ V}$	_	$0.35 \times V_{DD}$	V	
	• $1.7 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}$	_	$0.3 \times V_{DD}$	V	
V <sub>HYS</sub>	Input hysteresis	$0.06 \times V_{DD}$	_	V	
I <sub>ICDIO</sub>	Digital pin negative DC injection current — single pin				1
	• V <sub>IN</sub> < V <sub>SS</sub> -0.3V	-5	_	mA	
I <sub>ICAIO</sub>	Analog <sup>2</sup> , EXTAL, and XTAL pin DC injection current —				3
		F		mA	
	• $V_{IN} < V_{SS}$ -0.3V (Negative current injection)	-5			
	• $V_{IN} > V_{DD} + 0.3V$ (Positive current injection)	_	+5		
I <sub>ICcont</sub>	Contiguous pin DC injection current —regional limit,				
	includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins				
	Negative current injection	-25	—	mA	
	Positive current injection	_	+25		
V <sub>ODPU</sub>	Open drain pullup voltage level	V <sub>DD</sub>	V <sub>DD</sub>	V	4
V <sub>RAM</sub>	V <sub>DD</sub> voltage required to retain RAM	1.2	—	V	
V <sub>RFVBAT</sub>	V <sub>BAT</sub> voltage required to retain the VBAT register file	V <sub>POR VBAT</sub>	—	V	

- All 5 V tolerant digital I/O pins are internally clamped to V<sub>SS</sub> through an ESD protection diode. There is no diode connection to V<sub>DD</sub>. If V<sub>IN</sub> is less than V<sub>DIO\_MIN</sub>, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R=(V<sub>DIO\_MIN</sub>-V<sub>IN</sub>)/II<sub>ICDIO</sub>I.
- 2. Analog pins are defined as pins that do not have an associated general purpose I/O port function. Additionally, EXTAL and XTAL are analog pins.
- 3. All analog pins are internally clamped to V<sub>SS</sub> and V<sub>DD</sub> through ESD protection diodes. If V<sub>IN</sub> is less than V<sub>AIO\_MIN</sub> or greater than V<sub>AIO\_MAX</sub>, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R=(V<sub>AIO\_MIN</sub>-V<sub>IN</sub>)/II<sub>ICAIO</sub>I. The positive injection current limiting resistor is calculated as R=(V<sub>AIO\_MIN</sub>-V<sub>IN</sub>)/II<sub>ICAIO</sub>I. Select the larger of these two calculated resistances if the pin is exposed to positive and negative injection currents.
- 4. Open drain outputs must be pulled to VDD.



# 5.2.2 LVD and POR operating requirements

Table 2. V<sub>DD</sub> supply LVD and POR operating requirements

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V <sub>POR</sub>	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V <sub>LVDH</sub>	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V <sub>LVW1H</sub>	Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V <sub>LVW2H</sub>	Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V <sub>LVW3H</sub>	Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V <sub>LVW4H</sub>	Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V <sub>HYSH</sub>	Low-voltage inhibit reset/recover hysteresis — high range	_	±80	_	mV	
V <sub>LVDL</sub>	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V <sub>LVW1L</sub>	Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V <sub>LVW2L</sub>	Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V <sub>LVW3L</sub>	Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V <sub>LVW4L</sub>	Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V <sub>HYSL</sub>	Low-voltage inhibit reset/recover hysteresis — low range	_	±60		mV	
V <sub>BG</sub>	Bandgap voltage reference	0.97	1.00	1.03	V	
t <sub>LPO</sub>	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising thresholds are falling threshold + hysteresis voltage

#### Table 3. VBAT power operating requirements

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V <sub>POR_VBAT</sub>	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	



Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I <sub>DD_VBAT</sub>	Average current when CPU is not accessing RTC registers					10
	• @ 1.8V					
	● @ -40 to 25°C	_	0.57	0.67	μA	
	• @ 70°C	_	0.90	1.2	μA	
	• @ 105°C		2.4	3.5	μA	
	• @ 3.0V					
	<ul> <li>@ -40 to 25°C</li> </ul>		0.67	0.94	μA	
	• @ 70°C		1.0	1.4	μA	
	• @ 105°C	_	2.7	3.9	μA	

#### Table 6. Power consumption operating behaviors (continued)

- 1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
- 2. 100MHz core and system clock, 50MHz bus and FlexBus clock, and 25MHz flash clock . MCG configured for FEI mode. All peripheral clocks disabled.
- 3. 100MHz core and system clock, 50MHz bus and FlexBus clock, and 25MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled.
- 4. Max values are measured with CPU executing DSP instructions.
- 5. 25MHz core and system clock, 25MHz bus clock, and 12.5MHz FlexBus and flash clock. MCG configured for FEI mode.
- 6. 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
- 7. 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
- 8. 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
- 9. Data reflects devices with 128 KB of RAM. For devices with 64 KB of RAM, power consumption is reduced by 2 µA.
- 10. Includes 32kHz oscillator current and RTC operation.

### 5.2.5.1 Diagram: Typical IDD\_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at greater than 50 MHz frequencies.
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL



Board type	Symbol	Description	121 MAPBGA	Unit	Notes
Single-layer (1s)	R <sub>0JMA</sub>	Thermal resistance, junction to ambient (200 ft./ min. air speed)	52	°C/W	1
Four-layer (2s2p)	R <sub>0JMA</sub>	Thermal resistance, junction to ambient (200 ft./ min. air speed)	31	°C/W	1
_	R <sub>θJB</sub>	Thermal resistance, junction to board	17	°C/W	2
_	R <sub>θJC</sub>	Thermal resistance, junction to case	13	°C/W	3
	Ψ <sub>JT</sub>	Thermal characterization parameter, junction to package top outside center (natural convection)	3	°C/W	4

- 1. Determined according to JEDEC Standard JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air), or EIA/JEDEC Standard JESD51-6, Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air).
- 2. Determined according to JEDEC Standard JESD51-8, Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board.
- 3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
- 4. Determined according to JEDEC Standard JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air).

# 6 Peripheral operating requirements and behaviors

### 6.1 Core modules

### 6.1.1 Debug trace timing specifications

 Table 12.
 Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T <sub>cyc</sub>	Clock period	Frequency	MHz	
T <sub>wl</sub>	Low pulse width	2	_	ns
T <sub>wh</sub>	High pulse width	2	_	ns
T <sub>r</sub>	Clock and data rise time		3	ns

Table continues on the next page...



- 1. Assumes 25 MHz flash clock frequency.
- 2. Maximum times for erase parameters based on expectations at cycling end-of-life.
- 3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

# 6.4.1.3 Flash high voltage current behaviors

Table 22. Flash high voltage current behaviors

Symbol	Description	Min.	Тур.	Max.	Unit
I <sub>DD_PGM</sub>	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I <sub>DD_ERS</sub>	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

### 6.4.1.4 Reliability specifications

#### Table 23. NVM reliability specifications

Symbol	Description	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes		
Program Flash								
t <sub>nvmretp10k</sub>	Data retention after up to 10 K cycles	5	50	—	years			
t <sub>nvmretp1k</sub>	Data retention after up to 1 K cycles	20	100	_	years			
n <sub>nvmcycp</sub>	Cycling endurance	10 K	50 K	_	cycles	2		
	Data	Flash						
t <sub>nvmretd10k</sub>	Data retention after up to 10 K cycles	5	50	_	years			
t <sub>nvmretd1k</sub>	Data retention after up to 1 K cycles	20	100	—	years			
n <sub>nvmcycd</sub>	Cycling endurance	10 K	50 K	_	cycles	2		
FlexRAM as EEPROM								
t <sub>nvmretee100</sub>	Data retention up to 100% of write endurance	5	50	—	years			
t <sub>nvmretee10</sub>	Data retention up to 10% of write endurance	20	100	_	years			
	Write endurance					3		
n <sub>nvmwree16</sub>	<ul> <li>EEPROM backup to FlexRAM ratio = 16</li> </ul>	35 K	175 K	_	writes			
n <sub>nvmwree128</sub>	<ul> <li>EEPROM backup to FlexRAM ratio = 128</li> </ul>	315 K	1.6 M	_	writes			
n <sub>nvmwree512</sub>	<ul> <li>EEPROM backup to FlexRAM ratio = 512</li> </ul>	1.27 M	6.4 M	_	writes			
n <sub>nvmwree4k</sub>	EEPROM backup to FlexRAM ratio = 4096	10 M	50 M	_	writes			
n <sub>nvmwree32k</sub>	<ul> <li>EEPROM backup to FlexRAM ratio = 32,768</li> </ul>	80 M	400 M		writes			

- Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
- 2. Cycling endurance represents number of program/erase cycles at -40°C  $\leq$  T<sub>i</sub>  $\leq$  125°C.
- Write endurance represents the number of writes to each FlexRAM location at -40°C ≤Tj ≤ 125°C influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup per subsystem. Minimum and typical values assume all byte-writes to FlexRAM.



Figure 12. FlexBus write timing diagram

### 6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

# 6.6 Analog

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
C <sub>rate</sub>	ADC conversion	16-bit mode					5
	rate	No ADC hardware averaging	37.037	_	461.467	Ksps	
		Continuous conversions enabled, subsequent conversion time					

 Table 27.
 16-bit ADC operating conditions (continued)

- 1. Typical values assume  $V_{DDA}$  = 3.0 V, Temp = 25 °C,  $f_{ADCK}$  = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
- 2. DC potential difference.
- 3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8  $\Omega$  analog source resistance. The R<sub>AS</sub>/C<sub>AS</sub> time constant should be kept to < 1 ns.
- 4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
- 5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.



Figure 13. ADC input impedance equivalency diagram

#### 6.6.1.2 16-bit ADC electrical characteristics Table 28. 16-bit ADC characteristics (V<sub>REFH</sub> = V<sub>DDA</sub>, V<sub>REFL</sub> = V<sub>SSA</sub>)

Symbol	Description	Conditions <sup>1</sup> .	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
I <sub>DDA_ADC</sub>	Supply current		0.215		1.7	mA	3

Table continues on the next page ...



Symbol	Description	Conditions <sup>1</sup> .	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
EIL	Input leakage error			$I_{In} \times R_{AS}$		mV	I <sub>In</sub> = leakage current
							(refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	
V <sub>TEMP25</sub>	Temp sensor voltage	25 °C	706	716	726	mV	

#### Table 28. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ , $V_{REFL} = V_{SSA}$ ) (continued)

- 1. All accuracy numbers assume the ADC is calibrated with  $V_{REFH} = V_{DDA}$
- Typical values assume V<sub>DDA</sub> = 3.0 V, Temp = 25 °C, f<sub>ADCK</sub> = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC\_CFG1[ADLPC] (low power). For lowest power operation, ADC\_CFG1[ADLPC] must be set, the ADC\_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
- 4. 1 LSB =  $(V_{REFH} V_{REFL})/2^{N}$
- 5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
- 6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
- 7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.

#### Typical ADC 16-bit Differential ENOB vs ADC Clock 100Hz, 90% FS Sine Input







Symbol	Description	Conditions	Min. Typ. <sup>1</sup> Max.		Unit	Notes	
G	Gain <sup>4</sup>	PGAG=0	0.95	1	1.05		$R_{AS} < 100\Omega$
		• PGAG=1	1.9	2	2.1		
		• PGAG=2	3.8	4	4.2		
		• PGAG=3	7.6	8	8.4		
		• PGAG=4	15.2	16	16.6		
		• PGAG=5	30.0	31.6	33.2		
		• PGAG=6	58.8	63.3	67.8		
BW	Input signal	16-bit modes	_	_	4	kHz	
	bandwidth	<ul> <li>&lt; 16-bit modes</li> </ul>	_	_	40	kHz	
PSRR	Power supply rejection ratio	Gain=1	_	-84		dB	V <sub>DDA</sub> = 3V ±100mV, f <sub>VDDA</sub> = 50Hz, 60Hz
CMRR	Common mode	Gain=1	—	-84	—	dB	V <sub>CM</sub> =
	rejection ratio	• Gain=64	_	-85	_	dB	500mVpp, f <sub>VCM</sub> = 50Hz, 100Hz
V <sub>OFS</sub>	Input offset voltage		-	0.2	—	mV	Output offset = V <sub>OFS</sub> *(Gain+1)
T <sub>GSW</sub>	Gain switching settling time		-	_	10	μs	5
dG/dT	Gain drift over full	• Gain=1	—	6	10	ppm/°C	
	temperature range	• Gain=64		31	42	ppm/°C	
dG/dV <sub>DDA</sub>	Gain drift over	• Gain=1	—	0.07	0.21	%/V	V <sub>DDA</sub> from 1.71
	supply voltage	• Gain=64	—	0.14	0.31	%/V	to 3.6V
E <sub>IL</sub>	Input leakage error	All modes		$I_{ln} \times R_{AS}$		mV	I <sub>In</sub> = leakage current
							(refer to the MCU's voltage and current operating ratings)
V <sub>PP,DIFF</sub>	Maximum differential input signal swing		$\left(\frac{\min(v)}{v}\right)$	√ <sub>x</sub> ,V <sub>DDA</sub> −V <sub>x</sub> ) Gain	<u>-0.2)×4</u> )	V	6
			where V <sub>2</sub>	$x = V_{REFPG}$	<sub>A</sub> × 0.583		
SNR	Signal-to-noise	Gain=1	80	90		dB	16-bit
	Tallo	• Gain=64	52	66	_	dB	mode, Average=32
THD	Total harmonic	Gain=1	85	100	—	dB	16-bit
	aistortion	• Gain=64	49	95		dB	differential mode, Average=32, f <sub>in</sub> =100Hz

Table 30. 16-bit ADC with PGA characteristics (continued)

Table continues on the next page...

NP

rempheral operating requirements and behaviors



Figure 16. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=0)



Peripheral operating requirements and behaviors



Figure 18. Typical INL error vs. digital code



Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V <sub>out</sub>	Voltage reference output with factory trim at nominal $V_{\text{DDA}}$ and temperature=25C	1.1915	1.195	1.1977	V	
V <sub>out</sub>	Voltage reference output — factory trim	1.1584	—	1.2376	V	
V <sub>out</sub>	Voltage reference output — user trim	1.193	—	1.197	V	
V <sub>step</sub>	Voltage reference trim step	—	0.5	—	mV	
V <sub>tdrift</sub>	Temperature drift (Vmax -Vmin across the full temperature range)		_	80	mV	
I <sub>bg</sub>	Bandgap only current	—	—	80	μA	1
I <sub>lp</sub>	Low-power buffer current	—	—	360	uA	1
I <sub>hp</sub>	High-power buffer current	—	—	1	mA	1
$\Delta V_{LOAD}$	Load regulation				μV	1, 2
	• current = ± 1.0 mA	_	200	_		
T <sub>stup</sub>	Buffer startup time	_	—	100	μs	
V <sub>vdrift</sub>	Voltage drift (Vmax -Vmin across the full voltage range)	_	2	_	mV	1

Table 35. VREF full-range operating behaviors

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.

2. Load regulation voltage is the difference between the VREF\_OUT voltage with no load vs. voltage with defined load

#### Table 36. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T <sub>A</sub>	Temperature	0	50	°C	

#### Table 37. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>out</sub>	Voltage reference output with factory trim	1.173	1.225	V	

### 6.7 Timers

See General switching specifications.

## 6.8 Communication interfaces



### 6.8.5 CAN switching specifications

See General switching specifications.

### 6.8.6 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation		25	MHz	
DS1	DSPI_SCK output cycle time	2 x t <sub>BUS</sub>	—	ns	
DS2	DSPI_SCK output high/low time	(t <sub>SCK</sub> /2) – 2	$(t_{SCK}/2) + 2$	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	(t <sub>BUS</sub> x 2) – 2	_	ns	1
DS4	DSPI_SCK to DSPI_PCSn invalid delay	(t <sub>BUS</sub> x 2) – 2	_	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	_	8	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	0	_	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	14		ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

 Table 42.
 Master mode DSPI timing (limited voltage range)

1. The delay is programmable in SPIx\_CTARn[PSSCK] and SPIx\_CTARn[CSSCK].

2. The delay is programmable in SPIx\_CTARn[PASC] and SPIx\_CTARn[ASC].









Figure 27. SDHC timing

### 6.8.11 I2S/SAI switching specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

# 6.8.11.1 Normal Run, Wait and Stop mode performance over a limited operating voltage range

This section provides the operating performance over a limited operating voltage for the device in Normal Run, Wait and Stop modes.

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S1	I2S_MCLK cycle time	40	_	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	_	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns

 
 Table 48.
 I2S/SAI master mode timing in Normal Run, Wait and Stop modes (limited voltage range)

Table continues on the next page...



# Table 49. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (limited voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	4.5	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid <sup>1</sup>	—	25	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear



Figure 29. I2S/SAI timing — slave modes

# 6.8.11.2 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

 Table 50.
 I2S/SAI master mode timing in Normal Run, Wait and Stop modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	_	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	_	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	-1.0	—	ns

Table continues on the next page...



- 1. The TSI module is functional with capacitance values outside this range. However, optimal performance is not guaranteed.
- 2. Fixed external capacitance of 20 pF.
- 3. REFCHRG = 2, EXTCHRG=0.
- 4. REFCHRG = 0, EXTCHRG = 10.
- 5.  $V_{DD} = 3.0 V.$
- 6. The programmable current source value is generated by multiplying the SCANC[REFCHRG] value and the base current.
- 7. The programmable current source value is generated by multiplying the SCANC[EXTCHRG] value and the base current.
- 8. Measured with a 5 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 8; lext = 16.
- 9. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 2; lext = 16.
- 10. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 16, NSCN = 3; lext = 16.
- 11. Sensitivity defines the minimum capacitance change when a single count from the TSI module changes. Sensitivity depends on the configuration used. The documented values are provided as examples calculated for a specific configuration of operating conditions using the following equation: (C<sub>ref</sub> \* I<sub>ext</sub>)/(I<sub>ref</sub> \* PS \* NSCN)

The typical value is calculated with the following configuration:

I<sub>ext</sub> = 6 μA (EXTCHRG = 2), PS = 128, NSCN = 2, I<sub>ref</sub> = 16 μA (REFCHRG = 7), C<sub>ref</sub> = 1.0 pF

The minimum value is calculated with the following configuration:

I<sub>ext</sub> = 2 μA (EXTCHRG = 0), PS = 128, NSCN = 32, I<sub>ref</sub> = 32 μA (REFCHRG = 15), C<sub>ref</sub> = 0.5 pF

The highest possible sensitivity is the minimum value because it represents the smallest possible capacitance that can be measured by a single count.

- 12. Time to do one complete measurement of the electrode. Sensitivity resolution of 0.0133 pF, PS = 0, NSCN = 0, 1 electrode, EXTCHRG = 7.
- 13. REFCHRG=0, EXTCHRG=4, PS=7, NSCN=0F, LPSCNITV=F, LPO is selected (1 kHz), and fixed external capacitance of 20 pF. Data is captured with an average of 7 periods window.

## 7 Dimensions

### 7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
121-pin MAPBGA	98ASA00344D

# 8 Pinout



121	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
MAP Bga											
J4	PTA11	DISABLED		PTA11		FTM2_CH1	MII0_RXCLK		FTM2_QD_ PHB		
K8	PTA12	CMP2_IN0	CMP2_IN0	PTA12	CAN0_TX	FTM1_CH0	RMII0_RXD1/ MII0_RXD1		I2S0_TXD0	FTM1_QD_ PHA	
L8	PTA13/ LLWU_P4	CMP2_IN1	CMP2_IN1	PTA13/ LLWU_P4	CAN0_RX	FTM1_CH1	RMII0_RXD0/ MII0_RXD0		12S0_TX_FS	FTM1_QD_ PHB	
K9	PTA14	DISABLED		PTA14	SPI0_PCS0	UART0_TX	RMII0_CRS_ DV/ MII0_RXDV		I2S0_RX_BCLK	I2S0_TXD1	
L9	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_RX	RMII0_TXEN/ MII0_TXEN		I2S0_RXD0		
J10	PTA16	DISABLED		PTA16	SPI0_SOUT	UART0_CTS_ b/ UART0_COL_b	RMII0_TXD0/ MII0_TXD0		I2S0_RX_FS	12S0_RXD1	
H10	PTA17	ADC1_SE17	ADC1_SE17	PTA17	SPI0_SIN	UART0_RTS_b	RMII0_TXD1/ MII0_TXD1		I2S0_MCLK		
L10	VDD	VDD	VDD								
K10	VSS	VSS	VSS								
L11	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0				
K11	PTA19	XTAL0	XTAL0	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ALT1		
J11	RESET_b	RESET_b	RESET_b								
H11	PTA29	DISABLED		PTA29			MII0_COL		FB_A24		
G11	PTB0/ LLWU_P5	ADC0_SE8/ ADC1_SE8/ TSI0_CH0	ADC0_SE8/ ADC1_SE8/ TSI0_CH0	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0	rmiio_mdio/ Miio_mdio		FTM1_QD_ PHA		
G10	PTB1	ADC0_SE9/ ADC1_SE9/ TSI0_CH6	ADC0_SE9/ ADC1_SE9/ TSI0_CH6	PTB1	I2C0_SDA	FTM1_CH1	RMII0_MDC/ MII0_MDC		FTM1_QD_ PHB		
G9	PTB2	ADC0_SE12/ TSI0_CH7	ADC0_SE12/ TSI0_CH7	PTB2	I2C0_SCL	UART0_RTS_b	ENET0_1588_ TMR0		FTM0_FLT3		
G8	PTB3	ADC0_SE13/ TSI0_CH8	ADC0_SE13/ TSI0_CH8	PTB3	I2C0_SDA	UART0_CTS_ b/ UART0_COL_b	ENET0_1588_ TMR1		FTM0_FLT0		
F11	PTB6	ADC1_SE12	ADC1_SE12	PTB6				FB_AD23			
E11	PTB7	ADC1_SE13	ADC1_SE13	PTB7				FB_AD22			
D11	PTB8	DISABLED		PTB8		UART3_RTS_b		FB_AD21			
E10	PTB9	DISABLED		PTB9	SPI1_PCS1	UART3_CTS_b		FB_AD20			
D10	PTB10	ADC1_SE14	ADC1_SE14	PTB10	SPI1_PCS0	UART3_RX		FB_AD19	FTM0_FLT1		
C10	PTB11	ADC1_SE15	ADC1_SE15	PTB11	SPI1_SCK	UART3_TX		FB_AD18	FTM0_FLT2		
B10	PTB16	TSI0_CH9	TSI0_CH9	PTB16	SPI1_SOUT	UART0_RX		FB_AD17	EWM_IN		
E9	PTB17	TSI0_CH10	TSI0_CH10	PTB17	SPI1_SIN	UART0_TX		FB_AD16	EWM_OUT_b		
D9	PTB18	TSIO_CH11	TSI0_CH11	PTB18	CAN0_TX	FTM2_CH0	I2S0_TX_BCLK	FB_AD15	FTM2_QD_ PHA		
C9	PTB19	TSI0_CH12	TSI0_CH12	PTB19	CAN0_RX	FTM2_CH1	I2S0_TX_FS	FB_OE_b	FTM2_QD_ PHB		
F10	PTB20	DISABLED		PTB20	SPI2_PCS0			FB_AD31	CMP0_OUT		



Rev. No.	Date	Substantial Changes
3	6/2013	<ul> <li>In ESD handling ratings, added a note for ILAT.</li> <li>Updated "Voltage and current operating requirements" Table 1.</li> <li>Updated I<sub>OL</sub> data for V<sub>OL</sub> row in "Voltage and current operating behaviors" Table 4.</li> <li>Updated wakeup times and t<sub>POR</sub> value in "Power mode transition operating behaviors" Table 5.</li> <li>In "EMC radiated emissions operating behaviors" Table 7, added a column for 144MAPBGA.</li> <li>In "16-bit ADC operating conditions" Table 27, updated the max spec of VADIN.</li> <li>In "16-bit ADC electrical characteristics" Table 28, updated the temp sensor slope and voltage specs.</li> <li>Updated Inter-Integrated Circuit Interface (I<sup>2</sup>C) timing.</li> <li>In SDHC specifications, added operating voltage row.</li> </ul>

# Table 55. Revision history (continued)