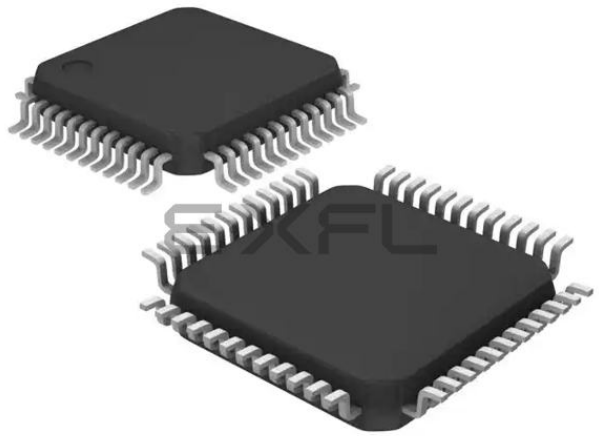

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	37
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f100c6t6b

2.1 Device overview

The description below gives an overview of the complete range of peripherals proposed in this family.

Figure 1 shows the general block diagram of the device family.

Table 2. STM32F100xx features and peripheral counts

Peripheral		STM32F100Cx				STM32F100Rx				STM32F100Vx	
Flash - Kbytes		16	32	64	128	16	32	64	128	64	128
SRAM - Kbytes		4	4	8	8	4	4	8	8	8	8
Timers	Advanced-control	1		1		1		1		1	
	General-purpose	5(1)		6		5(1)		6		6	
Communication interfaces	**SPI**	1(2)		2		1(2)		2		2	
	I^2C	1(3)		2		1(3)		2		2	
	USART	2(4)		3		2(4)		3		3	
	CEC	1									
12-bit synchronized ADC number of channels		1 10 channels				1 16 channels				1 16 channels	
GPIOs		37				51				80	
12-bit DAC Number of channels		2 2									
CPU frequency		24 MHz									
Operating voltage		2.0 to 3.6 V									
Operating temperatures		Ambient operating temperature: –40 to +85 °C /–40 to +105 °C (see *Table 8*) Junction temperature: –40 to +125 °C (see *Table 8*)									
Packages		LQFP48				LQFP64, TFBGA64				LQFP100	

1. TIM4 not present.
2. SPI2 is not present.
3. I2C2 is not present.
4. USART3 is not present.

higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

2.2.11 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop mode
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode, providing high impedance output.

2.2.12 Low-power modes

The STM32F100xx value line supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop** mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.
  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output or the RTC alarm.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), a IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.2.13 DMA

The flexible 7-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

Their counters can be frozen in debug mode.

Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.2.16 I²C bus

The I²C bus interface can operate in multimaster and slave modes. It can support standard and fast modes.

It supports dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.
The interface can be served by DMA and it supports SM Bus 2.0/PM Bus.

2.2.17 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F100xx value line embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

The available USART interfaces communicate at up to 3 Mbit/s. They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode and have LIN Master/Slave capability.

The USART interfaces can be served by the DMA controller.

3 Pinouts and pin description

Figure 3. STM32F100xx value line LQFP100 pinout

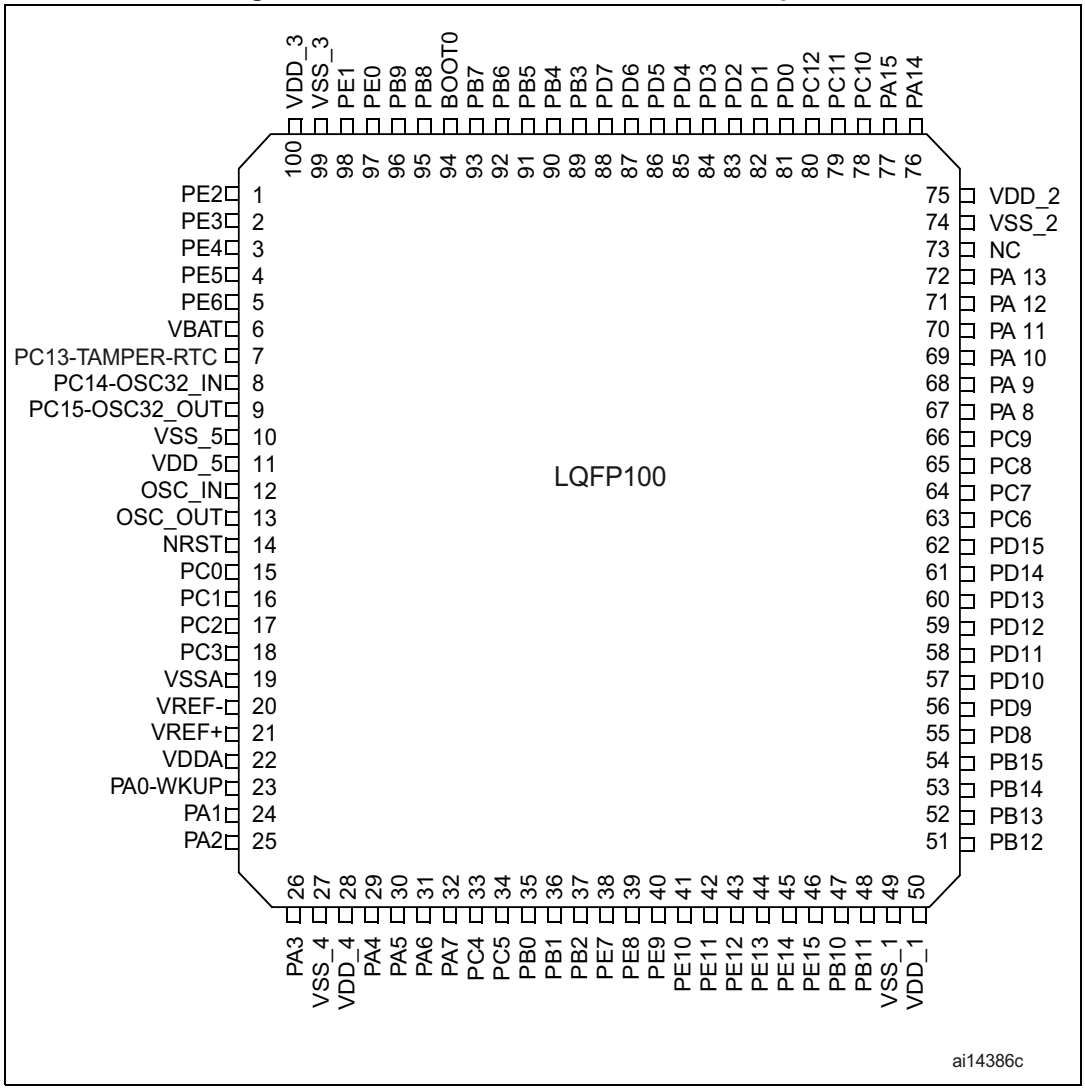


Figure 4. STM32F100xx value line LQFP64 pinout

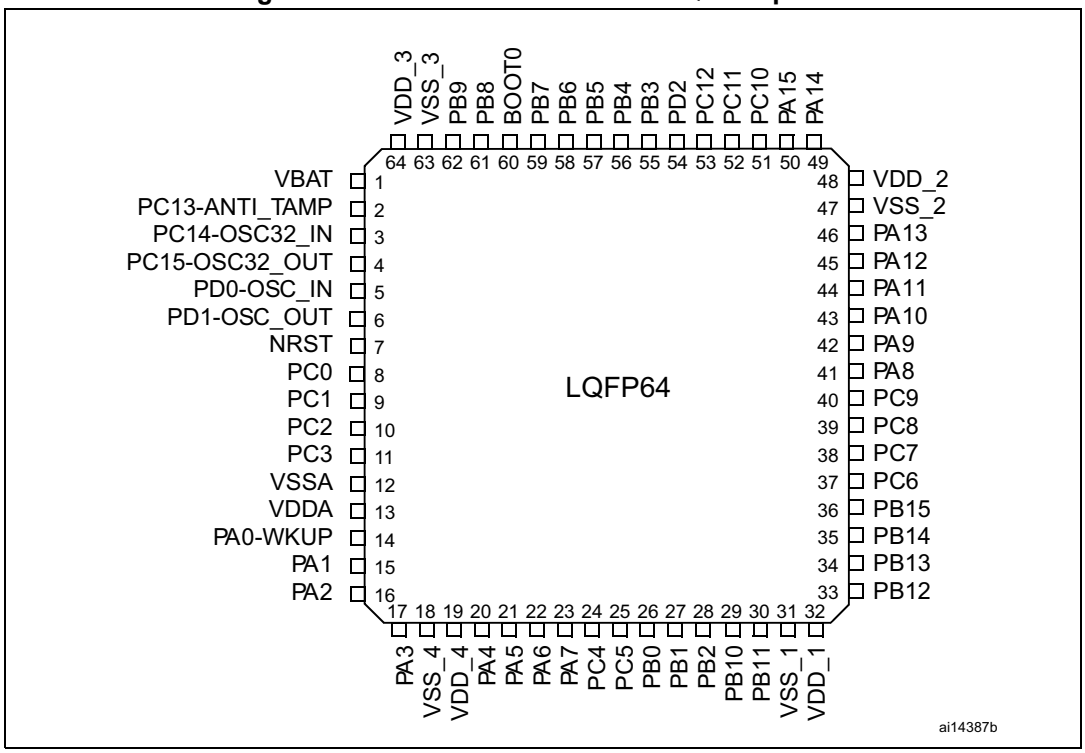


Figure 5. STM32F100xx value line LQFP48 pinout

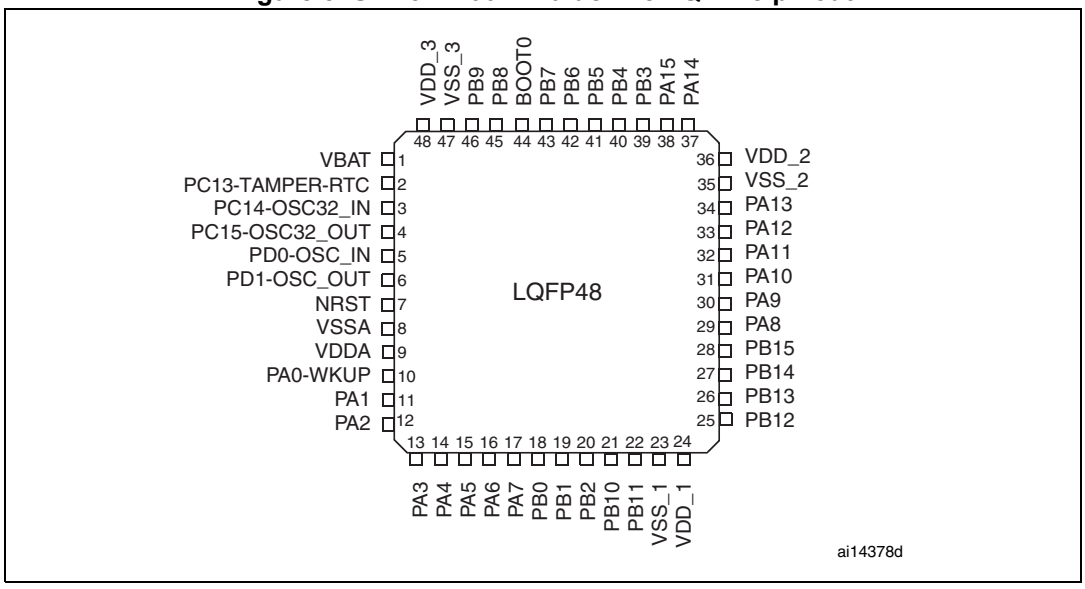


Table 4. Low & medium-density STM32F100xx pin definitions (continued)

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3)(4)	
LQFP100	LQFP64	TFBGA64	LQFP48					Default	Remap
57	-	-	-	PD10	I/O	FT	PD10	-	USART3_CK
58	-	-	-	PD11	I/O	FT	PD11	-	USART3_CTS
59	-	-	-	PD12	I/O	FT	PD12	-	TIM4_CH1(11) / USART3_RTS
60	-	-	-	PD13	I/O	FT	PD13	-	TIM4_CH2(11)
61	-	-	-	PD14	I/O	FT	PD14	-	TIM4_CH3(11)
62	-	-	-	PD15	I/O	FT	PD15	-	TIM4_CH4(11)
63	37	F6	-	PC6	I/O	FT	PC6	-	TIM3_CH1
64	38	E7	-	PC7	I/O	FT	PC7	-	TIM3_CH2
65	39	E8	-	PC8	I/O	FT	PC8	-	TIM3_CH3
66	40	D8	-	PC9	I/O	FT	PC9	-	TIM3_CH4
67	41	D7	29	PA8	I/O	FT	PA8	USART1_CK / MCO / TIM1_CH1	-
68	42	C7	30	PA9	I/O	FT	PA9	USART1_TX(12) / TIM1_CH2 / TIM15_BKIN	-
69	43	C6	31	PA10	I/O	FT	PA10	USART1_RX(12) / TIM1_CH3 / TIM17_BKIN	-
70	44	C8	32	PA11	I/O	FT	PA11	USART1_CTS / TIM1_CH4	-
71	45	B8	33	PA12	I/O	FT	PA12	USART1_RTS / TIM1_ETR	-
72	46	A8	34	PA13	I/O	FT	JTMS-SWDIO	-	PA13
73	-	-	-	Not connected					-
74	47	D5	35	V_{SS_2}	S	-	V_{SS_2}	-	-
75	48	E5	36	V_{DD_2}	S	-	V_{DD_2}	-	-
76	49	A7	37	PA14	I/O	FT	JTCK/SWCLK	-	PA14
77	50	A6	38	PA15	I/O	FT	JTDI	-	TIM2_CH1_ETR/ PA15/ SPI1_NSS
78	51	B7	-	PC10	I/O	FT	PC10	-	USART3_TX

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 2 V ≤V_{DD} ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

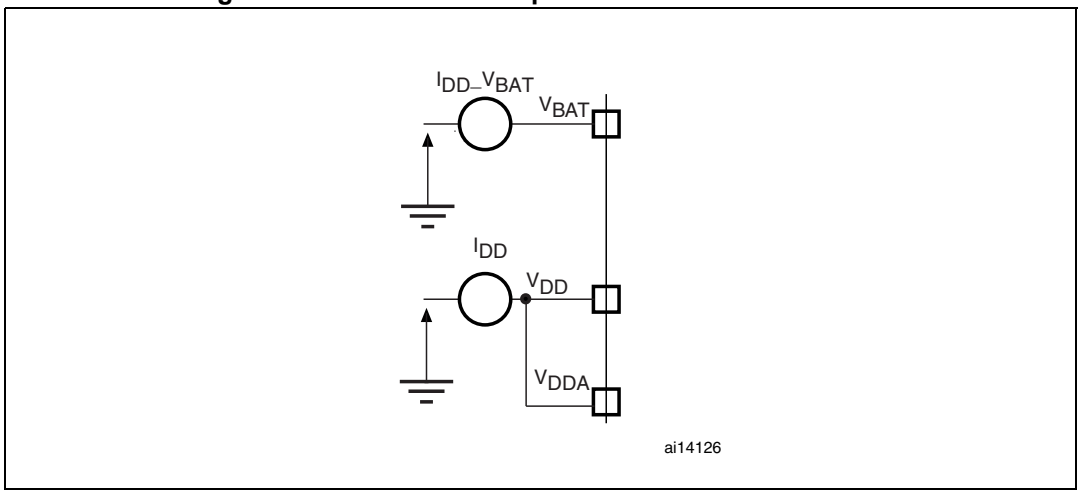
The loading conditions used for pin parameter measurement are shown in *Figure 8*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

5.1.7 Current consumption measurement

Figure 11. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 5: Voltage characteristics*, *Table 6: Current characteristics*, and *Table 7: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD} –V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}(2)	Input voltage on five volt tolerant pin	V_{SS} –0.3	V_{DD} +4.0	
	Input voltage on any other pin	V_{SS} –0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 5.3.11: Absolute maximum ratings (electrical sensitivity)*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 6: Current characteristics* for the maximum allowed injected current values.

Table 8. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(2)	LQFP100	-	434	mW
		LQFP64	-	444	
		TFBGA64	-	308	
		LQFP48	-	363	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low power dissipation(3)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low power dissipation(3)	–40	125	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

1. When the ADC is used, refer to *Table 42: ADC characteristics*.
2. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed $T_J$max (see *Table 6.5: Thermal characteristics on page 89*).
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed $T_J$max (see *Table 6.5: Thermal characteristics on page 89*).

Note: It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.

5.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Table 9. Operating conditions at power-up / power-down

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	0	∞	µs/V
	V_{DD} fall time rate	20	∞	

5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 10* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 10. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	V
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	V
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8(1)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$(2)	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(2)	Reset temporization	-	1.5	2.5	4.5	ms

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design.

Table 17. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typical values(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	Running on high-speed external clock with an 8 MHz crystal(3)	24 MHz	7.3	2.6	mA
			16 MHz	5.2	2	
			8 MHz	2.8	1.3	
			4 MHz	2	1.1	
			2 MHz	1.5	1.1	
			1 MHz	1.25	1	
			500 kHz	1.1	1	
			125 kHz	1.05	0.95	
		Running on high-speed internal RC (HSI)	24 MHz	6.65	1.9	
			16 MHz	4.5	1.4	
			8 MHz	2.2	0.7	
			4 MHz	1.35	0.55	
			2 MHz	0.85	0.45	
			1 MHz	0.6	0.41	
			500 kHz	0.5	0.39	
			125 kHz	0.4	0.37	

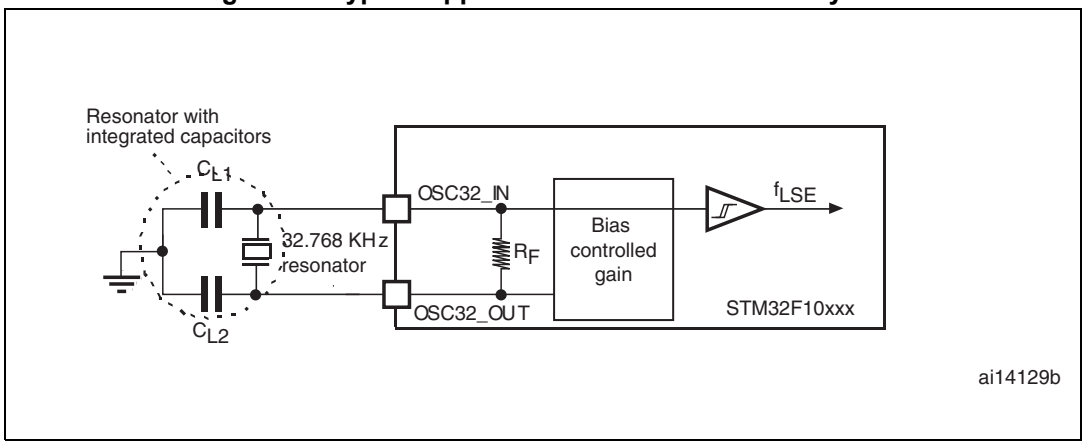
1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA for the ADC and of 0.5 mA for the DAC analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. An 8 MHz crystal is used as the external clock source. The AHB prescaler is used to reduce the frequency when f_{HCLK} > 8 MHz, the PLL is used when f_{HCLK} > 8 MHz.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 18*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions summarized in *Table 5*.

Figure 21. Typical application with a 32.768 kHz crystal



5.3.7 Internal clock source characteristics

The parameters given in *Table 23* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

High-speed internal (HSI) RC oscillator

Table 23. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
$DuCy_{(HSI)}$	Duty cycle	-	45	-	55	%
ACC_{HSI}	Accuracy of HSI oscillator	T_A = –40 to 105 °C(2)	-2.4	-	2.5	%
		T_A = –10 to 85 °C(2)	-2.2	-	1.3	%
		T_A = 0 to 70 °C(2)	-1.9	-	1.3	%
		T_A = 25 °C	-1	-	1	%
$t_{su(HSI)}$(3)	HSI oscillator startup time	-	1	-	2	µs
$I_{DD(HSI)}$(3)	HSI oscillator power consumption	-	-	80	100	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C °C unless otherwise specified.
2. Guaranteed by characterization results.
3. Guaranteed by design. Not tested in production

Figure 22. Standard I/O input characteristics - CMOS port

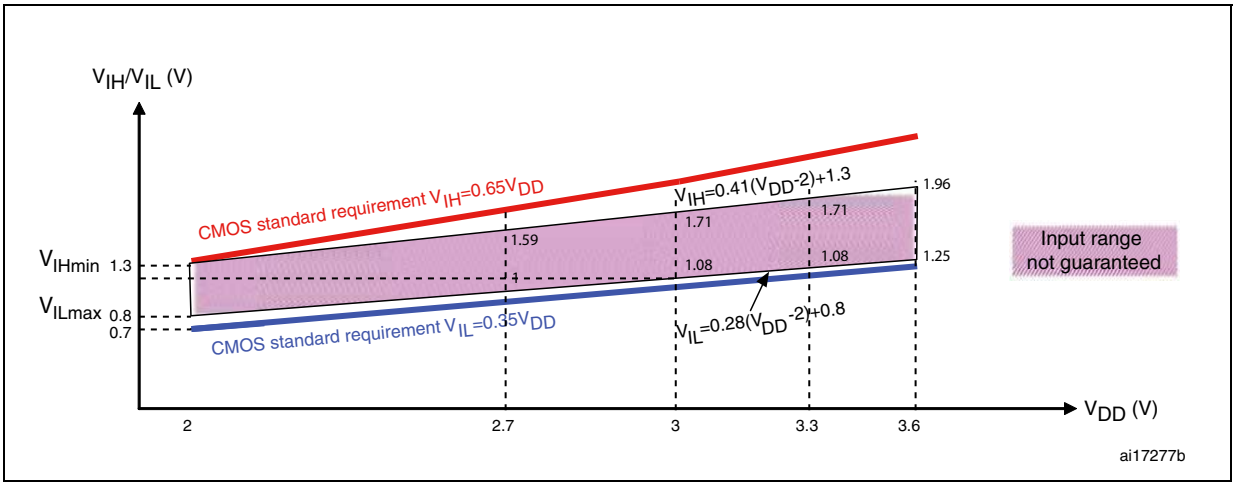
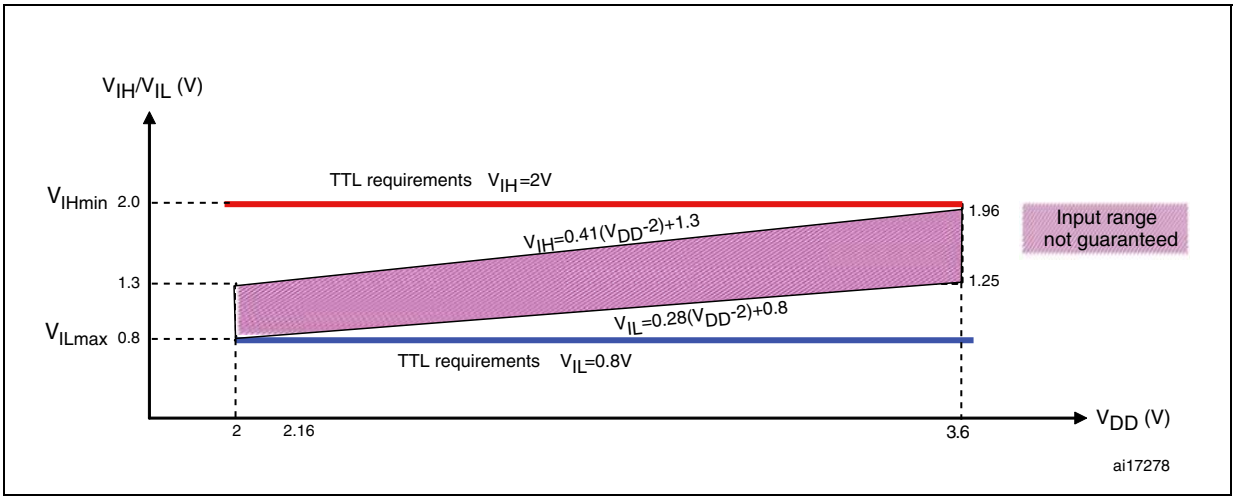


Figure 23. Standard I/O input characteristics - TTL port



5.3.19 Temperature sensor characteristics

Table 47. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L (1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope (1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25} (1)	Voltage at 25°C	1.32	1.41	1.50	V
t_{START} (2)	Startup time	4	-	10	µs
T_{S_temp} (3)(2)	ADC sampling time when reading the temperature	-	-	17.1	µs

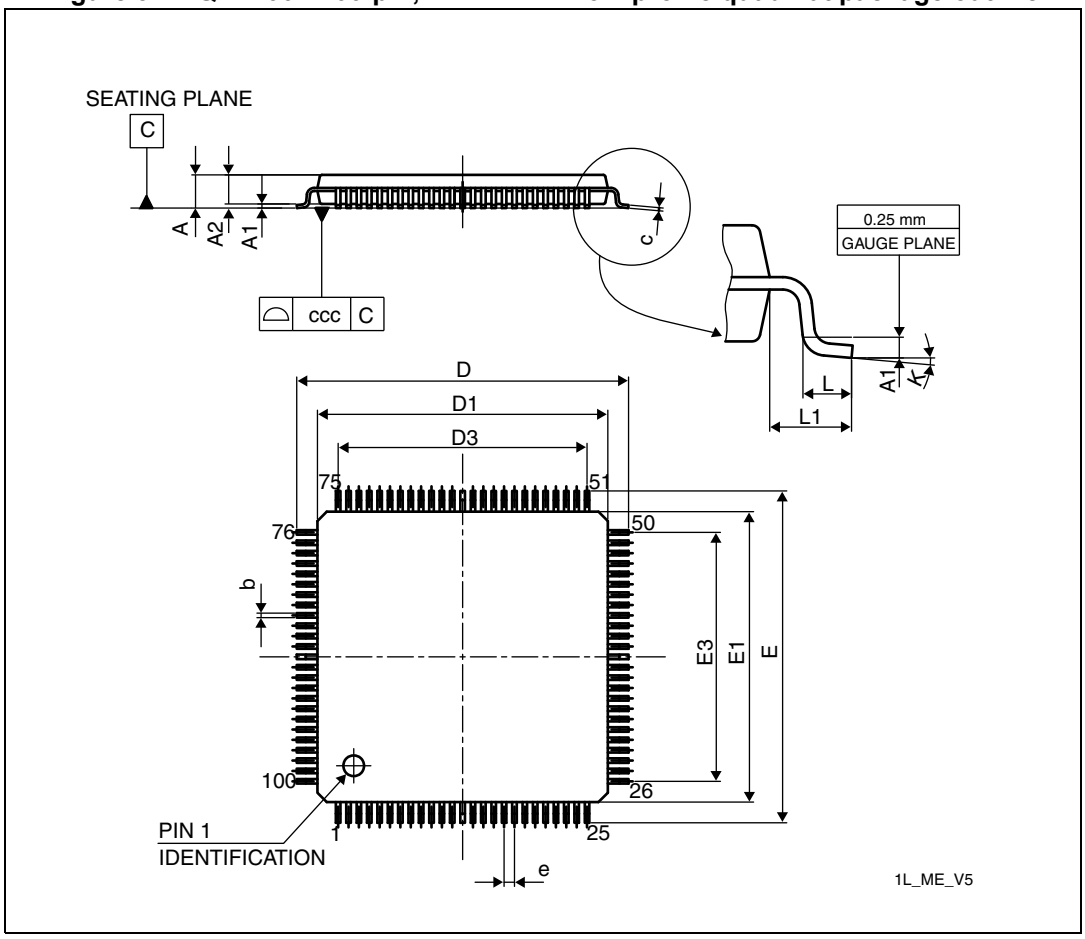
1. Guaranteed by characterization results.
2. Guaranteed by design.
3. Shortest sampling time can be determined in the application by multiple iterations.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

6.1 LQFP100 package information

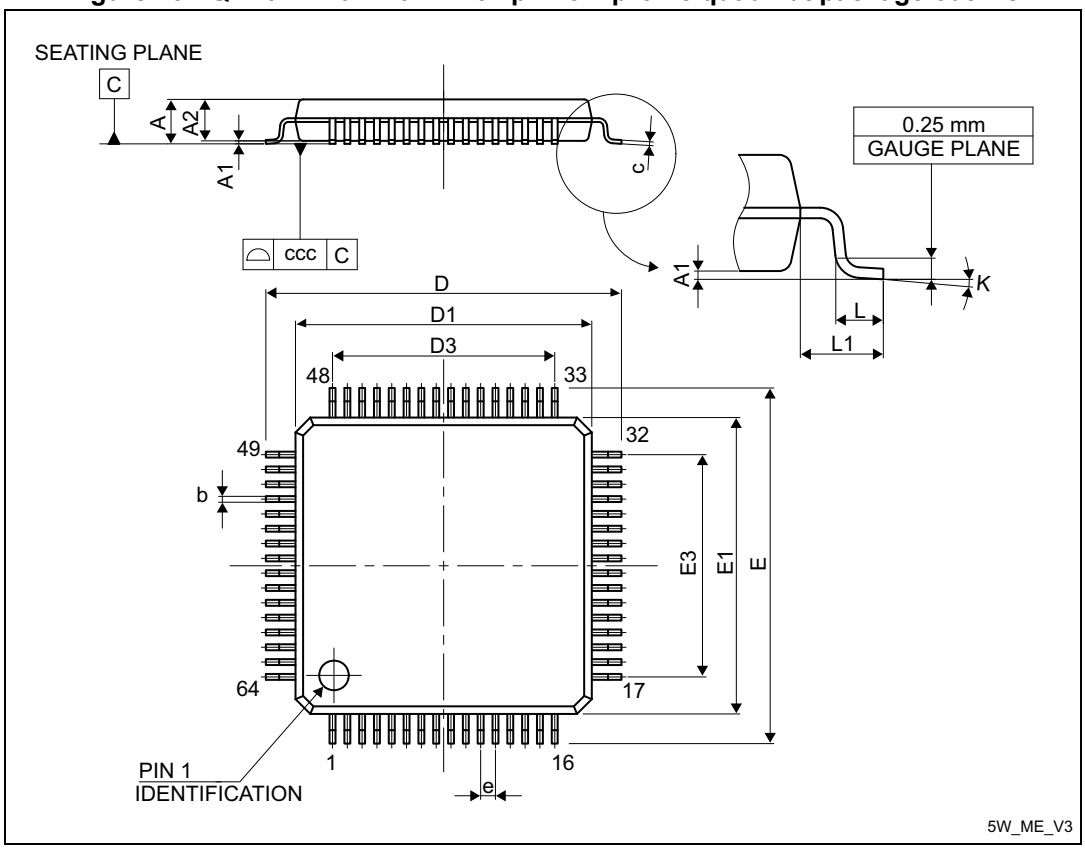
Figure 37. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale. Dimensions are in millimeters.

6.2 LQFP64 package information

Figure 40.LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline



1. Drawing is not in scale.

Table 49. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

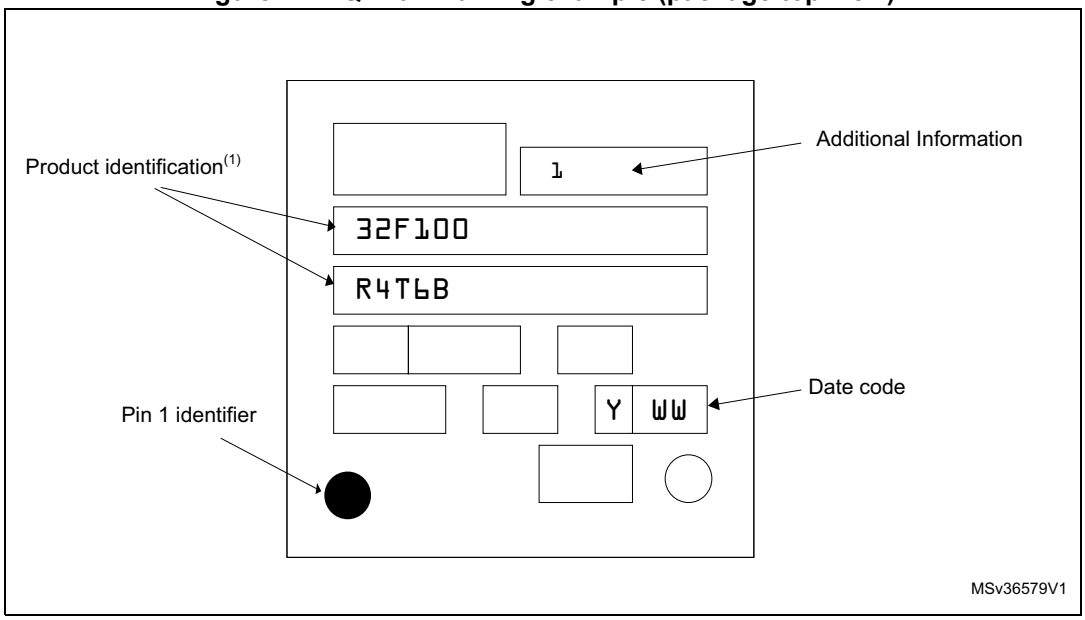
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-

Device marking for LQFP64

The following figure gives an example of topside marking and pin 1 position identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 42. LQFP64 marking example (package top view)



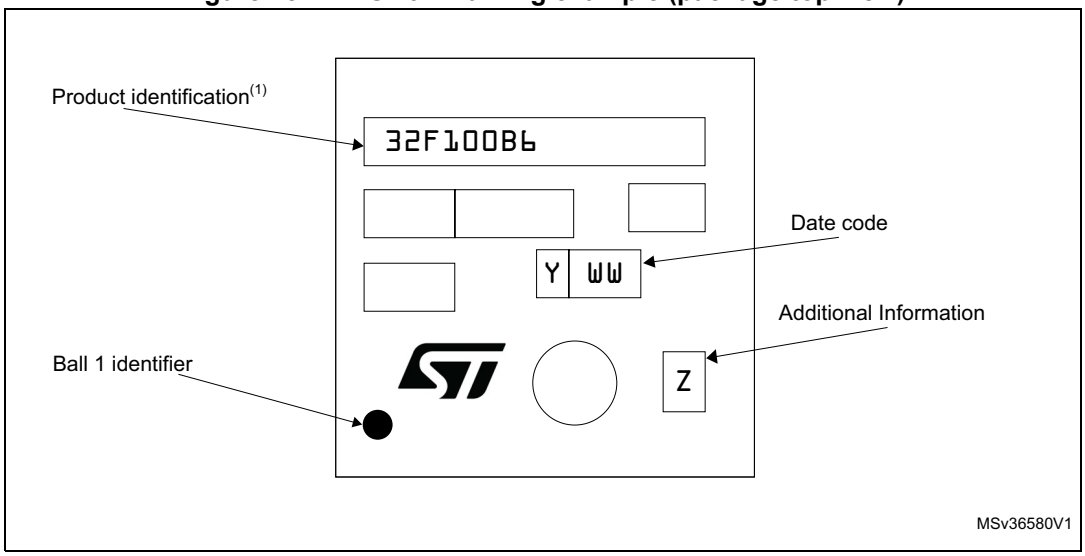
1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Device marking for TFBGA64

The following figure gives an example of topside marking and pin 1 position identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 45. TFBGA64 marking example (package top view)



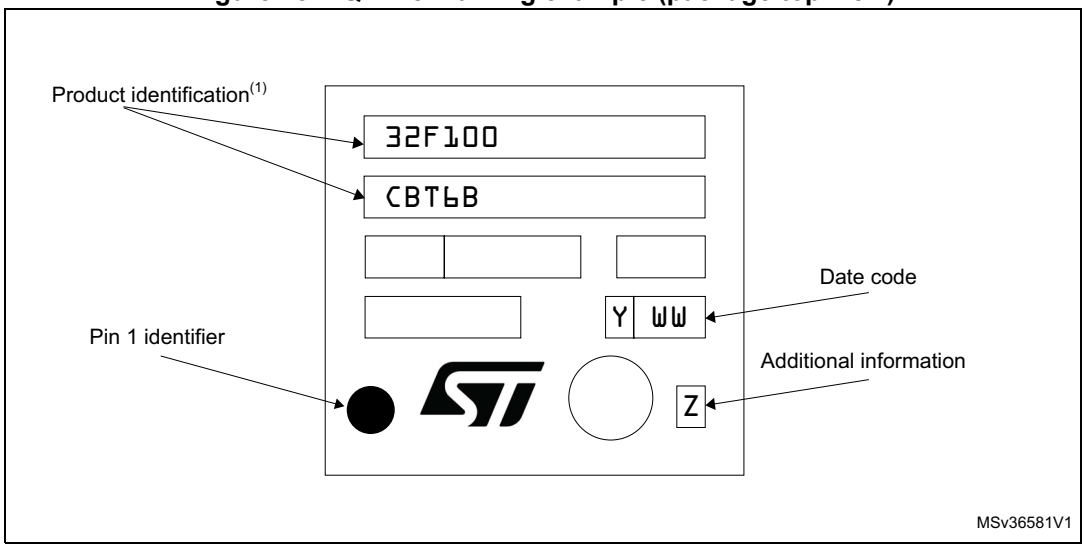
1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Device marking for LQFP48

The following figure gives an example of topside marking and pin 1 position identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 48. LQFP48 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 55. Document revision history (continued)

Date	Revision	Changes
30-Mar-2010	3	Revision history corrected. Updated *Table 6: Current characteristics* Values and note updated in *Table 16: Typical current consumption in Run mode, code with data processing running from Flash* and *Table 17: Typical current consumption in Sleep mode, code running from Flash or RAM*. Updated *Table 15: Typical and maximum current consumptions in Stop and Standby modes* Added *Figure 14: Typical current consumption on VBAT with RTC on vs. temperature at different VBAT values* Typical consumption for ADC1 corrected in *Table 18: Peripheral current consumption*. *Maximum current consumption* and *Typical current consumption*: frequency conditions corrected. *Output driving current* corrected. Updated *Table 30: EMI characteristics* f_{ADC} max corrected in *Table 42: ADC characteristics*. Small text changes.
06-May-2010	4	Updated *Table 31: ESD absolute maximum ratings on page 55* and *Table 32: Electrical sensitivities on page 56* Updated *Table 44: ADC accuracy - limited test conditions on page 70* and *Table 45: ADC accuracy on page 70*
12-Jul-2010	5	Updated *Table 24: LSI oscillator characteristics on page 51* Updated *Table 44: ADC accuracy - limited test conditions on page 70* and *Table 45: ADC accuracy on page 70*
04-Apr-2011	6	Updated *Figure 2: Clock tree* to add FLITF clock Updated footnotes below *Table 5: Voltage characteristics on page 33* and *Table 6: Current characteristics on page 34* Updated tw min in *Table 19: High-speed external user clock characteristics on page 46* Updated startup time in *Table 22: LSE oscillator characteristics (fLSE = 32.768 kHz) on page 49* Updated *Table 23: HSI oscillator characteristics on page 50* Added *Section 5.3.12: I/O current injection characteristics on page 56* Updated *Table 34: I/O static characteristics on page 57* Corrected TTL and CMOS designations in *Table 35: Output voltage characteristics on page 60* Removed note on remapped characteristics from *Table 41: SPI characteristics on page 66*