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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	37
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f100c8t7b

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2 Description

The STM32F100x4, STM32F100x6, STM32F100x8 and STM32F100xB microcontrollers incorporate the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a 24 MHz frequency, high-speed embedded memories (Flash memory up to 128 Kbytes and SRAM up to 8 Kbytes), and an extensive range of enhanced peripherals and I/Os connected to two APB buses. All devices offer standard communication interfaces (up to two I²Cs, two SPIs, one HDMI CEC, and up to three USARTs), one 12-bit ADC, two 12-bit DACs, up to six general-purpose 16-bit timers and an advanced-control PWM timer.

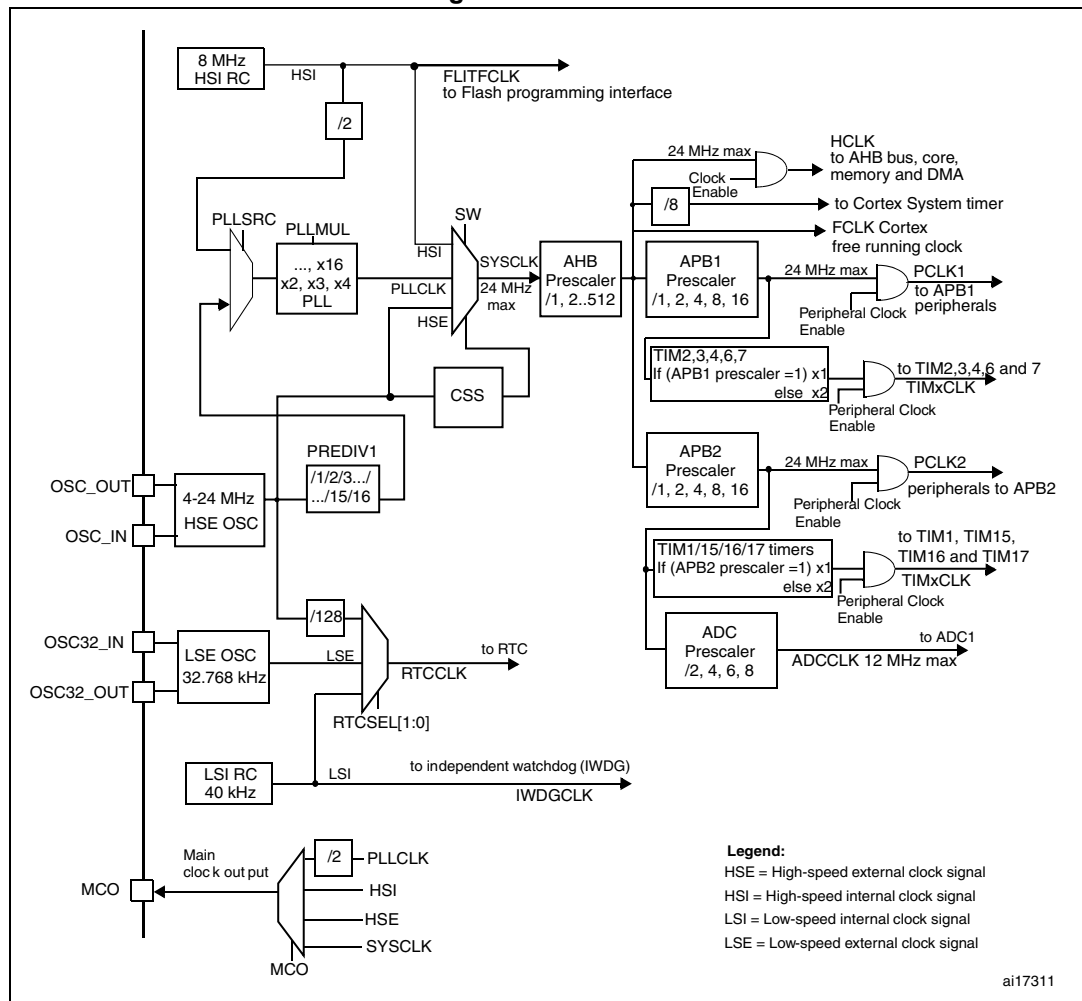
The STM32F100xx low- and medium-density devices operate in the – 40 to + 85 °C and – 40 to + 105 °C temperature ranges, from a 2.0 to 3.6 V power supply.

A comprehensive set of power-saving mode allows the design of low-power applications.

These microcontrollers include devices in three different packages ranging from 48 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included.

These features make these microcontrollers suitable for a wide range of applications such as application control and user interfaces, medical and hand-held equipment, PC and gaming peripherals, GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms, and HVACs.

Figure 2. Clock tree



1. To have an ADC conversion time of 1.2 μ s, APB2 must be at 24 MHz.

2.2.6 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 18 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 80 GPIOs can be connected to the 16 external interrupt lines.

2.2.7 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-24 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 24 MHz.

2.2.8 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1. For further details please refer to AN2606.

2.2.9 Power supply schemes

- $V_{DD} = 2.0$ to 3.6 V: External power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA} , $V_{DDA} = 2.0$ to 3.6 V: External analog power supplies for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC or DAC is used).
 V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.
- $V_{BAT} = 1.8$ to 3.6 V: Power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

2.2.10 Power supply supervisor

The device has an integrated power on reset (POR)/power down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is

2.2.18 Serial peripheral interface (SPI)

Up to two SPIs are able to communicate up to 12 Mbit/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits.

Both SPIs can be served by the DMA controller.

2.2.19 HDMI (high-definition multimedia interface) consumer electronics control (CEC)

The STM32F100xx value line embeds a HDMI-CEC controller that provides hardware support of consumer electronics control (CEC) (Appendix supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead.

2.2.20 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

2.2.21 Remap capability

This feature allows the use of a maximum number of peripherals in a given application. Indeed, alternate functions are available not only on the default pins but also on other specific pins onto which they are remappable. This has the advantage of making board design and port usage much more flexible.

For details refer to [Table 4: Low & medium-density STM32F100xx pin definitions](#); it shows the list of remappable alternate functions and the pins onto which they can be remapped. See the STM32F10xxx reference manual for software considerations.

2.2.22 ADC (analog-to-digital converter)

The 12-bit analog to digital converter has up to 16 external channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

2.2.23 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in noninverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- up to 10-bit output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channels' independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the STM32F100xx. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

2.2.24 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between $2\text{ V} < V_{DDA} < 3.6\text{ V}$. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.2.25 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

1. I = input, O = output, S = supply, HiZ= high impedance.
2. FT= 5 V tolerant.
3. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripherals that is included. For example, if a device has only one SPI, two USARTs and two timers, they will be called SPI1, USART1 & USART2 and TIM2 & TIM 3, respectively. Refer to [Table 2 on page 11](#).
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch and since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is restricted: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must *not* be used as a current source (e.g. to drive an LED).
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
7. The pins number 2 and 3 in the VFQFPN36 package, 5 and 6 in the LQFP48 and LQFP64 packages and C1 and C2 in the TFBGA64 package are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.
8. Unlike in the LQFP64 package, there is no PC3 in the TFBGA64 package. The V_{REF+} functionality is provided instead.
9. I2C2 is not present on low-density value line devices.
10. SPI2 is not present on low-density value line devices.
11. TIM4 is not present on low-density value line devices.
12. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS} .

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25\text{ }^{\circ}\text{C}$ and $T_A = T_{A\text{max}}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation ($\text{mean} \pm 3\Sigma$).

5.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 3.3\text{ V}$ (for the $2\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated ($\text{mean} \pm 2\Sigma$).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 8](#).

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 9](#).

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 22](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Note: For C_{L1} and C_{L2} it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF. For further details, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF) it is strongly recommended to use a resonator with a load capacitance $C_L \leq 7$ pF. Never use a resonator with a load capacitance of 12.5 pF.

Example: if you choose a resonator with a load capacitance of $C_L = 6$ pF, and $C_{stray} = 2$ pF, then $C_{L1} = C_{L2} = 8$ pF.

Table 22. LSE oscillator characteristics ($f_{LSE} = 32.768$ kHz)⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	5	-	MΩ
$C_{L1} C_{L2}^{(2)}$	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S) ⁽³⁾	$R_S = 30$ KΩ	-	-	15	pF
I_2	LSE driving current	$V_{DD} = 3.3$ V $V_{IN} = V_{SS}$	-	-	1.4	μA
g_m	Oscillator transconductance	-	5	-	-	μA/V
$t_{SU(LSE)}^{(4)}$	Startup time	V_{DD} is stabilized	$T_A = 50$ °C	-	1.5	-
			$T_A = 25$ °C	-	2.5	-
			$T_A = 10$ °C	-	4	-
			$T_A = 0$ °C	-	6	-
			$T_A = -10$ °C	-	10	-
			$T_A = -20$ °C	-	17	-
			$T_A = -30$ °C	-	32	-
			$T_A = -40$ °C	-	60	-

- Guaranteed by characterization results.
- Refer to the note and caution paragraphs above the table.
- The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value for example MSIV-TIN32.768 kHz. Refer to crystal manufacturer for more details
- $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

5.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in [Table 34](#) are derived from tests performed under the conditions summarized in [Table 8](#). All I/Os are CMOS and TTL compliant.

Table 34. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard I/O input low level voltage	-	-0.3	-	$0.28 \cdot (V_{DD} - 2 \text{ V}) + 0.8 \text{ V}$	V
	I/O FT ⁽¹⁾ input low level voltage		-0.3	-	$0.32 \cdot (V_{DD} - 2 \text{ V}) + 0.75 \text{ V}$	
V_{IH}	Standard I/O input high level voltage		$0.41 \cdot (V_{DD} - 2 \text{ V}) + 1.3 \text{ V}$	-	$V_{DD} + 0.3$	
	I/O FT ⁽¹⁾ input high level voltage	$V_{DD} > 2 \text{ V}$	$0.42 \cdot (V_{DD} - 2) + 1 \text{ V}$	-	5.5	
		$V_{DD} \leq 2 \text{ V}$			5.2	
V_{hys}	Standard I/O Schmitt trigger voltage hysteresis ⁽²⁾	-	200	-	-	mV
	I/O FT Schmitt trigger voltage hysteresis ⁽²⁾		$5\% V_{DD}^{(3)}$	-	-	mV
I_{lkg}	Input leakage current ⁽⁴⁾	$V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os	-	-	± 1	μA
		$V_{IN} = 5 \text{ V}$ I/O FT	-	-	3	
R_{PU}	Weak pull-up equivalent resistor ⁽⁵⁾	$V_{IN} = V_{SS}$	30	40	50	$k\Omega$
R_{PD}	Weak pull-down equivalent resistor ⁽⁵⁾	$V_{IN} = V_{DD}$	30	40	50	$k\Omega$
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. FT = 5V tolerant. To sustain a voltage higher than $V_{DD} + 0.3$ the internal pull-up/pull-down resistors must be disabled.
2. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by design.
3. With a minimum of 100 mV.
4. Leakage could be higher than max. if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in [Figure 22](#) and [Figure 23](#) for standard I/Os, and in [Figure 24](#) and [Figure 25](#) for 5 V tolerant I/Os.

Figure 22. Standard I/O input characteristics - CMOS port

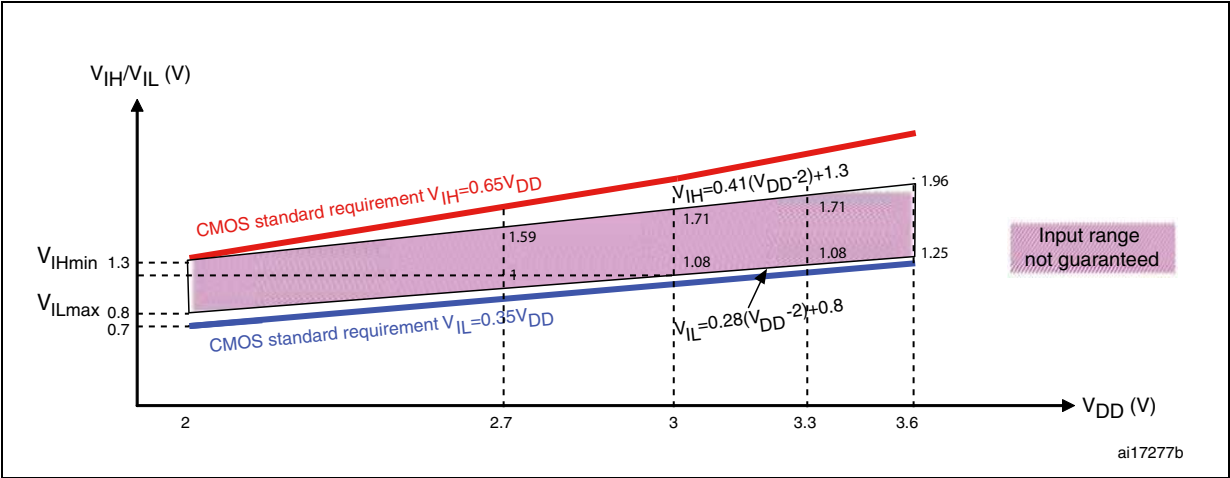
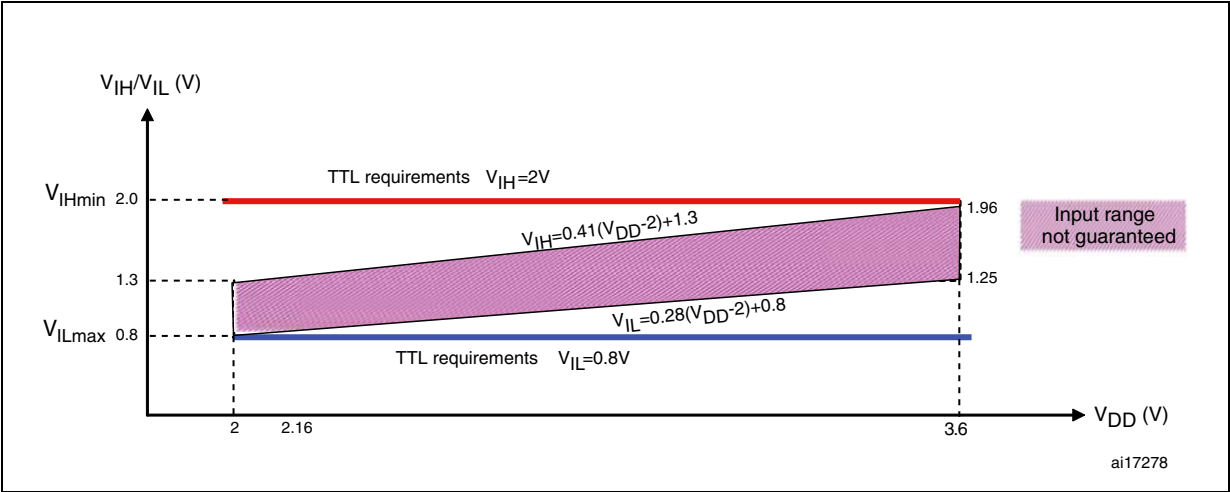


Figure 23. Standard I/O input characteristics - TTL port



Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 26](#) and [Table 36](#), respectively.

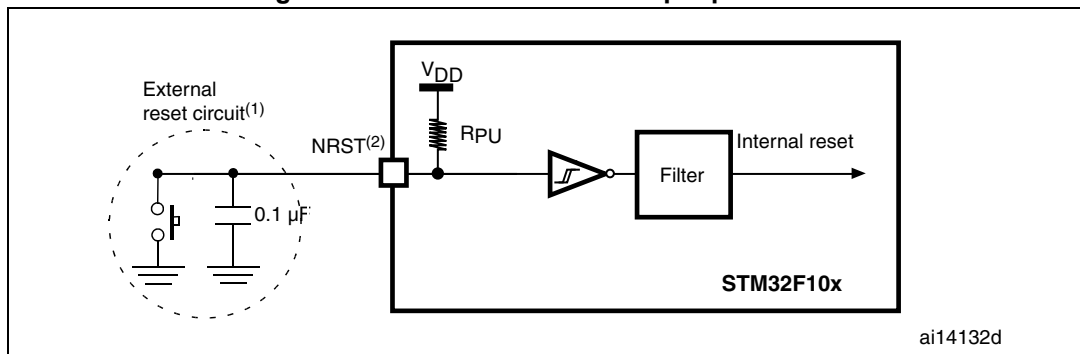
Unless otherwise specified, the parameters given in [Table 36](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 8](#).

Table 36. I/O AC characteristics⁽¹⁾

MODEx [1:0] bit value ⁽¹⁾	Symbol	Parameter	Conditions	Max	Unit
10	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽²⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	2 ⁽³⁾	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	125 ⁽³⁾	ns
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time		125 ⁽³⁾	
01	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽²⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	10 ⁽³⁾	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	25 ⁽³⁾	ns
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time		25 ⁽³⁾	
11	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽²⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	24	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time	$C_L = 30 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	5 ⁽³⁾	ns
			$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	8 ⁽³⁾	
			$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 2.7 \text{ V}$	12 ⁽³⁾	
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time	$C_L = 30 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	5 ⁽³⁾	
			$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	8 ⁽³⁾	
			$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 2.7 \text{ V}$	12 ⁽³⁾	
-	$t_{\text{EXTI}pw}$	Pulse width of external signals detected by the EXTI controller	-	10 ⁽³⁾	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in [Figure 26](#).
3. Guaranteed by design.

Figure 27. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in [Table 37](#). Otherwise the reset will not be taken into account by the device.

5.3.15 TIMx characteristics

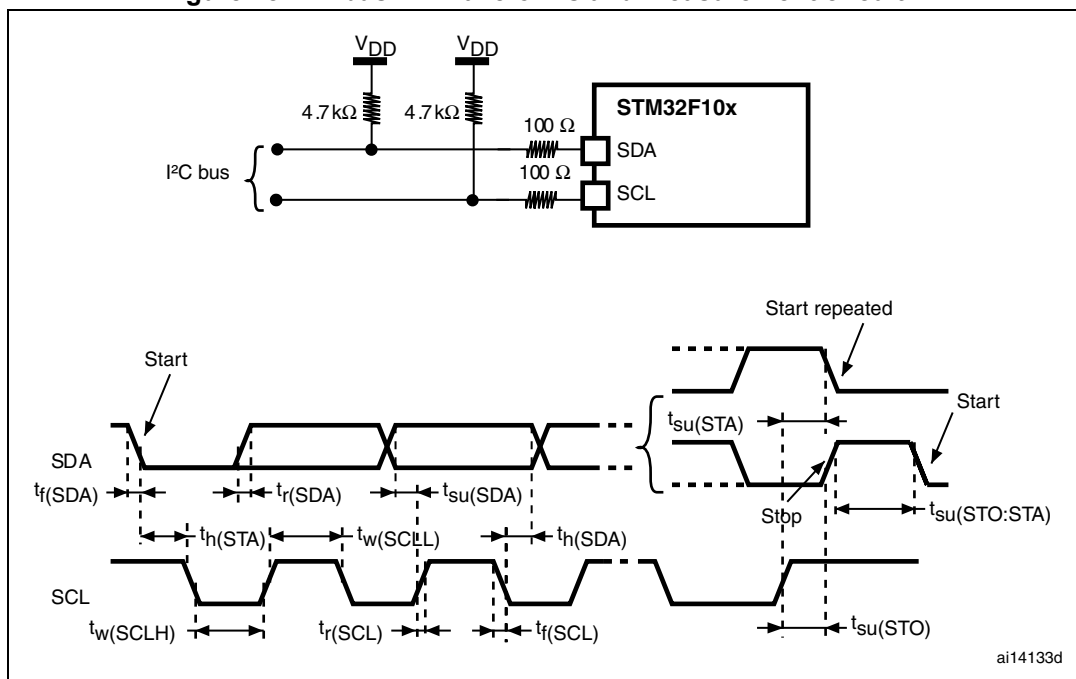
The parameters given in [Table 38](#) are guaranteed by design.

Refer to [Section 5.3.12: I/O current injection characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 38. TIMx characteristics

Symbol	Parameter	Conditions ⁽¹⁾	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 24 \text{ MHz}$	41.7	-	ns
f_{EXT}	Timer external clock frequency on CHx ⁽²⁾	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK} = 24 \text{ MHz}$	0	12	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock period when the internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 24 \text{ MHz}$	-	2730	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536×65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 24 \text{ MHz}$	-	178	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3, TIM4, TIM15, TIM16 and TIM17 timers.
2. CHx is used as a general term to refer to CH1 to CH4 for TIM1, TIM2, TIM3 and TIM4, to the CH1 to CH2 for TIM15, and to CH1 for TIM16 and TIM17.

Figure 28. I²C bus AC waveforms and measurement circuit⁽¹⁾

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 40. SCL frequency ($f_{PCLK1} = 24 \text{ MHz}$, $V_{DD} = 3.3 \text{ V}$)⁽¹⁾⁽²⁾

$f_{SCL} \text{ (kHz)}^{(3)}$	I2C_CCR value
	$R_P = 4.7 \text{ k}\Omega$
400	0x8011
300	0x8016
200	0x8021
100	0x0064
50	0x00C8
20	0x01F4

- R_P = External pull-up resistance, f_{SCL} = I²C speed,
- For speeds around 400 kHz, the tolerance on the achieved speed is of $\pm 2\%$. For other speed ranges, the tolerance on the achieved speed $\pm 1\%$. These variations depend on the accuracy of the external components used to design the application.
- Guaranteed by design.

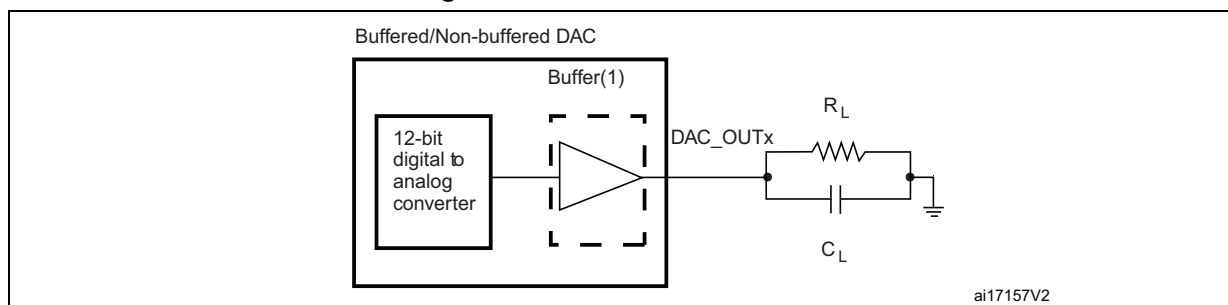
Table 46. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max ⁽¹⁾	Unit	Comments
Offset ⁽¹⁾	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$)	-	-	± 10	mV	Given for the DAC in 12-bit configuration
		-	-	± 3	LSB	Given for the DAC in 10-bit at $V_{REF+} = 3.6$ V
		-	-	± 12	LSB	Given for the DAC in 12-bit at $V_{REF+} = 3.6$ V
Gain error ⁽¹⁾	Gain error	-	-	± 0.5	%	Given for the DAC in 12bit configuration
$t_{SETTLING}^{(1)}$	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ± 1 LSB)	-	3	4	μ s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ k Ω
Update rate ⁽¹⁾	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ k Ω
$t_{WAKEUP}^{(1)}$	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	μ s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ k Ω input code between lowest and highest possible ones.
PSRR+ (1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	-	-67	-40	dB	No R_{LOAD} , $C_{LOAD} = 50$ pF

1. Guaranteed by characterization results.

2. Guaranteed by design.

Figure 36. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.5.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in [Table 54: Ordering information scheme](#).

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F10xxx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example: high-performance application

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax} = 82\text{ }^{\circ}\text{C}$ (measured according to JESD51-2),
 $I_{DDmax} = 50\text{ mA}$, $V_{DD} = 3.5\text{ V}$, maximum 20 I/Os used at the same time in output at low level with $I_{OL} = 8\text{ mA}$, $V_{OL} = 0.4\text{ V}$ and maximum 8 I/Os used at the same time in output mode at low level with $I_{OL} = 20\text{ mA}$, $V_{OL} = 1.3\text{ V}$

$$P_{INTmax} = 50\text{ mA} \times 3.5\text{ V} = 175\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} + 8 \times 20\text{ mA} \times 1.3\text{ V} = 272\text{ mW}$$

$$\text{This gives: } P_{INTmax} = 175\text{ mW and } P_{IOmax} = 272\text{ mW}$$

$$P_{Dmax} = 175 + 272 = 447\text{ mW}$$

$$\text{Thus: } P_{Dmax} = 447\text{ mW}$$

Using the values obtained in [Table 53](#) T_{Jmax} is calculated as follows:

– For LQFP64, $45\text{ }^{\circ}\text{C/W}$

$$T_{Jmax} = 82\text{ }^{\circ}\text{C} + (45\text{ }^{\circ}\text{C/W} \times 447\text{ mW}) = 82\text{ }^{\circ}\text{C} + 20.1\text{ }^{\circ}\text{C} = 102.1\text{ }^{\circ}\text{C}$$

This is within the range of the suffix 6 version parts ($-40 < T_J < 105\text{ }^{\circ}\text{C}$).

In this case, parts must be ordered at least with the temperature range suffix 6 (see [Table 54: Ordering information scheme](#)).

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax} = 115\text{ }^{\circ}\text{C}$ (measured according to JESD51-2),
 $I_{DDmax} = 20\text{ mA}$, $V_{DD} = 3.5\text{ V}$, maximum 20 I/Os used at the same time in output at low level with $I_{OL} = 8\text{ mA}$, $V_{OL} = 0.4\text{ V}$

$$P_{INTmax} = 20\text{ mA} \times 3.5\text{ V} = 70\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} = 64\text{ mW}$$

$$\text{This gives: } P_{INTmax} = 70\text{ mW and } P_{IOmax} = 64\text{ mW:}$$

$$P_{Dmax} = 70 + 64 = 134\text{ mW}$$

$$\text{Thus: } P_{Dmax} = 134\text{ mW}$$

Using the values obtained in [Table 53](#) T_{Jmax} is calculated as follows:

– For LQFP100, 46 °C/W

$$T_{Jmax} = 115\text{ °C} + (46\text{ °C/W} \times 134\text{ mW}) = 115\text{ °C} + 6.2\text{ °C} = 121.2\text{ °C}$$

This is within the range of the suffix 7 version parts ($-40 < T_J < 125\text{ °C}$).

In this case, parts must be ordered at least with the temperature range suffix 7 (see [Table 54: Ordering information scheme](#)).

Figure 49. LQFP100 P_D max vs. T_A

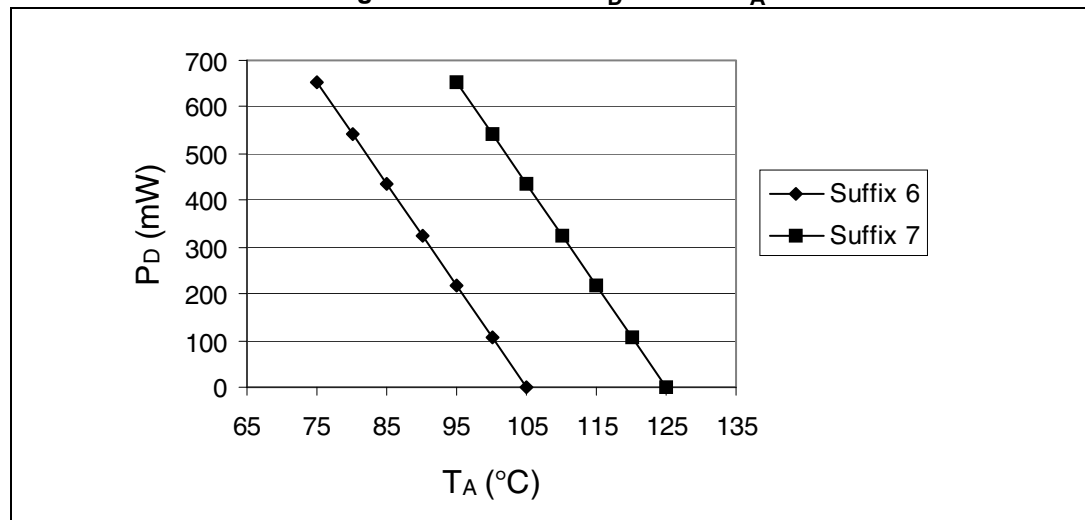


Table 55. Document revision history (continued)

Date	Revision	Changes
08-Jun-2012	7	<p>Updated Table 6: Current characteristics on page 34</p> <p>Updated Table 39: I2C characteristics on page 64</p> <p>Corrected note “non-robust “ in Section 5.3.17: 12-bit ADC characteristics on page 68</p> <p>Updated Section 5.3.13: I/O port characteristics on page 57</p> <p>Updated Section 2.2.20: GPIOs (general-purpose inputs/outputs) on page 20</p> <p>Updated Table 4: Low & medium-density STM32F100xx pin definitions on page 24</p> <p>Updated Section 5.3.1: General operating conditions on page 34</p> <p>Updated Table 14: Maximum current consumption in Sleep mode, code running from Flash or RAM on page 39</p>
08-Jun-2015	8	<p>Updated Table 18: Peripheral current consumption, Table 31: ESD absolute maximum ratings, Table 48: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data, Table 49: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data, Table 50: TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package mechanical data, Table 51: TFBGA64 recommended PCB design rules (0.5 mm pitch BGA) and Table 52: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data.</p> <p>Updated Figure 37: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline, Figure 38: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint, Figure 40: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline, Figure 41: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint, Figure 43: TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch thin profile fine pitch ball grid array package outline, Figure 44: TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array, recommended footprint, Figure 46: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline and Figure 47: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint.</p> <p>Added Figure 39: LQFP100 marking example (package top view), Figure 42: LQFP64 marking example (package top view) Figure 45: TFBGA64 marking example (package top view) and Figure 48: LQFP48 marking example (package top view).</p>
21-Nov-2016	9	<p>Updated:</p> <ul style="list-style-type: none"> – Figure 7: Memory map – Figure 18: High-speed external clock source AC timing diagram – Figure 19: Low-speed external clock source AC timing diagram – Table 19: High-speed external user clock characteristics – Table 20: Low-speed external user clock characteristics – Table 42: ADC characteristics