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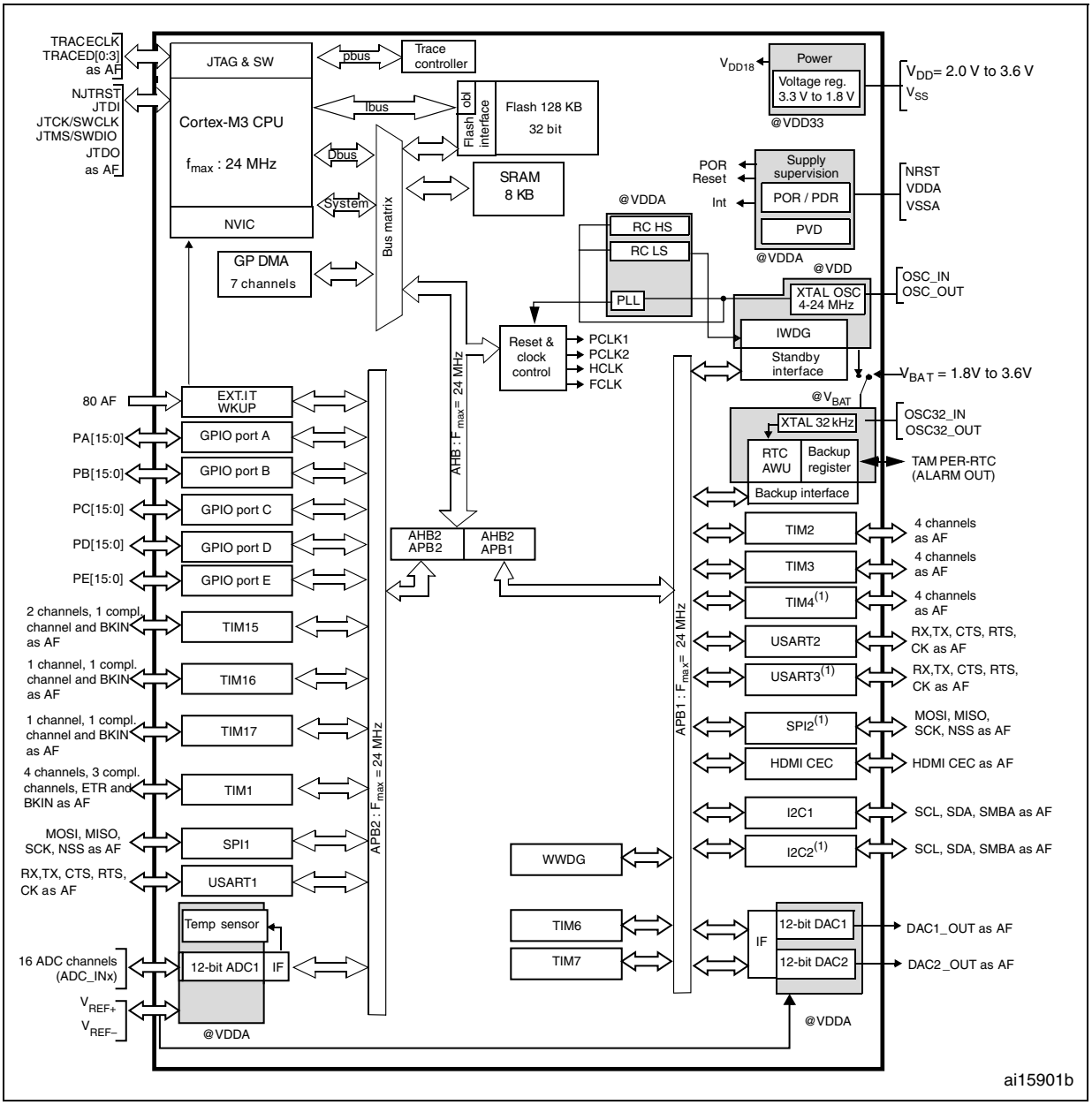
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	37
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f100c8t7btr

List of tables

Figure 1. STM32F100xx value line block diagram



1. Peripherals not present in low-density value line devices.
2. AF = alternate function on I/O port pin.
3. T_A = –40 °C to +85 °C (junction temperature up to 105 °C) or T_A = –40 °C to +105 °C (junction temperature up to 125 °C).

Figure 4. STM32F100xx value line LQFP64 pinout

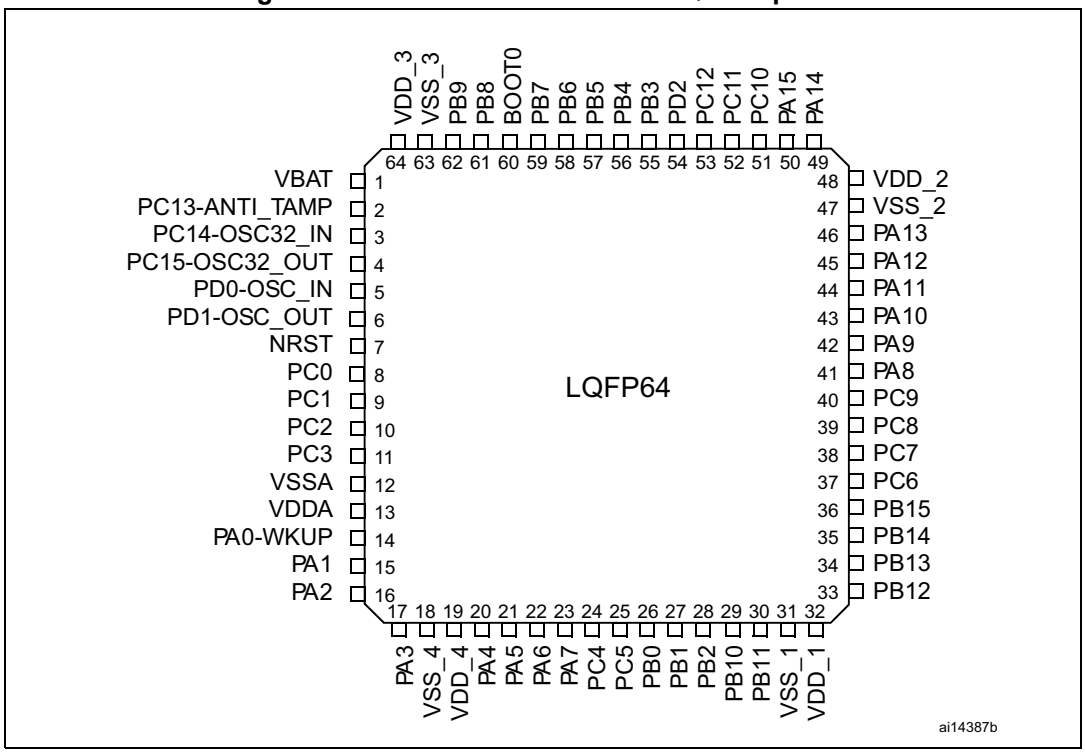


Figure 5. STM32F100xx value line LQFP48 pinout

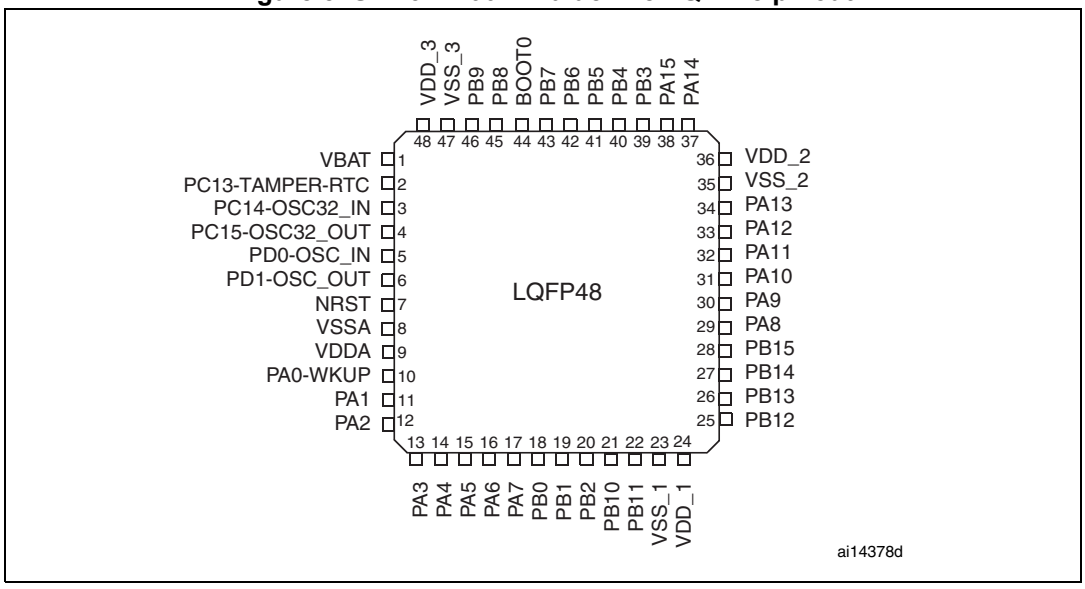


Figure 6. STM32F100xx value line TFBGA64 ballout

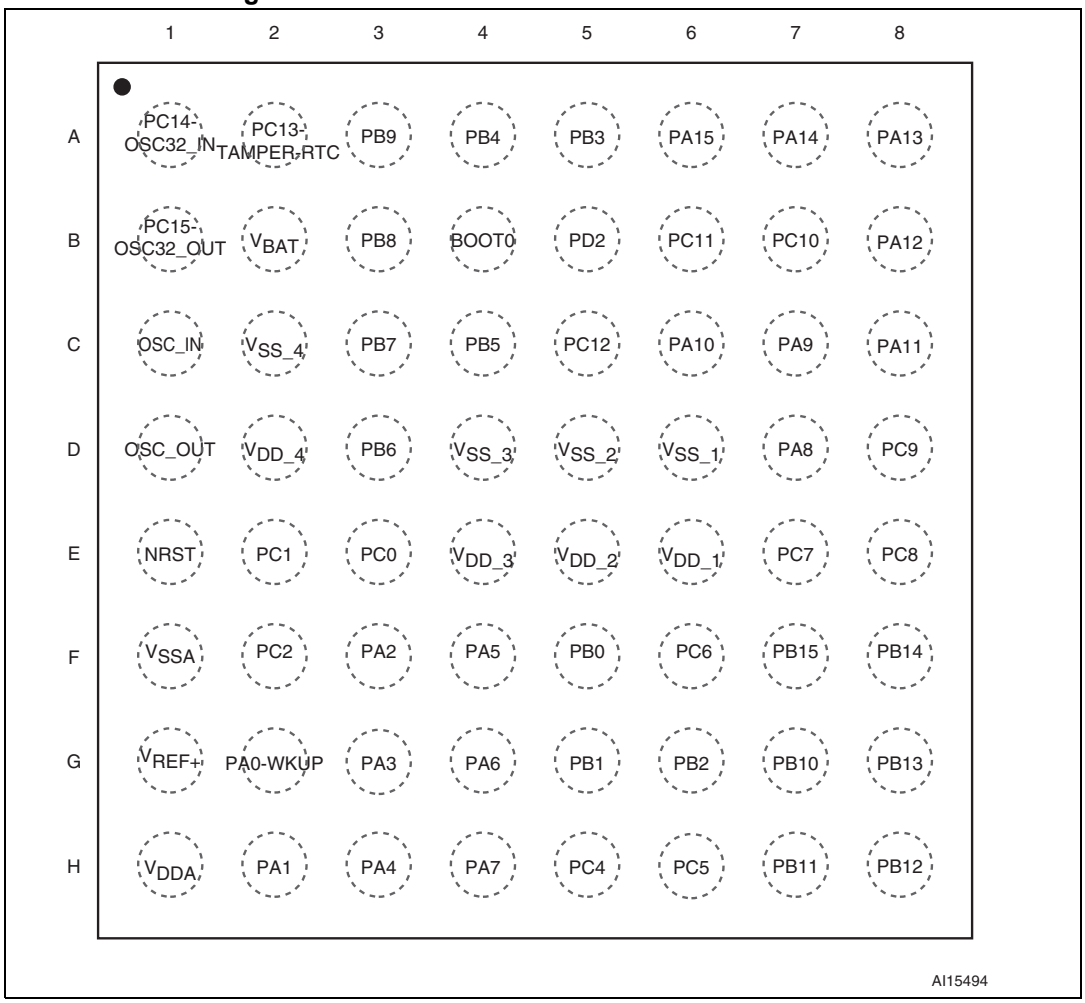


Table 4. Low & medium-density STM32F100xx pin definitions

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3)(4)	
LQFP100	LQFP64	TFBGA64	LQFP48					Default	Remap
1	-	-	-	PE2	I/O	FT	PE2	TRACECLK	-
2	-	-	-	PE3	I/O	FT	PE3	TRACED0	-
3	-	-	-	PE4	I/O	FT	PE4	TRACED1	-
4	-	-	-	PE5	I/O	FT	PE5	TRACED2	-
5	-	-	-	PE6	I/O	FT	PE6	TRACED3	-
6	1	B2	1	V_{BAT}	S	-	V_{BAT}	-	-
7	2	A2	2	PC13-TAMPER-RTC(5)	I/O	-	PC13(6)	TAMPER-RTC	-
8	3	A1	3	PC14-OSC32_IN(5)	I/O	-	PC14(6)	OSC32_IN	-

1. I = input, O = output, S = supply, HiZ= high impedance.
2. FT= 5 V tolerant.
3. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripherals that is included. For example, if a device has only one SPI, two USARTs and two timers, they will be called SPI1, USART1 & USART2 and TIM2 & TIM 3, respectively. Refer to *Table 2 on page 11*.
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch and since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is restricted: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must *not* be used as a current source (e.g. to drive an LED).
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.
7. The pins number 2 and 3 in the VFQFPN36 package, 5 and 6 in the LQFP48 and LQFP64 packages and C1 and C2 in the TFBGA64 package are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.
8. Unlike in the LQFP64 package, there is no PC3 in the TFBGA64 package. The V_{REF+} functionality is provided instead.
9. I2C2 is not present on low-density value line devices.
10. SPI2 is not present on low-density value line devices.
11. TIM4 is not present on low-density value line devices.
12. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.

Figure 8. Pin loading conditions

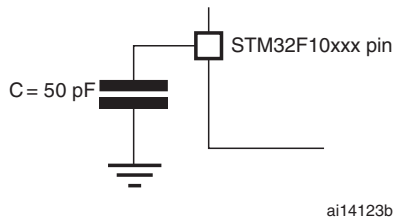
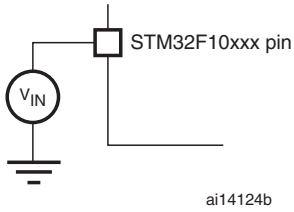
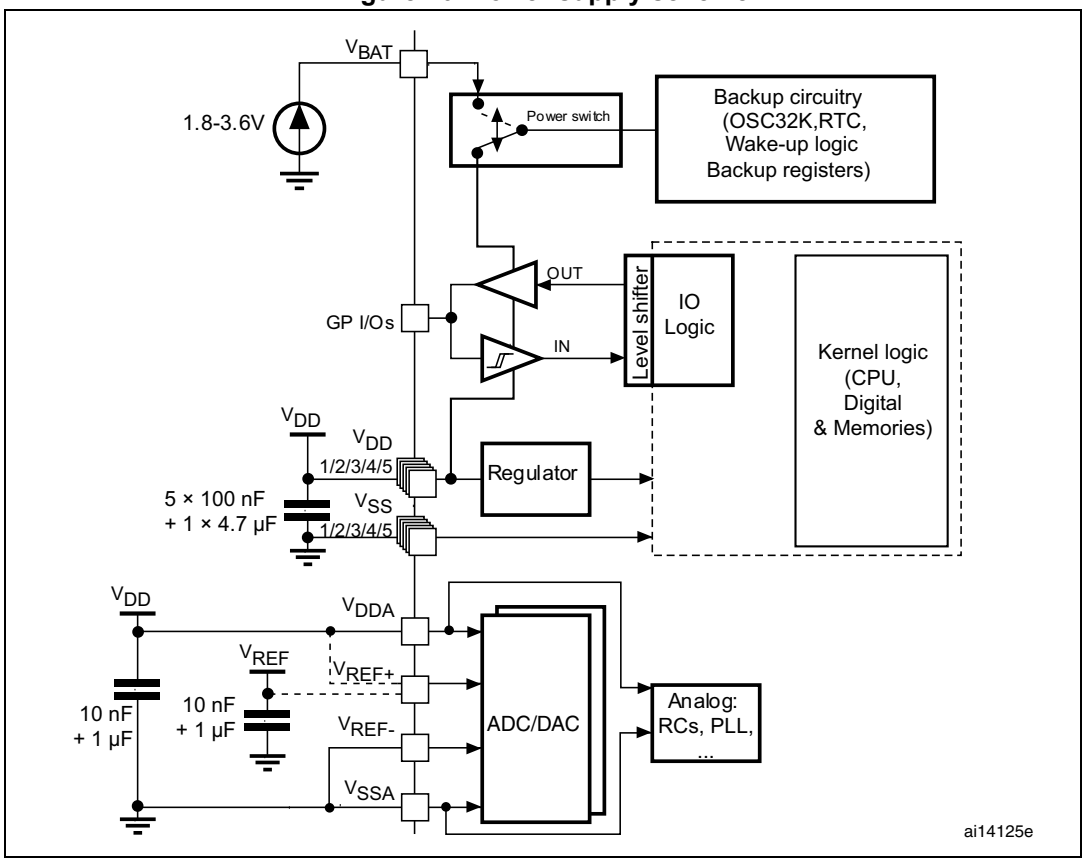


Figure 9. Pin input voltage



5.1.6 Power supply scheme

Figure 10. Power supply scheme



Caution: In *Figure 10*, the 4.7 µF capacitor must be connected to V_{DD3}.

Table 8. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(2)	LQFP100	-	434	mW
		LQFP64	-	444	
		TFBGA64	-	308	
		LQFP48	-	363	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low power dissipation(3)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low power dissipation(3)	–40	125	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

1. When the ADC is used, refer to *Table 42: ADC characteristics*.
2. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed $T_J$max (see *Table 6.5: Thermal characteristics on page 89*).
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed $T_J$max (see *Table 6.5: Thermal characteristics on page 89*).

Note: It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.

5.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Table 9. Operating conditions at power-up / power-down

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	0	∞	µs/V
	V_{DD} fall time rate	20	∞	

5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 10* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 12. Maximum current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock (2), all peripherals enabled	24 MHz	15.4	15.7	mA
			16 MHz	11	11.5	
			8 MHz	6.7	6.9	
		External clock(2), all peripherals disabled	24 MHz	10.3	10.5	
			16 MHz	7.8	8.1	
			8 MHz	5.1	5.3	

1. Guaranteed by characterization results.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 13. Maximum current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock (2), all peripherals enabled	24 MHz	14.5	15	mA
			16 MHz	10	10.5	
			8 MHz	6	6.3	
		External clock(2) all peripherals disabled	24MHz	9.3	9.7	
			16 MHz	6.8	7.2	
			8 MHz	4.4	4.7	

1. Guaranteed by characterization, tested in production at V_{DD} max, f_{HCLK} max.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 15. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)			Max		Unit
			V_{DD}/ V_{BAT} = 2.0 V	V_{DD}/ V_{BAT} = 2.4 V	V_{DD}/ V_{BAT} = 3.3 V	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in Run mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	23.5	24	190	350	µA
		Regulator in Low-Power mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	13.5	14	170	330	
	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog ON	-	2.6	3.4	-	-	
		Low-speed internal RC oscillator ON, independent watchdog OFF	-	2.4	3.2	-	-	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	-	1.7	2	4	5	
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	0.9	1.1	1.4	1.9	2.2	

1. Typical values are measured at T_A = 25 °C.

Figure 14. Typical current consumption on V_{BAT} with RTC on vs. temperature at different V_{BAT} values

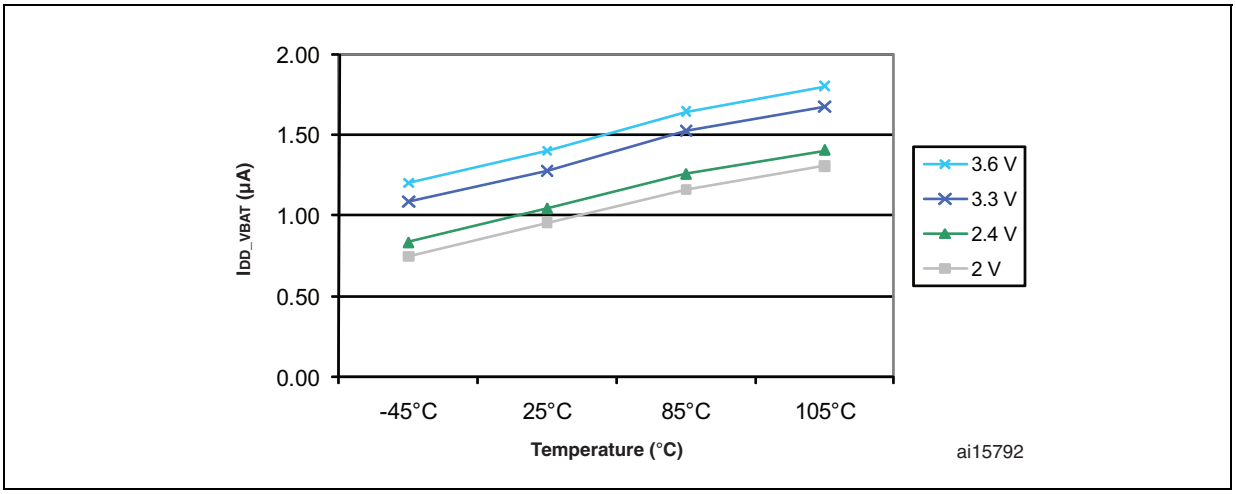


Table 16. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typical values(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Run mode	Running on high-speed external clock with an 8 MHz crystal(3)	24 MHz	12.8	9.3	mA
			16 MHz	9.3	6.6	
			8 MHz	5.1	3.9	
			4 MHz	3.2	2.5	
			2 MHz	2.1	1.75	
			1 MHz	1.55	1.4	
			500 kHz	1.3	1.2	
			125 kHz	1.1	1.05	
		Running on high-speed internal RC (HSI)	24 MHz	12.2	8.6	
			16 MHz	8.5	6	
			8 MHz	4.6	3.3	
			4 MHz	2.6	1.9	
			2 MHz	1.5	1.15	
			1 MHz	0.9	0.8	
			500 kHz	0.65	0.6	
			125 kHz	0.45	0.43	

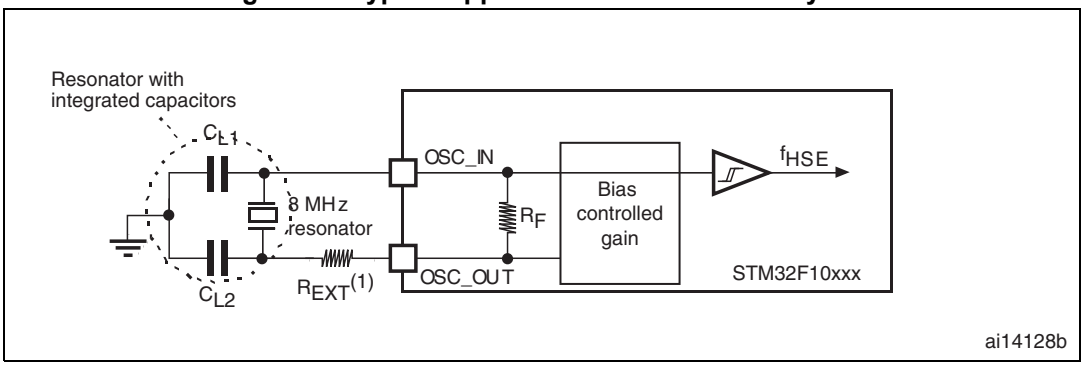
1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA for the ADC and of 0.5 mA for the DAC analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. An 8 MHz crystal is used as the external clock source. The AHB prescaler is used to reduce the frequency when f_{HCLK} < 8 MHz, the PLL is used when f_{HCLK} > 8 MHz.

Table 21. HSE 4-24 MHz oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	24	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
C_{L1} C_{L2}(3)	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(4)	R_S = 30 Ω	-	30	-	pF
i_2	HSE driving current	V_{DD} = 3.3 V V_{IN} = V_{SS} with 30 pF load	-	-	1	mA
g_m	Oscillator transconductance	Startup	25	-	-	mA/V
$t_{SU(HSE)}$ (5)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results.
3. It is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.
4. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
5. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Figure 20. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

5.3.16 Communications interfaces

I²C interface characteristics

Unless otherwise specified, the parameters given in *Table 39* are derived from tests performed under the ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage conditions summarized in *Table 8*.

The STM32F100xx value line I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I²C characteristics are described in *Table 39*. Refer also to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 39. I²C characteristics

Symbol	Parameter	Standard mode I²C(1)		Fast mode I²C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	-	0	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. Guaranteed by design.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I²C frequencies. It must be at least 4 MHz to achieve fast mode I²C frequencies. It must be a multiple of 10 MHz to reach the 400 kHz maximum I2C fast mode clock.
3. The maximum Data hold time has only to be met if the interface does not stretch the low period of SCL signal.

Table 42. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
I_{VREF}	Current on the V_{REF} input pin	-	-	160(1)	220(1)	µA
f_{ADC}	ADC clock frequency	-	0.6	-	12	MHz
f_S(2)	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 12 MHz	-	-	705	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}(3)	Conversion voltage range	-	0 (V_{SSA} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* and *Table 43* for details	-	-	50	kΩ
R_{ADC}(2)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 12 MHz	6.9			µs
		-	83			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 12 MHz	-	-	0.25	µs
		-	-	-	3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 12 MHz	-	-	0.166	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 12 MHz	0.125	-	20.0	µs
			1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	0	0	1	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 12 MHz	1.17	-	21	µs
		-	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Based on characterization results, not tested in production.
2. Guaranteed by design.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Table 4: Low & medium-density STM32F100xx pin definitions* and *Figure 6* for further details.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 42*.

Equation 1: R_{AIN} max formula:

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above formula (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Figure 32. ADC accuracy characteristics

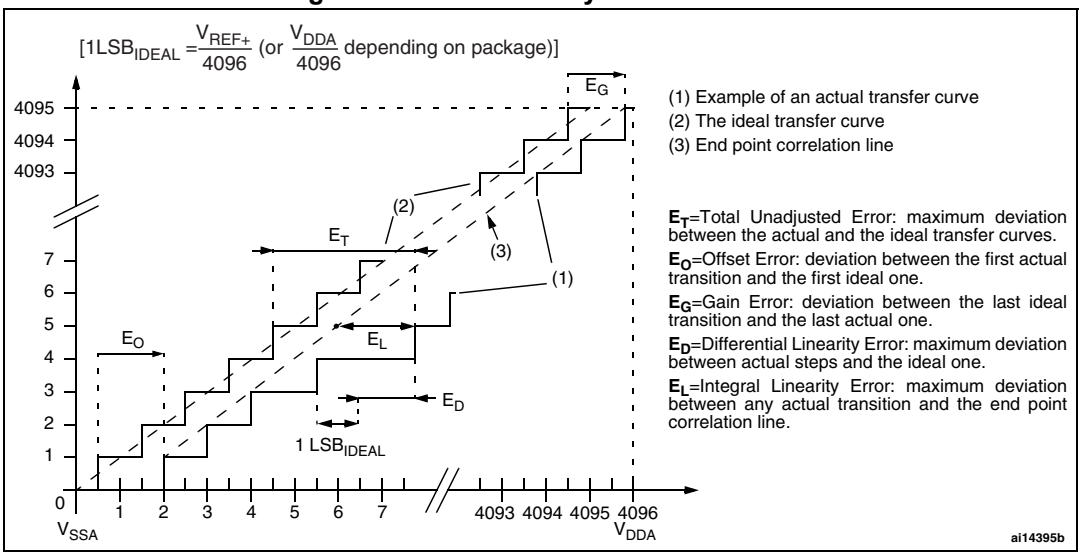
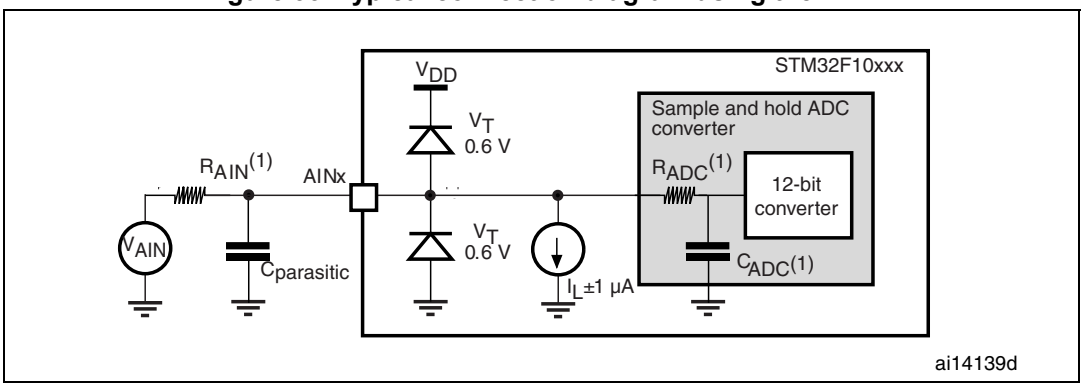


Figure 33. Typical connection diagram using the ADC



1. Refer to *Table 42* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

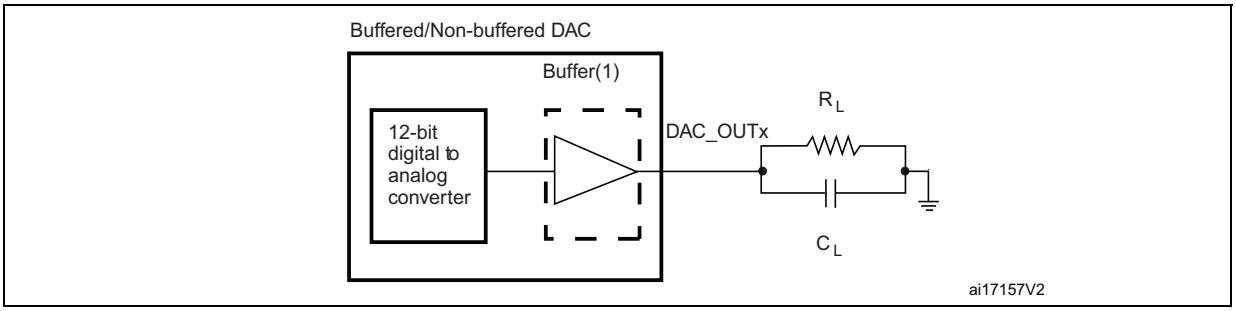
Power supply decoupling should be performed as shown in *Figure 34* or *Figure 35*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Table 46. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max(1)	Unit	Comments
Offset(1)	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{REF+}/2)	-	-	±10	mV	Given for the DAC in 12-bit configuration
		-	-	±3	LSB	Given for the DAC in 10-bit at V_{REF+} = 3.6 V
		-	-	±12	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V
Gain error(1)	Gain error	-	-	±0.5	%	Given for the DAC in 12bit configuration
$t_{SETTLING}$(1)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	-	3	4	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
Update rate(1)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
t_{WAKEUP}(1)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+ (1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement	-	–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. Guaranteed by characterization results.
2. Guaranteed by design.

Figure 36. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Table 48. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 55. Document revision history (continued)

Date	Revision	Changes
08-Jun-2012	7	Updated *Table 6: Current characteristics on page 34* Updated *Table 39: I2C characteristics on page 64* Corrected note “non-robust “ in *Section 5.3.17: 12-bit ADC characteristics on page 68* Updated *Section 5.3.13: I/O port characteristics on page 57* Updated *Section 2.2.20: GPIOs (general-purpose inputs/outputs) on page 20* Updated *Table 4: Low & medium-density STM32F100xx pin definitions on page 24* Updated *Section 5.3.1: General operating conditions on page 34* Updated *Table 14: Maximum current consumption in Sleep mode, code running from Flash or RAM on page 39*
08-Jun-2015	8	Updated *Table 18: Peripheral current consumption*, *Table 31: ESD absolute maximum ratings*, *Table 48: LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data*, *Table 49: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data*, *Table 50: TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package mechanical data*, *Table 51: TFBGA64 recommended PCB design rules (0.5 mm pitch BGA)* and *Table 52: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data*. Updated *Figure 37: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline*, *Figure 38: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint*, *Figure 40: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline*, *Figure 41: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint*, *Figure 43: TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch thin profile fine pitch ball grid array package outline*, *Figure 44: TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array, recommended footprint*, *Figure 46: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline* and *Figure 47: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint*. Added *Figure 39: LQFP100 marking example (package top view)*, *Figure 42: LQFP64 marking example (package top view) Figure 45: TFBGA64 marking example (package top view)* and *Figure 48: LQFP48 marking example (package top view)*.
21-Nov-2016	9	Updated: – *Figure 7: Memory map* – *Figure 18: High-speed external clock source AC timing diagram* – *Figure 19: Low-speed external clock source AC timing diagram* – *Table 19: High-speed external user clock characteristics* – *Table 20: Low-speed external user clock characteristics* – *Table 42: ADC characteristics*