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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f100cbt7btr

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Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard TIM timers which have the same architecture. The advanced control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIM2, TIM3, TIM4, TIM15, TIM16 & TIM17)

There are six synchronizable general-purpose timers embedded in the STM32F100xx devices (see [Table 3](#) for differences). Each general-purpose timers can be used to generate PWM outputs, or as simple time base.

TIM2, TIM3, TIM4

STM32F100xx devices feature three synchronizable 4-channels general-purpose timers. These timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2, TIM3, TIM4 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2, TIM3, TIM4 all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

TIM15, TIM16 and TIM17

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate with TIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16, and TIM17 have a complementary output with dead-time generation and independent DMA request generation

Their counters can be frozen in debug mode.

Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.2.16 I²C bus

The I²C bus interface can operate in multimaster and slave modes. It can support standard and fast modes.

It supports dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

The interface can be served by DMA and it supports SM Bus 2.0/PM Bus.

2.2.17 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F100xx value line embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

The available USART interfaces communicate at up to 3 Mbit/s. They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode and have LIN Master/Slave capability.

The USART interfaces can be served by the DMA controller.

2.2.23 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in noninverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- up to 10-bit output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channels' independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the STM32F100xx. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

2.2.24 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between $2\text{ V} < V_{DDA} < 3.6\text{ V}$. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.2.25 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

Figure 4. STM32F100xx value line LQFP64 pinout

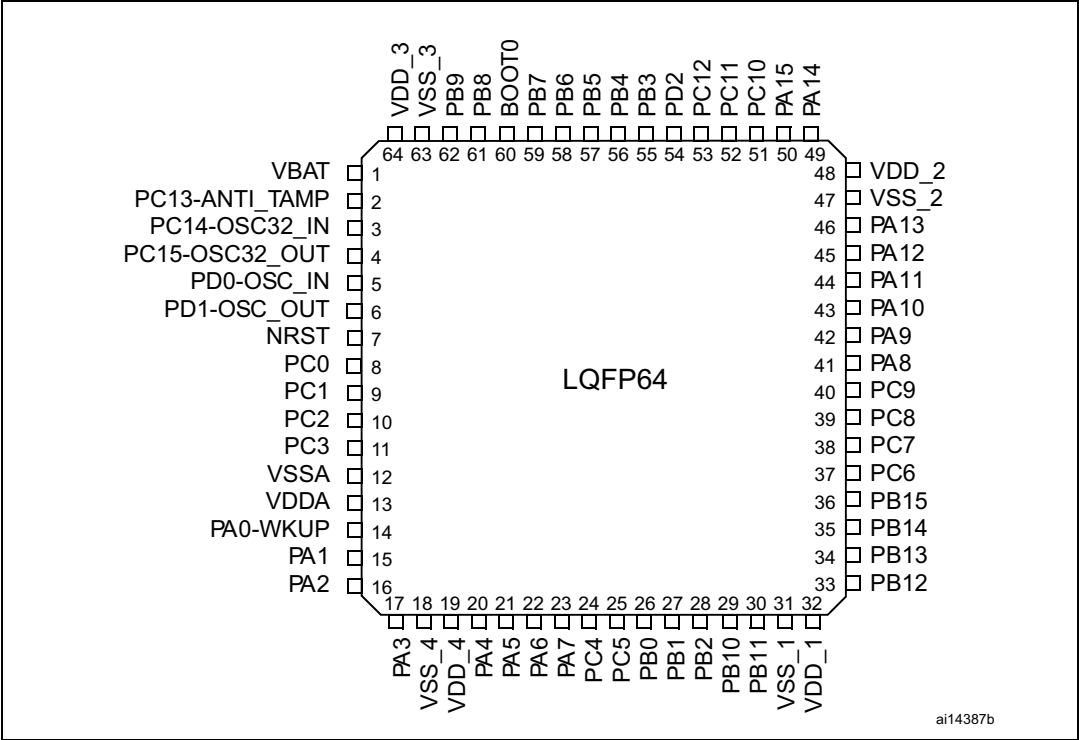
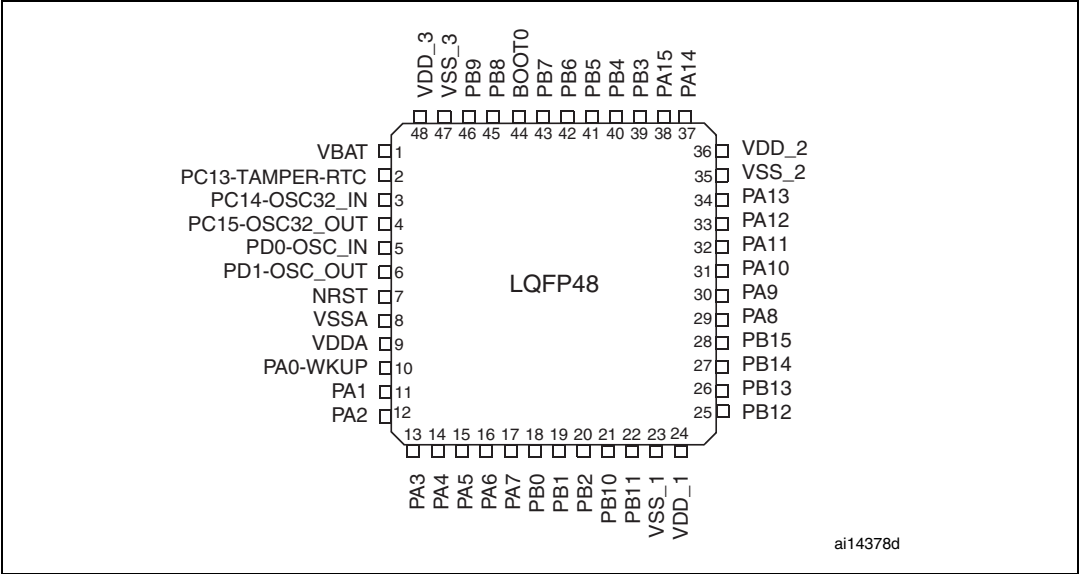


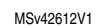
Figure 5. STM32F100xx value line LQFP48 pinout



1. I = input, O = output, S = supply, HiZ= high impedance.
2. FT= 5 V tolerant.
3. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripherals that is included. For example, if a device has only one SPI, two USARTs and two timers, they will be called SPI1, USART1 & USART2 and TIM2 & TIM 3, respectively. Refer to [Table 2 on page 11](#).
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch and since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is restricted: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must *not* be used as a current source (e.g. to drive an LED).
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
7. The pins number 2 and 3 in the VFQFPN36 package, 5 and 6 in the LQFP48 and LQFP64 packages and C1 and C2 in the TFBGA64 package are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.
8. Unlike in the LQFP64 package, there is no PC3 in the TFBGA64 package. The V_{REF+} functionality is provided instead.
9. I2C2 is not present on low-density value line devices.
10. SPI2 is not present on low-density value line devices.
11. TIM4 is not present on low-density value line devices.
12. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.

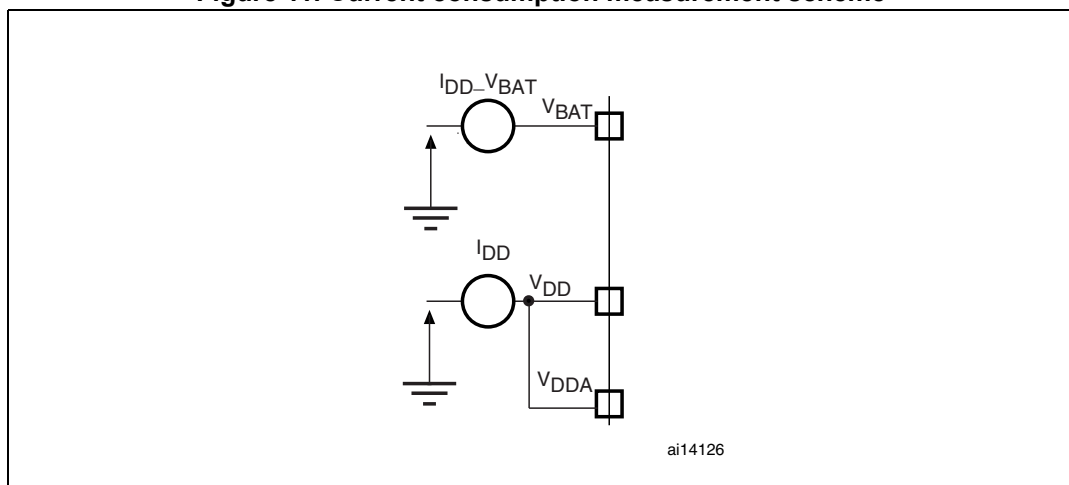
The memory map is shown in *Figure 7*.

Figure 7. Memory map



5.1.7 Current consumption measurement

Figure 11. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 5: Voltage characteristics](#), [Table 6: Current characteristics](#), and [Table 7: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD} - V_{SS}$	External main supply voltage (including V_{DDA} and V_{DD}) ⁽¹⁾	-0.3	4.0	V
V_{IN} ⁽²⁾	Input voltage on five volt tolerant pin	$V_{SS} - 0.3$	$V_{DD} + 4.0$	
	Input voltage on any other pin	$V_{SS} - 0.3$	4.0	
$ \Delta V_{DDx} $	Variations between different V_{DD} power pins	-	50	mV
$ V_{SSx} - V_{SS} $	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see Section 5.3.11: Absolute maximum ratings (electrical sensitivity)		-

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to [Table 6: Current characteristics](#) for the maximum allowed injected current values.

Table 6. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source) ⁽¹⁾	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink) ⁽¹⁾	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	-25	
$I_{INJ(PIN)}^{(2)}$	Injected current on five volt tolerant pins ⁽³⁾	-5 / +0	
	Injected current on any other pin ⁽⁴⁾	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) ⁽⁵⁾	± 25	

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See [Note: on page 70](#).
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to [Table 5: Voltage characteristics](#) for the maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to [Table 5: Voltage characteristics](#) for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 7. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	150	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 8. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	24	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	24	
f_{PCLK2}	Internal APB2 clock frequency	-	0	24	
V_{DD}	Standard operating voltage	-	2	3.6	V
$V_{DDA}^{(1)}$	Analog operating voltage (ADC not used)	Must be the same potential as V_{DD}	2	3.6	V
	Analog operating voltage (ADC used)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.8	3.6	V

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

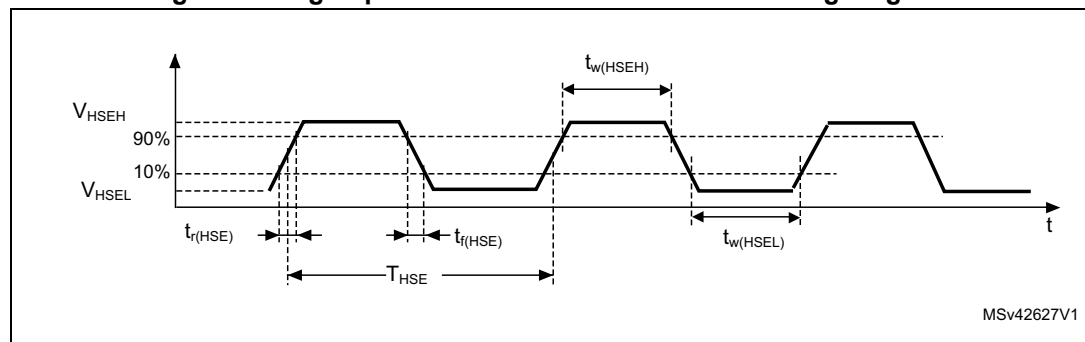
The characteristics given in [Table 19](#) result from tests performed using an high-speed external clock source, and under the ambient temperature and supply voltage conditions summarized in [Table 8](#).

Table 19. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency ⁽¹⁾	-	1	8	24	MHz
V_{HSEH}	OSC_IN input pin high level voltage ⁽¹⁾		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage ⁽¹⁾		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time ⁽¹⁾		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time ⁽¹⁾		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance ⁽¹⁾	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle ⁽¹⁾	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	± 1	μA

1. Guaranteed by design.

Figure 18. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

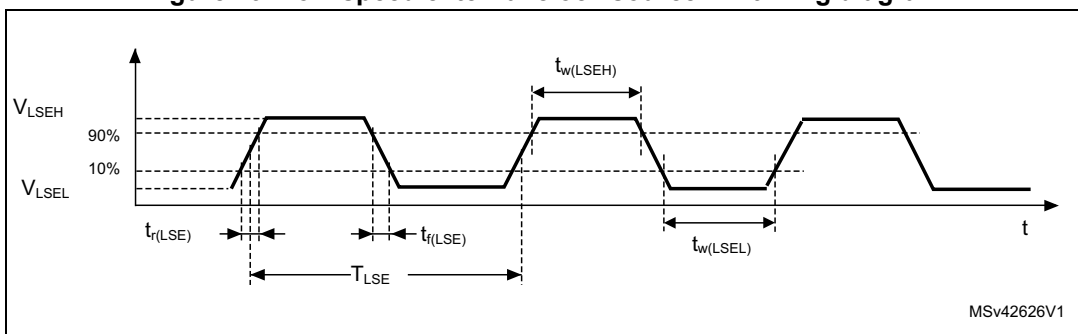
The characteristics given in [Table 20](#) result from tests performed using an low-speed external clock source, and under the ambient temperature and supply voltage conditions summarized in [Table 8](#).

Table 20. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency ⁽¹⁾	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage ⁽¹⁾		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage ⁽¹⁾		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time ⁽¹⁾		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time ⁽¹⁾		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance ⁽¹⁾		-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle ⁽¹⁾		30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	± 1	μA

1. Guaranteed by design.

Figure 19. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 21](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

5.3.9 Memory characteristics

Flash memory

The characteristics are given at $T_A = -40$ to $+105$ °C unless otherwise specified.

Table 27. Flash memory characteristics

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ	Max ⁽¹⁾	Unit
t_{prog}	16-bit programming time	$T_A = -40$ to $+105$ °C	40	52.5	70	µs
t_{ERASE}	Page (1 KB) erase time	$T_A = -40$ to $+105$ °C	20	-	40	ms
t_{ME}	Mass erase time	$T_A = -40$ to $+105$ °C	20	-	40	ms
I_{DD}	Supply current	Read mode $f_{\text{HCLK}} = 24$ MHz, $V_{\text{DD}} = 3.3$ V	-	-	20	mA
		Write / Erase modes $f_{\text{HCLK}} = 24$ MHz, $V_{\text{DD}} = 3.3$ V	-	-	5	mA
		Power-down mode / Halt, $V_{\text{DD}} = 3.0$ to 3.6 V	-	-	50	µA
V_{prog}	Programming voltage	-	2	-	3.6	V

1. Guaranteed by design.

Table 28. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value			Unit
			Min ⁽¹⁾	Typ	Max	
N_{END}	Endurance	$T_A = -40$ to $+85$ °C (6 suffix versions) $T_A = -40$ to $+105$ °C (7 suffix versions)	10	-	-	kcycles
t_{RET}	Data retention	1 kcycle ⁽²⁾ at $T_A = 85$ °C	30	-	-	Years
		1 kcycle ⁽²⁾ at $T_A = 105$ °C	10	-	-	
		10 kcycles ⁽²⁾ at $T_A = 55$ °C	20	-	-	

1. Based on characterization not tested in production.

2. Cycling performed over the whole temperature range.

Figure 24. 5 V tolerant I/O input characteristics - CMOS port

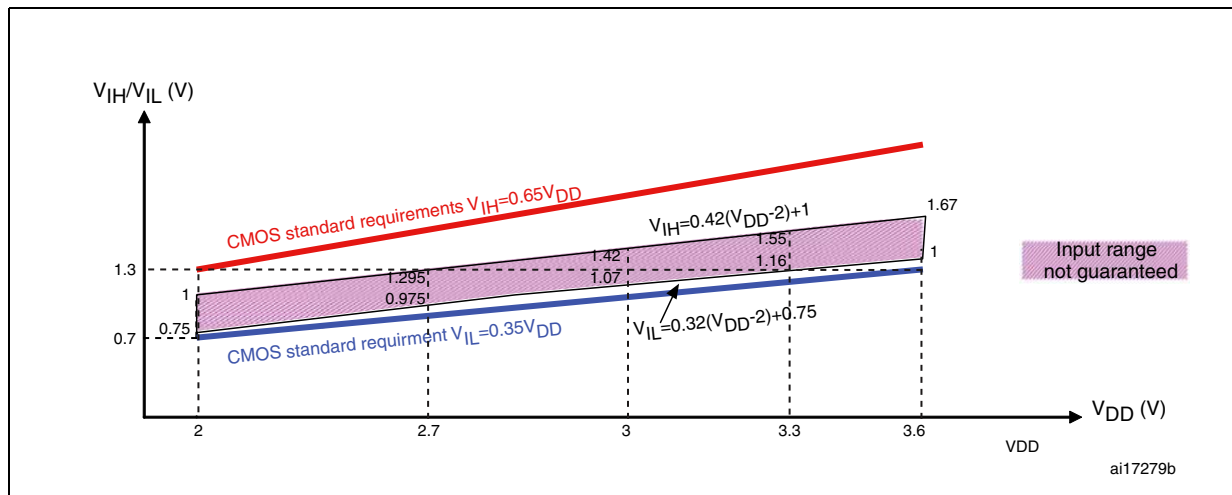
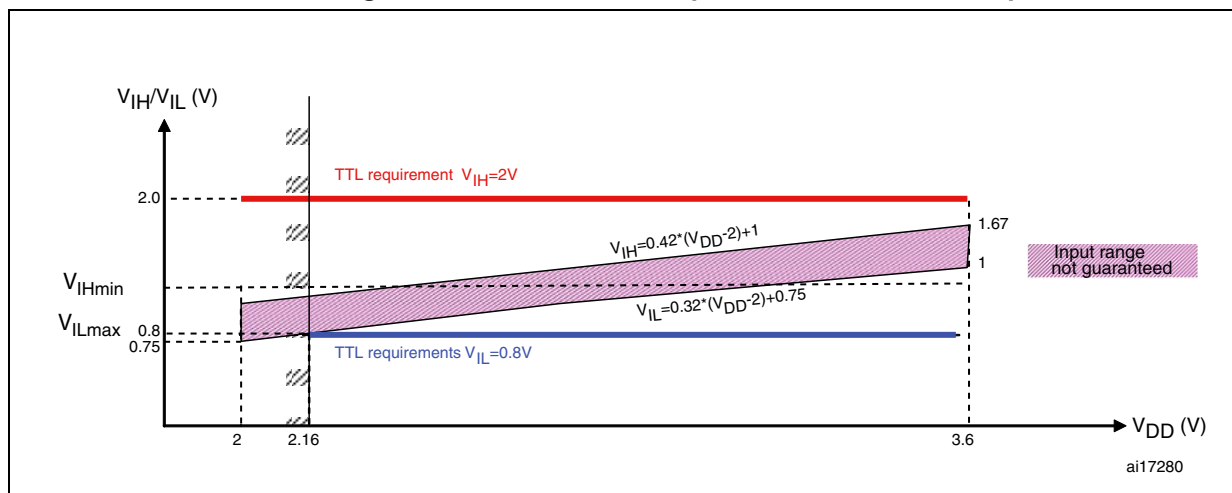


Figure 25. 5 V tolerant I/O input characteristics - TTL port



Output driving current

The GPIOs (general-purpose inputs/outputs) can sink or source up to ± 8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 5.2](#):

- The sum of the currents sourced by all the I/Os on V_{DD} , plus the maximum Run consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating I_{VDD} (see [Table 6](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see [Table 6](#)).

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 26](#) and [Table 36](#), respectively.

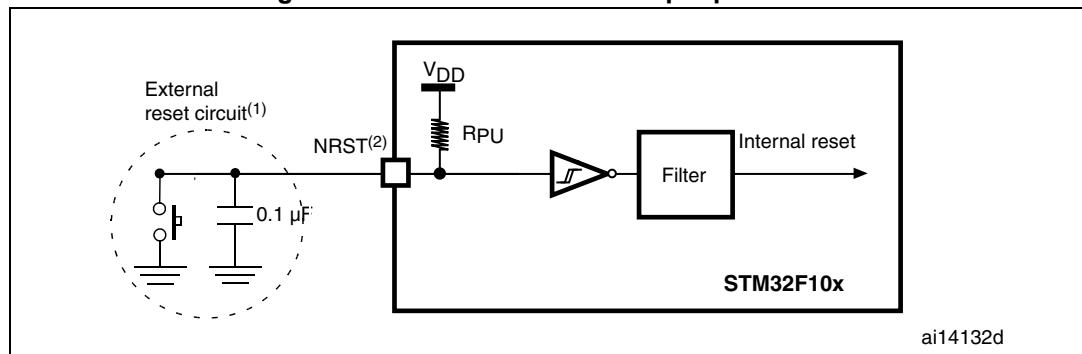
Unless otherwise specified, the parameters given in [Table 36](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 8](#).

Table 36. I/O AC characteristics⁽¹⁾

MODEx [1:0] bit value ⁽¹⁾	Symbol	Parameter	Conditions	Max	Unit
10	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽²⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	2 ⁽³⁾	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	125 ⁽³⁾	ns
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time		125 ⁽³⁾	
01	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽²⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	10 ⁽³⁾	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	25 ⁽³⁾	ns
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time		25 ⁽³⁾	
11	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽²⁾	$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 3.6 \text{ V}$	24	MHz
	$t_{f(\text{IO})\text{out}}$	Output high to low level fall time	$C_L = 30 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	5 ⁽³⁾	ns
			$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	8 ⁽³⁾	
			$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 2.7 \text{ V}$	12 ⁽³⁾	
	$t_{r(\text{IO})\text{out}}$	Output low to high level rise time	$C_L = 30 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	5 ⁽³⁾	
			$C_L = 50 \text{ pF}$, $V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	8 ⁽³⁾	
			$C_L = 50 \text{ pF}$, $V_{DD} = 2 \text{ V to } 2.7 \text{ V}$	12 ⁽³⁾	
-	$t_{\text{EXTI}pw}$	Pulse width of external signals detected by the EXTI controller	-	10 ⁽³⁾	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in [Figure 26](#).
3. Guaranteed by design.

Figure 27. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in [Table 37](#). Otherwise the reset will not be taken into account by the device.

5.3.15 TIMx characteristics

The parameters given in [Table 38](#) are guaranteed by design.

Refer to [Section 5.3.12: I/O current injection characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 38. TIMx characteristics

Symbol	Parameter	Conditions ⁽¹⁾	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 24 \text{ MHz}$	41.7	-	ns
f_{EXT}	Timer external clock frequency on CHx ⁽²⁾	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK} = 24 \text{ MHz}$	0	12	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock period when the internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 24 \text{ MHz}$	-	2730	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536×65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 24 \text{ MHz}$	-	178	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3, TIM4, TIM15, TIM16 and TIM17 timers.
2. CHx is used as a general term to refer to CH1 to CH4 for TIM1, TIM2, TIM3 and TIM4, to the CH1 to CH2 for TIM15, and to CH1 for TIM16 and TIM17.

5.3.19 Temperature sensor characteristics

Table 47. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	V_{SENSE} linearity with temperature	-	± 1	± 2	$^{\circ}\text{C}$
Avg_Slope ⁽¹⁾	Average slope	4.0	4.3	4.6	mV/ $^{\circ}\text{C}$
$V_{25}^{(1)}$	Voltage at 25 $^{\circ}\text{C}$	1.32	1.41	1.50	V
$t_{START}^{(2)}$	Startup time	4	-	10	μs
$T_{S_temp}^{(3)(2)}$	ADC sampling time when reading the temperature	-	-	17.1	μs

1. Guaranteed by characterization results.

2. Guaranteed by design.

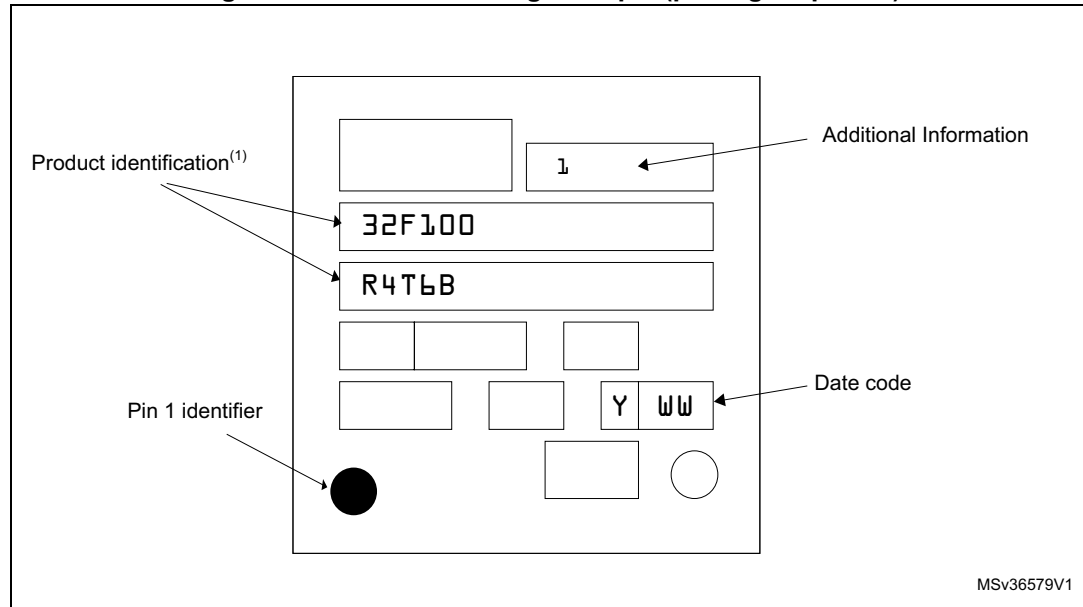
3. Shortest sampling time can be determined in the application by multiple iterations.

Device marking for LQFP64

The following figure gives an example of topside marking and pin 1 position identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 42. LQFP64 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

6.5.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in [Table 54: Ordering information scheme](#).

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F10xxx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example: high-performance application

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax} = 82\text{ }^{\circ}\text{C}$ (measured according to JESD51-2),
 $I_{DDmax} = 50\text{ mA}$, $V_{DD} = 3.5\text{ V}$, maximum 20 I/Os used at the same time in output at low level with $I_{OL} = 8\text{ mA}$, $V_{OL} = 0.4\text{ V}$ and maximum 8 I/Os used at the same time in output mode at low level with $I_{OL} = 20\text{ mA}$, $V_{OL} = 1.3\text{ V}$

$$P_{INTmax} = 50\text{ mA} \times 3.5\text{ V} = 175\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} + 8 \times 20\text{ mA} \times 1.3\text{ V} = 272\text{ mW}$$

$$\text{This gives: } P_{INTmax} = 175\text{ mW and } P_{IOmax} = 272\text{ mW}$$

$$P_{Dmax} = 175 + 272 = 447\text{ mW}$$

$$\text{Thus: } P_{Dmax} = 447\text{ mW}$$

Using the values obtained in [Table 53](#) T_{Jmax} is calculated as follows:

– For LQFP64, $45\text{ }^{\circ}\text{C/W}$

$$T_{Jmax} = 82\text{ }^{\circ}\text{C} + (45\text{ }^{\circ}\text{C/W} \times 447\text{ mW}) = 82\text{ }^{\circ}\text{C} + 20.1\text{ }^{\circ}\text{C} = 102.1\text{ }^{\circ}\text{C}$$

This is within the range of the suffix 6 version parts ($-40 < T_J < 105\text{ }^{\circ}\text{C}$).

In this case, parts must be ordered at least with the temperature range suffix 6 (see [Table 54: Ordering information scheme](#)).

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax} = 115\text{ }^{\circ}\text{C}$ (measured according to JESD51-2),
 $I_{DDmax} = 20\text{ mA}$, $V_{DD} = 3.5\text{ V}$, maximum 20 I/Os used at the same time in output at low level with $I_{OL} = 8\text{ mA}$, $V_{OL} = 0.4\text{ V}$

$$P_{INTmax} = 20\text{ mA} \times 3.5\text{ V} = 70\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} = 64\text{ mW}$$

$$\text{This gives: } P_{INTmax} = 70\text{ mW and } P_{IOmax} = 64\text{ mW:}$$

$$P_{Dmax} = 70 + 64 = 134\text{ mW}$$

$$\text{Thus: } P_{Dmax} = 134\text{ mW}$$

Using the values obtained in [Table 53](#) T_{Jmax} is calculated as follows:

– For LQFP100, 46 °C/W

$$T_{Jmax} = 115\text{ °C} + (46\text{ °C/W} \times 134\text{ mW}) = 115\text{ °C} + 6.2\text{ °C} = 121.2\text{ °C}$$

This is within the range of the suffix 7 version parts ($-40 < T_J < 125\text{ °C}$).

In this case, parts must be ordered at least with the temperature range suffix 7 (see [Table 54: Ordering information scheme](#)).

Figure 49. LQFP100 P_D max vs. T_A

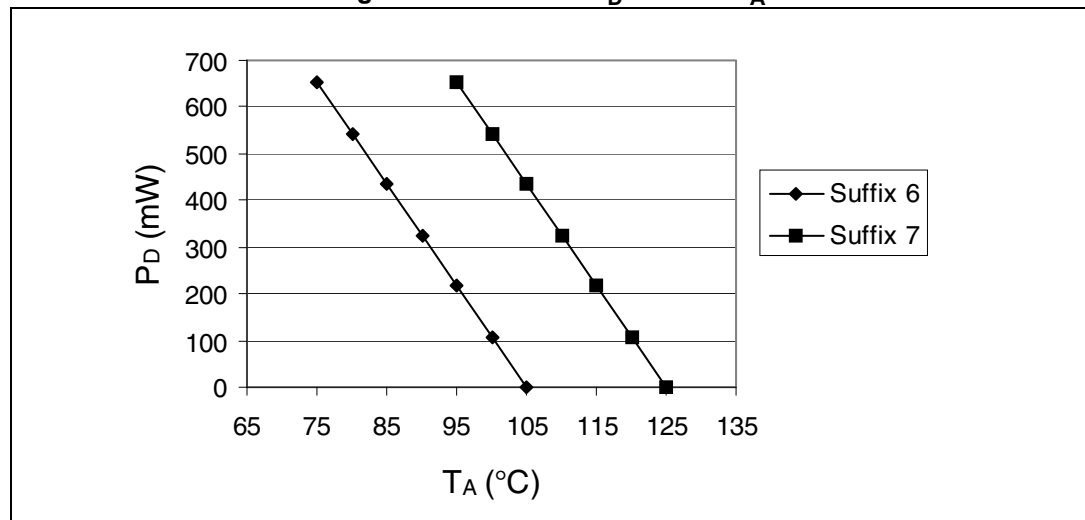


Table 55. Document revision history (continued)

Date	Revision	Changes
08-Jun-2012	7	<p>Updated Table 6: Current characteristics on page 34</p> <p>Updated Table 39: I2C characteristics on page 64</p> <p>Corrected note “non-robust “ in Section 5.3.17: 12-bit ADC characteristics on page 68</p> <p>Updated Section 5.3.13: I/O port characteristics on page 57</p> <p>Updated Section 2.2.20: GPIOs (general-purpose inputs/outputs) on page 20</p> <p>Updated Table 4: Low & medium-density STM32F100xx pin definitions on page 24</p> <p>Updated Section 5.3.1: General operating conditions on page 34</p> <p>Updated Table 14: Maximum current consumption in Sleep mode, code running from Flash or RAM on page 39</p>
08-Jun-2015	8	<p>Updated Table 18: Peripheral current consumption, Table 31: ESD absolute maximum ratings, Table 48: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data, Table 49: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data, Table 50: TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package mechanical data, Table 51: TFBGA64 recommended PCB design rules (0.5 mm pitch BGA) and Table 52: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data.</p> <p>Updated Figure 37: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline, Figure 38: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint, Figure 40: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline, Figure 41: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint, Figure 43: TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch thin profile fine pitch ball grid array package outline, Figure 44: TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array, recommended footprint, Figure 46: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline and Figure 47: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint.</p> <p>Added Figure 39: LQFP100 marking example (package top view), Figure 42: LQFP64 marking example (package top view) Figure 45: TFBGA64 marking example (package top view) and Figure 48: LQFP48 marking example (package top view).</p>
21-Nov-2016	9	<p>Updated:</p> <ul style="list-style-type: none"> – Figure 7: Memory map – Figure 18: High-speed external clock source AC timing diagram – Figure 19: Low-speed external clock source AC timing diagram – Table 19: High-speed external user clock characteristics – Table 20: Low-speed external user clock characteristics – Table 42: ADC characteristics