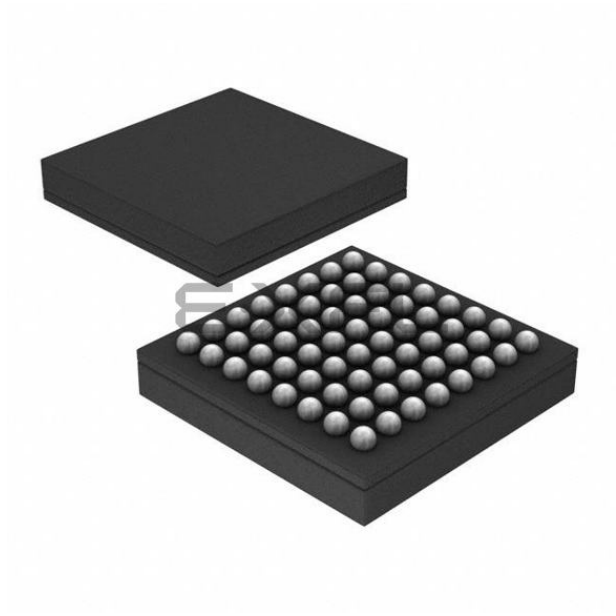

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 24MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT |
| Number of I/O | 51 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 16x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-TFBGA |
| Supplier Device Package | 64-TFBGA (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f100r8h7b |

## 2.1 Device overview

The description below gives an overview of the complete range of peripherals proposed in this family.

*Figure 1* shows the general block diagram of the device family.

**Table 2. STM32F100xx features and peripheral counts**

| Peripheral | | STM32F100Cx | | | | STM32F100Rx | | | | STM32F100Vx | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Flash - Kbytes** | | 16 | 32 | 64 | 128 | 16 | 32 | 64 | 128 | 64 | 128 |
| **SRAM - Kbytes** | | 4 | 4 | 8 | 8 | 4 | 4 | 8 | 8 | 8 | 8 |
| **Timers** | Advanced-control | 1 | | 1 | | 1 | | 1 | | 1 | |
| | **General-purpose** | 5(1) | | 6 | | 5(1) | | 6 | | 6 | |
| **Communication interfaces** | **SPI** | 1(2) | | 2 | | 1(2) | | 2 | | 2 | |
| | **$I^2C$** | 1(3) | | 2 | | 1(3) | | 2 | | 2 | |
| | **USART** | 2(4) | | 3 | | 2(4) | | 3 | | 3 | |
| | **CEC** | 1 | | | | | | | | | |
| **12-bit synchronized ADC number of channels** | | 1<br>10 channels | | | | 1<br>16 channels | | | | 1<br>16 channels | |
| **GPIOs** | | 37 | | | | 51 | | | | 80 | |
| **12-bit DAC Number of channels** | | 2<br>2 | | | | | | | | | |
| **CPU frequency** | | 24 MHz | | | | | | | | | |
| **Operating voltage** | | 2.0 to 3.6 V | | | | | | | | | |
| **Operating temperatures** | | Ambient operating temperature: –40 to +85 °C /–40 to +105 °C (see *Table 8*)<br>Junction temperature: –40 to +125 °C (see *Table 8*) | | | | | | | | | |
| **Packages** | | LQFP48 | | | | LQFP64, TFBGA64 | | | | LQFP100 | |

1. TIM4 not present.
2. SPI2 is not present.
3. I2C2 is not present.
4. USART3 is not present.

### 2.2.23 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in noninverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- up to 10-bit output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channels' independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference $V_{REF+}$

Eight DAC trigger inputs are used in the STM32F100xx. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

### 2.2.24 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < $V_{DDA}$ < 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

### 2.2.25 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

**Figure 4. STM32F100xx value line LQFP64 pinout**

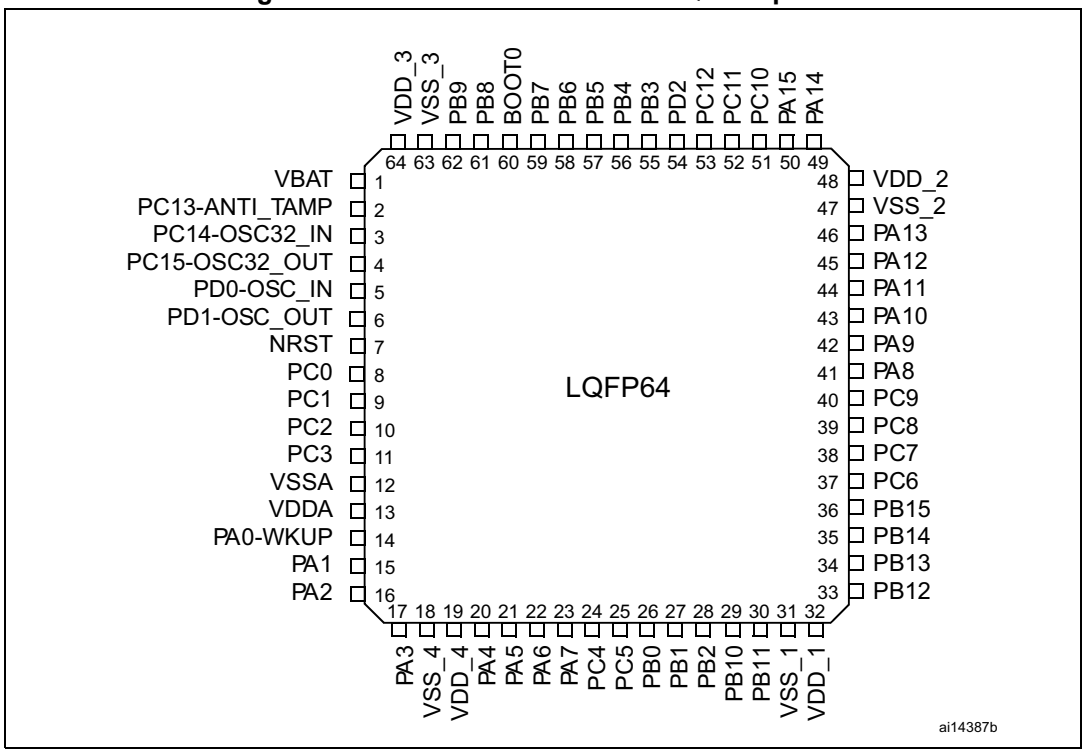



**Figure 5. STM32F100xx value line LQFP48 pinout**

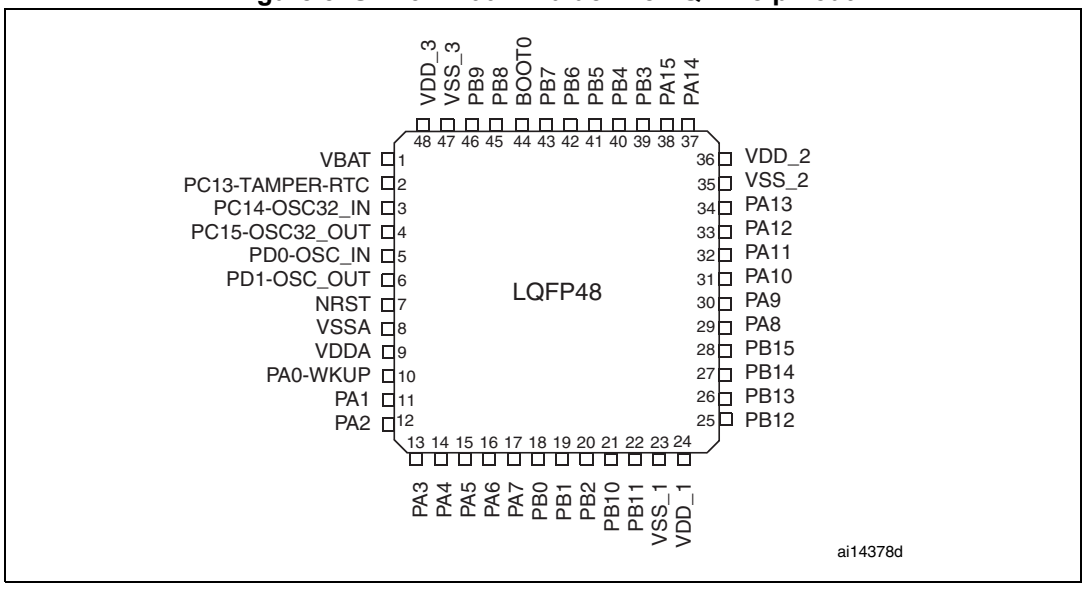


**Table 4. Low & medium-density STM32F100xx pin definitions (continued)**

| Pins | | | | Pin name | Type(1) | I / O level(2) | Main function(3) (after reset) | Alternate functions(3)(4) | |
|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | LQFP64 | TFBGA64 | LQFP48 | | | | | Default | Remap |
| 33 | 24 | H5 | - | PC4 | I/O | - | PC4 | ADC1_IN14 | - |
| 34 | 25 | H6 | - | PC5 | I/O | - | PC5 | ADC1_IN15 | - |
| 35 | 26 | F5 | 18 | PB0 | I/O | - | PB0 | ADC1_IN8/TIM3_CH3(12) | TIM1_CH2N |
| 36 | 27 | G5 | 19 | PB1 | I/O | - | PB1 | ADC1_IN9/TIM3_CH4(12) | TIM1_CH3N |
| 37 | 28 | G6 | 20 | PB2 | I/O | FT | PB2/BOOT1 | - | - |
| 38 | - | - | - | PE7 | I/O | FT | PE7 | - | TIM1_ETR |
| 39 | - | - | - | PE8 | I/O | FT | PE8 | - | TIM1_CH1N |
| 40 | - | - | - | PE9 | I/O | FT | PE9 | - | TIM1_CH1 |
| 41 | - | - | - | PE10 | I/O | FT | PE10 | - | TIM1_CH2N |
| 42 | - | - | - | PE11 | I/O | FT | PE11 | - | TIM1_CH2 |
| 43 | - | - | - | PE12 | I/O | FT | PE12 | - | TIM1_CH3N |
| 44 | - | - | - | PE13 | I/O | FT | PE13 | - | TIM1_CH3 |
| 45 | - | - | - | PE14 | I/O | FT | PE14 | - | TIM1_CH4 |
| 46 | - | - | - | PE15 | I/O | FT | PE15 | - | TIM1_BKIN |
| 47 | 29 | G7 | 21 | PB10 | I/O | FT | PB10 | I2C2_SCL(9)/USART3_TX (12) | TIM2_CH3 / HDMI_CEC |
| 48 | 30 | H7 | 22 | PB11 | I/O | FT | PB11 | I2C2_SDA(9)/USART3_RX( 12) | TIM2_CH4 |
| 49 | 31 | D6 | 23 | $V_{SS\_1}$ | S | - | $V_{SS\_1}$ | - | - |
| 50 | 32 | E6 | 24 | $V_{DD\_1}$ | S | - | $V_{DD\_1}$ | - | - |
| 51 | 33 | H8 | 25 | PB12 | I/O | FT | PB12 | SPI2_NSS(10)/ I2C2_SMBA(9)/ TIM1_BKIN(12)/USART3_C K(12) | - |
| 52 | 34 | G8 | 26 | PB13 | I/O | FT | PB13 | SPI2_SCK(10) /TIM1_CH1N(12) USART3_CTS(12) | - |
| 53 | 35 | F8 | 27 | PB14 | I/O | FT | PB14 | SPI2_MISO(10)/ TIM1_CH2N(12) / USART3_RTS(12) | TIM15_CH1 |
| 54 | 36 | F7 | 28 | PB15 | I/O | FT | PB15 | SPI2_MOSI(10) / TIM1_CH3N / TIM15_CH1N(12) | TIM15_CH2 |
| 55 | - | - | - | PD8 | I/O | FT | PD8 | - | USART3_TX |
| 56 | - | - | - | PD9 | I/O | FT | PD9 | - | USART3_RX |

**Table 6. Current characteristics**

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $I_{VDD}$ | Total current into $V_{DD}/V_{DDA}$ power lines (source)(1) | 150 | mA |
| $I_{VSS}$ | Total current out of $V_{SS}$ ground lines (sink)(1) | 150 | |
| $I_{IO}$ | Output current sunk by any I/O and control pin | 25 | |
| | Output current source by any I/Os and control pin | -25 | |
| $I_{INJ(PIN)}$(2) | Injected current on five volt tolerant pins(3) | -5 / +0 | |
| | Injected current on any other pin(4) | ± 5 | |
| $\Sigma I_{INJ(PIN)}$ | Total injected current (sum of all I/O and control pins)(5) | ± 25 | |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See*Note: on page 70*.
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 5: Voltage characteristics* for the maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 5: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

**Table 7. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $T_J$ | Maximum junction temperature | 150 | °C |

# 5.3 Operating conditions

## 5.3.1 General operating conditions

**Table 8. General operating conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{HCLK}$ | Internal AHB clock frequency | - | 0 | 24 | MHz |
| $f_{PCLK1}$ | Internal APB1 clock frequency | - | 0 | 24 | |
| $f_{PCLK2}$ | Internal APB2 clock frequency | - | 0 | 24 | |
| $V_{DD}$ | Standard operating voltage | - | 2 | 3.6 | V |
| $V_{DDA}$(1) | Analog operating voltage (ADC not used) | Must be the same potential as $V_{DD}$ | 2 | 3.6 | V |
| | Analog operating voltage (ADC used) | | 2.4 | 3.6 | |
| $V_{BAT}$ | Backup operating voltage | - | 1.8 | 3.6 | V |

**Figure 12. Maximum current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled**

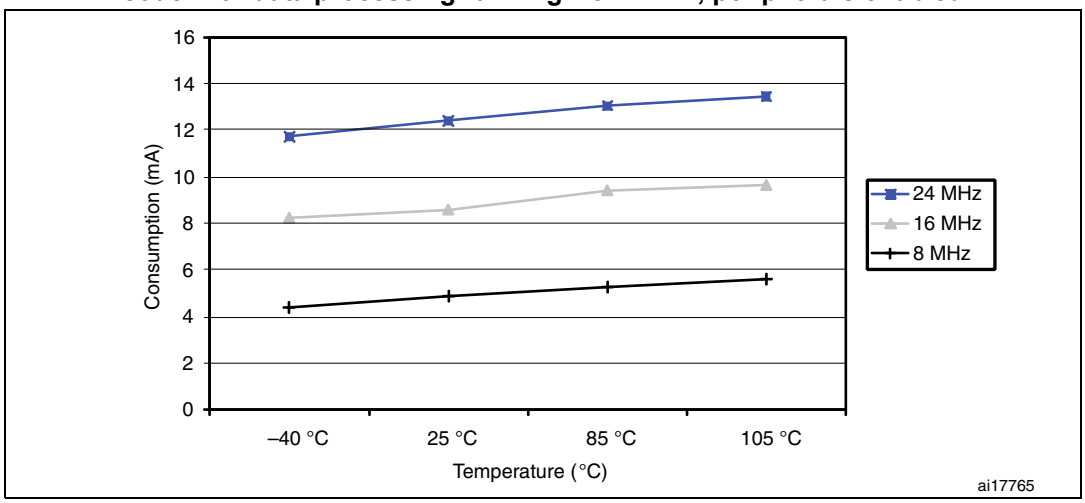



**Figure 13. Maximum current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled**

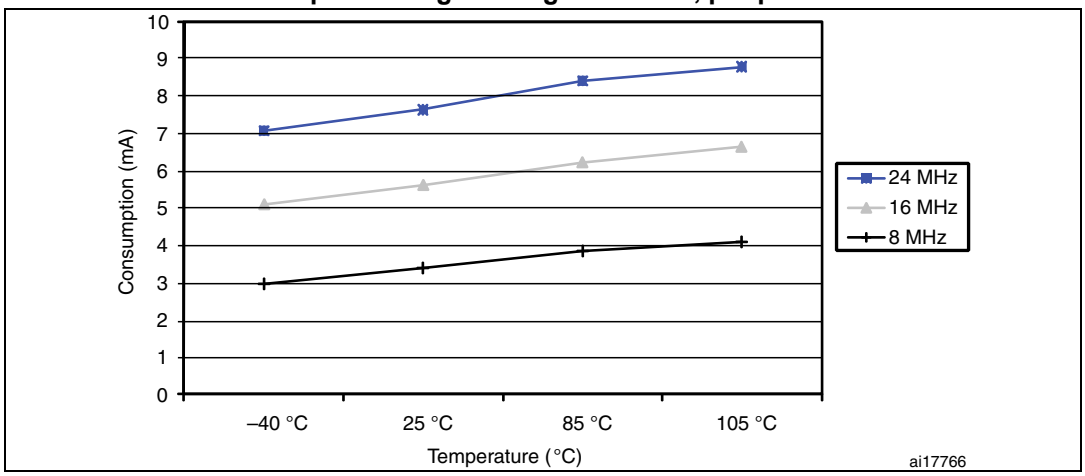
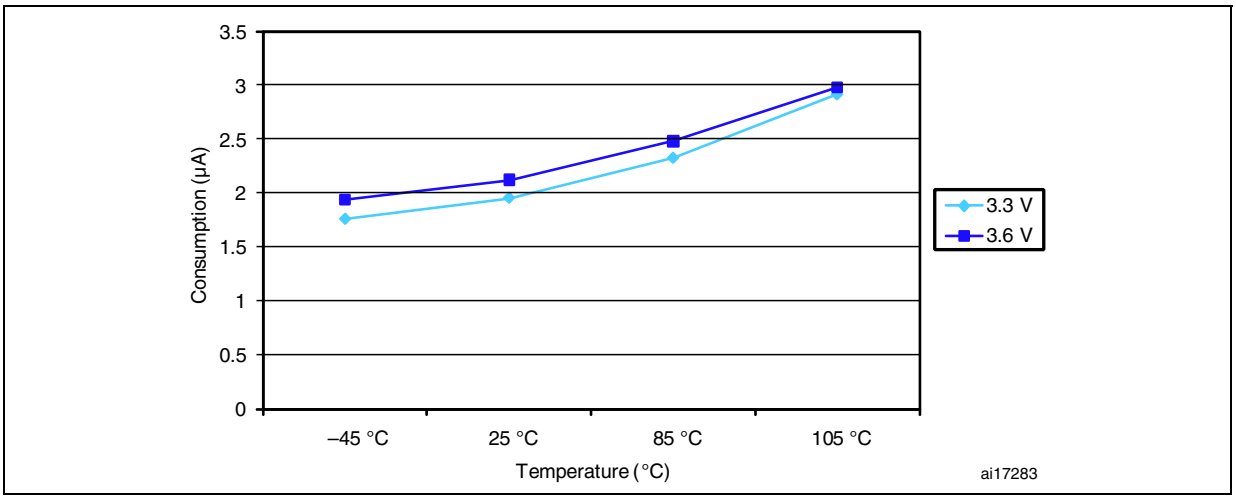



**Table 14. Maximum current consumption in Sleep mode, code running from Flash or RAM**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Max(1) | | Unit |
|---|---|---|---|---|---|---|
| | | | | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in Sleep mode | External clock(2) all peripherals enabled | 24 MHz | 9.6 | 10 | mA |
| | | | 16 MHz | 7.1 | 7.5 | |
| | | | 8 MHz | 4.5 | 4.8 | |
| | | External clock(2), all peripherals disabled | 24 MHz | 3.8 | 4 | |
| | | | 16 MHz | 3.3 | 3.5 | |
| | | | 8 MHz | 2.7 | 3 | |

1. Guaranteed by characterization, tested in production at $V_{DD}$ max and $f_{HCLK}$ max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when $f_{HCLK}$ > 8 MHz.

**Figure 17. Typical current consumption in Standby mode versus temperature at $V_{DD}$ = 3.3 V and 3.6 V**




## Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)
- All peripherals are disabled except if it is explicitly mentioned
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK2} = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$

The parameters given in *Table 16* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 8*.

**Table 16. Typical current consumption in Run mode, code with data processing running from Flash**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typical values(1) | | Unit |
|---|---|---|---|---|---|---|
| | | | | All peripherals enabled(2) | All peripherals disabled | |
| $I_{DD}$ | Supply current in Run mode | Running on high-speed external clock with an 8 MHz crystal(3) | 24 MHz | 12.8 | 9.3 | mA |
| | | | 16 MHz | 9.3 | 6.6 | |
| | | | 8 MHz | 5.1 | 3.9 | |
| | | | 4 MHz | 3.2 | 2.5 | |
| | | | 2 MHz | 2.1 | 1.75 | |
| | | | 1 MHz | 1.55 | 1.4 | |
| | | | 500 kHz | 1.3 | 1.2 | |
| | | | 125 kHz | 1.1 | 1.05 | |
| | | Running on high-speed internal RC (HSI) | 24 MHz | 12.2 | 8.6 | |
| | | | 16 MHz | 8.5 | 6 | |
| | | | 8 MHz | 4.6 | 3.3 | |
| | | | 4 MHz | 2.6 | 1.9 | |
| | | | 2 MHz | 1.5 | 1.15 | |
| | | | 1 MHz | 0.9 | 0.8 | |
| | | | 500 kHz | 0.65 | 0.6 | |
| | | | 125 kHz | 0.45 | 0.43 | |

1. Typical values are measures at $T_A$ = 25 °C, $V_{DD}$ = 3.3 V.
2. Add an additional power consumption of 0.8 mA for the ADC and of 0.5 mA for the DAC analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. An 8 MHz crystal is used as the external clock source. The AHB prescaler is used to reduce the frequency when $f_{HCLK}$ < 8 MHz, the PLL is used when $f_{HCLK}$ > 8 MHz.

**Table 18. Peripheral current consumption(1)**

| Peripheral | | Current consumption (µA/MHz) |
|---|---|---|
| AHB (up to 24MHz) | DMA1 | 22.92 |
| | CRC | 2,08 |
| | BusMatrix(2) | 4,17 |
| APB1 (up to 24MHz) | APB1-Bridge | 2,92 |
| | TIM2 | 18,75 |
| | TIM3 | 17,92 |
| | TIM4 | 18,33 |
| | TIM6 | 5,00 |
| | TIM7 | 5,42 |
| | SPI2/I2S2 | 4,17 |
| | USART2 | 12,08 |
| | USART3 | 12,92 |
| | I2C1 | 10,83 |
| | I2C2 | 10,83 |
| | CEC | 5,83 |
| | DAC(3) | 8,33 |
| | WWDG | 2,50 |
| | PWR | 2,50 |
| | BKP | 3,33 |
| | IWDG | 7,50 |
| APB2 (up to 24MHz) | APB2-Bridge | 3.75 |
| | GPIOA | 6,67 |
| | GPIOB | 6,25 |
| | GPIOC | 7,08 |
| | GPIOD | 6,67 |
| | GPIOE | 6,25 |
| | SPI1 | 4,17 |
| | USART1 | 11,67 |
| | TIM1 | 22,92 |
| | TIM15 | 14,58 |
| | TIM16 | 11,67 |
| | TIM17 | 10.83 |
| | ADC1(4) | 15.83 |

1. $f_{HCLK}$ = 24 MHz, $f_{APB1} = f_{HCLK}$, fAPB2 = $f_{HCLK}$, default prescaler value for each peripheral.
2. The BusMatrix is automatically active when at least one master is ON.
3. When DAC_OUT1 or DAC_OU2 is enabled a current consumption equal to 0,5 mA must be added
4. Specific conditions for ADC: $f_{HCLK}$ = 24 MHz, $f_{APB1} = f_{HCLK}$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/2$. When ADON bit in the ADC_CR2 register is set to 1, a current consumption equal to 0, 1mA must be added.

## 5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

### Functional EMS (Electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 29*. They are based on the EMS levels and classes defined in application note AN1709.

**Table 29. EMS characteristics**

| Symbol | Parameter | Conditions | Level/Class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, $T_A$ = +25 °C, $f_{HCLK}$ = 24 MHz, LQFP100 package, conforms to IEC 61000-4-2 | 2B |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$ = 3.3 V, $T_A$ = +25 °C, $f_{HCLK}$ = 24 MHz, LQFP100 package, conforms to IEC 61000-4-4 | 4A |

### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

Software recommendations

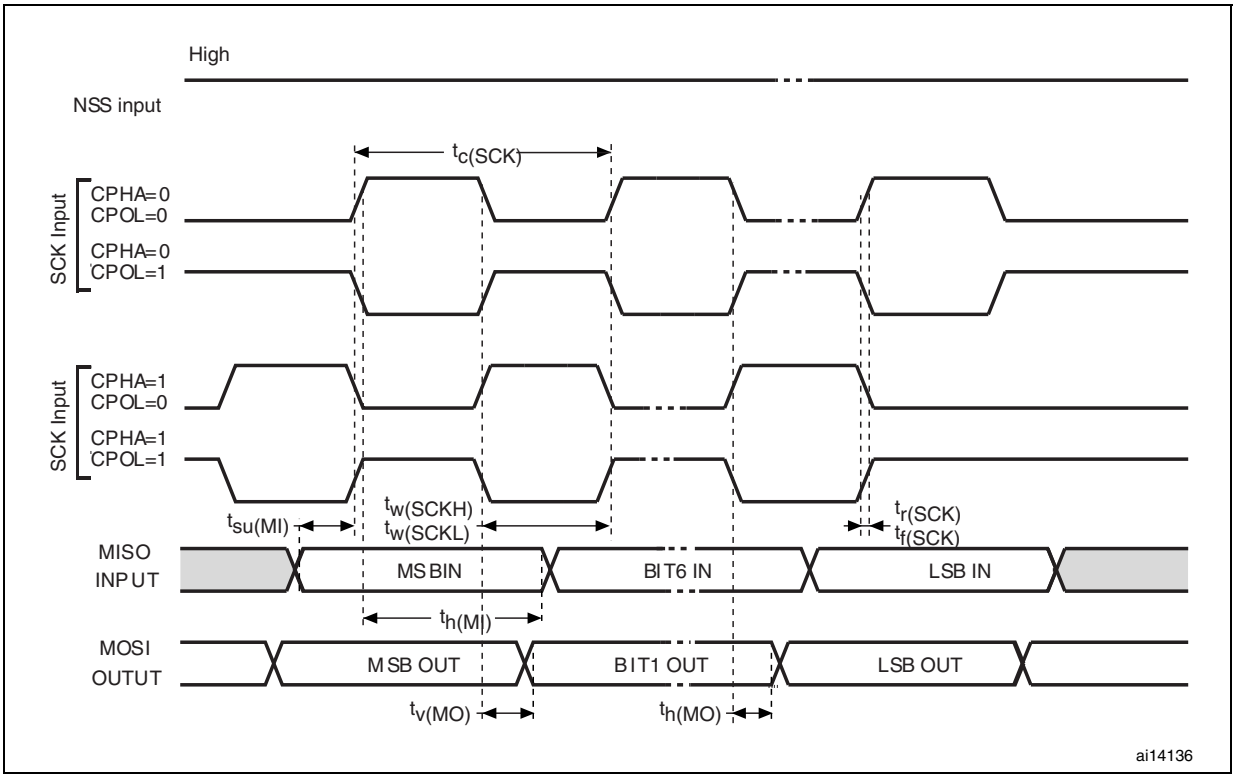
The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

### Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second. To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

**Figure 31. SPI timing diagram - master mode(1)**




1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

### HDMI consumer electronics control (CEC)

Refer to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics.

## 5.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 42* are derived from tests performed under the ambient temperature, $f_{PCLK2}$ frequency and $V_{DDA}$ supply voltage conditions summarized in *Table 8*.

*Note: It is recommended to perform a calibration after each power-up.*

**Table 42. ADC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Power supply | - | 2.4 | - | 3.6 | V |
| $V_{REF+}$ | Positive reference voltage | - | 2.4 | - | $V_{DDA}$ | V |
| $I_{VREF}$ | Current on the $V_{REF}$ input pin | - | - | 160(1) | 220(1) | µA |
| $f_{ADC}$ | ADC clock frequency | - | 0.6 | - | 12 | MHz |
| $f_S$(2) | Sampling rate | - | 0.05 | - | 1 | MHz |
| $f_{TRIG}$(2) | External trigger frequency | $f_{ADC}$ = 12 MHz | - | - | 705 | kHz |
| | | - | - | - | 17 | $1/f_{ADC}$ |
| $V_{AIN}$(3) | Conversion voltage range | - | 0 ($V_{SSA}$ tied to ground) | - | $V_{REF+}$ | V |
| $R_{AIN}$(2) | External input impedance | See *Equation 1* and *Table 43* for details | - | - | 50 | kΩ |
| $R_{ADC}$(2) | Sampling switch resistance | - | - | - | 1 | kΩ |
| $C_{ADC}$(2) | Internal sample and hold capacitor | - | - | - | 8 | pF |
| $t_{CAL}$(2) | Calibration time | $f_{ADC}$ = 12 MHz | 6.9 | | | µs |
| | | - | 83 | | | $1/f_{ADC}$ |
| $t_{lat}$(2) | Injection trigger conversion latency | $f_{ADC}$ = 12 MHz | - | - | 0.25 | µs |
| | | - | - | - | 3(4) | $1/f_{ADC}$ |
| $t_{latr}$(2) | Regular trigger conversion latency | $f_{ADC}$ = 12 MHz | - | - | 0.166 | µs |
| | | - | - | - | 2(4) | $1/f_{ADC}$ |
| $t_S$(2) | Sampling time | $f_{ADC}$ = 12 MHz | 0.125 | - | 20.0 | µs |
| | | | 1.5 | - | 239.5 | $1/f_{ADC}$ |
| $t_{STAB}$(2) | Power-up time | - | 0 | 0 | 1 | µs |
| $t_{CONV}$(2) | Total conversion time (including sampling time) | $f_{ADC}$ = 12 MHz | 1.17 | - | 21 | µs |
| | | - | 14 to 252 ($t_S$ for sampling +12.5 for successive approximation) | | | $1/f_{ADC}$ |

1. Based on characterization results, not tested in production.
2. Guaranteed by design.
3. $V_{REF+}$ can be internally connected to $V_{DDA}$ and $V_{REF-}$ can be internally connected to $V_{SSA}$, depending on the package. Refer to *Table 4: Low & medium-density STM32F100xx pin definitions* and *Figure 6* for further details.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 42*.

**Equation 1: $R_{AIN}$ max formula:**

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

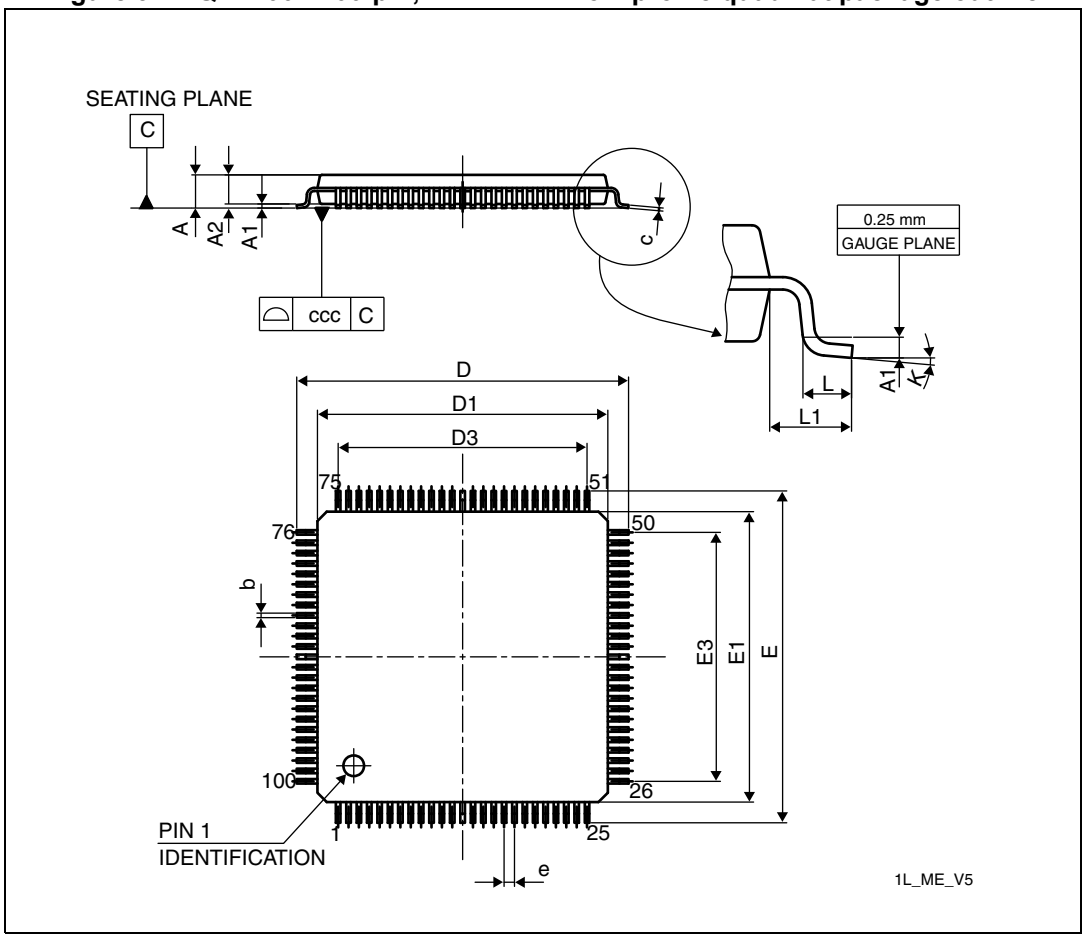
The above formula (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

# 6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

## 6.1 LQFP100 package information

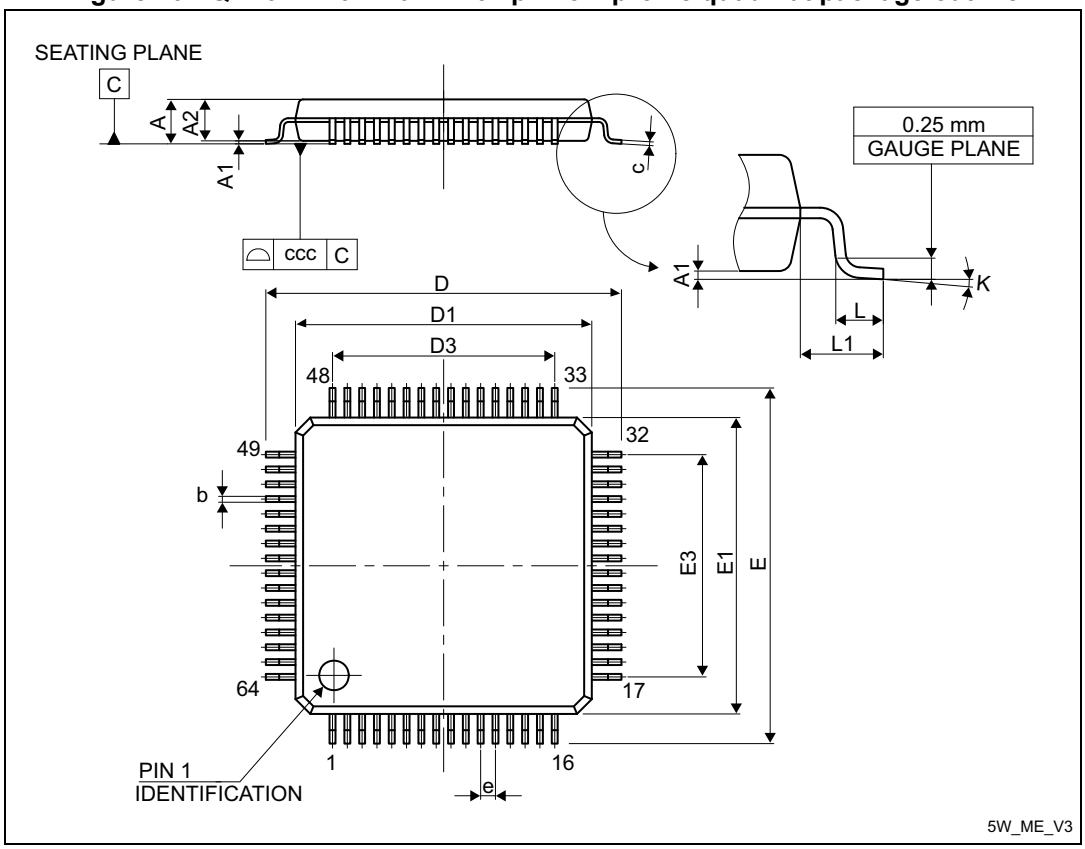
**Figure 37. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline**




1. Drawing is not to scale. Dimensions are in millimeters.

## 6.2 LQFP64 package information

**Figure 40.LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline**




1. Drawing is not in scale.

**Table 49. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | - | 12.000 | - | - | 0.4724 | - |
| D1 | - | 10.000 | - | - | 0.3937 | - |
| D3 | - | 7.500 | - | - | 0.2953 | - |
| E | - | 12.000 | - | - | 0.4724 | - |
| E1 | - | 10.000 | - | - | 0.3937 | - |
| E3 | - | 7.500 | - | - | 0.2953 | - |

**Table 50. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| E1 | - | 3.500 | - | - | 0.1378 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| F | - | 0.750 | - | - | 0.0295 | - |
| ddd | - | - | 0.080 | - | - | 0.0031 |
| eee | - | - | 0.150 | - | - | 0.0059 |
| fff | - | - | 0.050 | - | - | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 44. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array, recommended footprint**

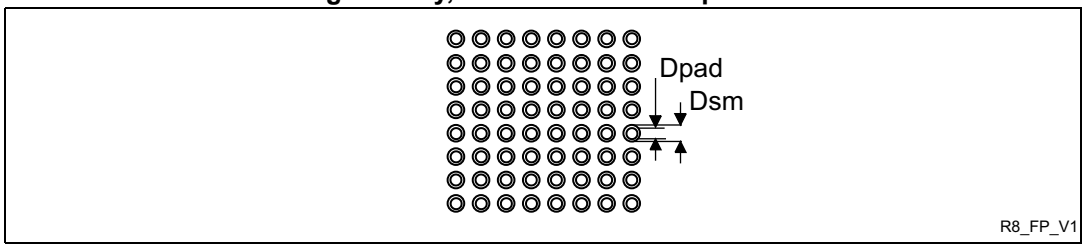
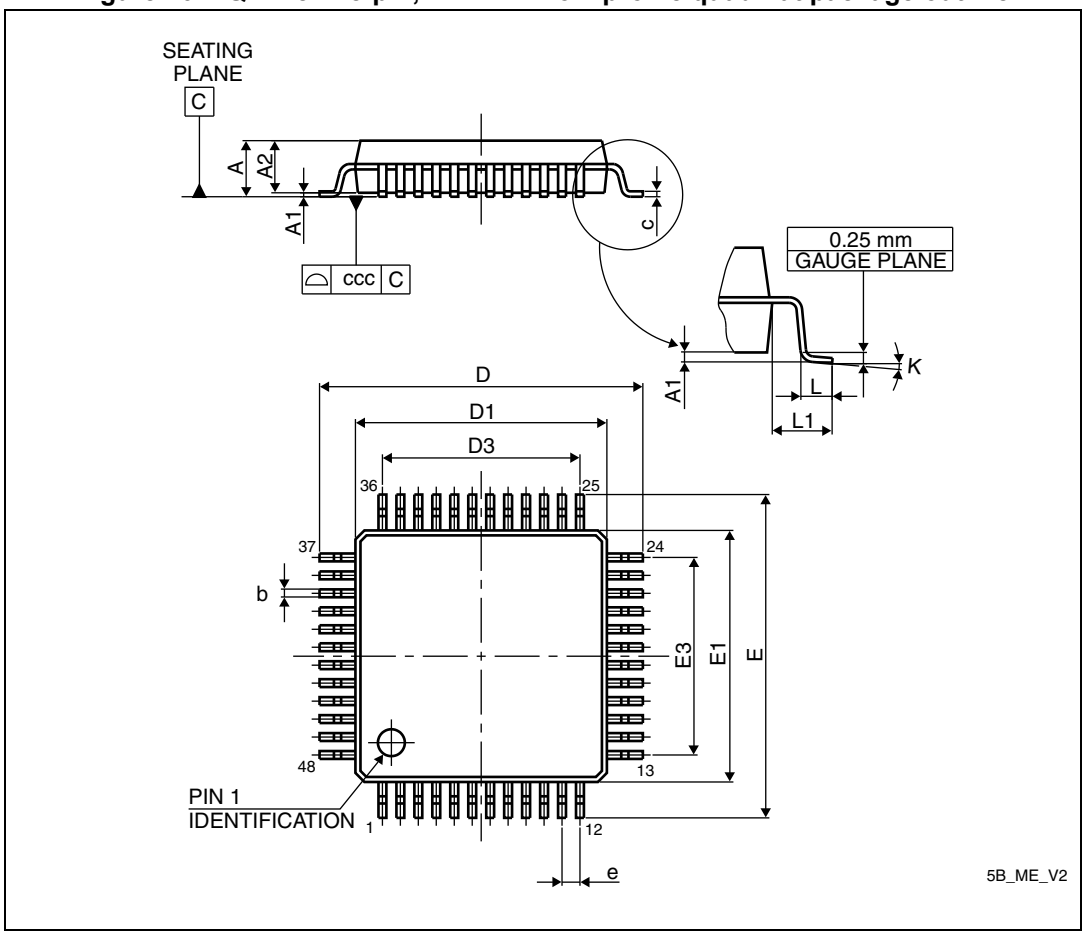



**Table 51. TFBGA64 recommended PCB design rules (0.5 mm pitch BGA)**

| Dimension | Recommended values |
|---|---|
| Pitch | 0.5 |
| Dpad | 0.280 mm |
| Dsm | 0.370 mm typ. (depends on the soldermask registration tolerance) |
| Stencil opening | 0.280 mm |
| Stencil thickness | Between 0.100 mm and 1.125 mm |
| Pad trace width | 0.100 mm |

## 6.4 LQFP48 package information

**Figure 46. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline**




1. Drawing is not to scale.

**Table 52. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | - | 5.500 | - | - | 0.2165 | - |
| E | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |

# 8 Revision history

**Table 55. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 12-Oct-2009 | 1 | Initial release. |
| 26-Feb-2010 | 2 | TFBGA64 package added (see *Table 50* and *Table 41*).<br>*Note 5* modified in *Table 4: Low & medium-density STM32F100xx pin definitions*.<br>$I_{INJ(PIN)}$ modified in *Table 6: Current characteristics*. Conditions removed from *Table 25: Low-power mode wakeup timings*.<br>Notes modified in *Table 34: I/O static characteristics*.<br>*Figure 27: Recommended NRST pin protection* modified.<br>Note modified in *Table 39: I2C characteristics*. *Figure 28: I2C bus AC waveforms and measurement circuit(1)* modified.<br>*Table 46: DAC characteristics* modified. *Figure 36: 12-bit buffered /non-buffered DAC* added.<br>*TIM2, TIM3, TIM4* and *TIM15, TIM16 and TIM17* updated.<br>HDMI-CEC electrical characteristics added.<br>Values added to:<br>– *Table 12: Maximum current consumption in Run mode, code with data processing running from Flash*<br>– *Table 13: Maximum current consumption in Run mode, code with data processing running from RAM*<br>– *Table 14: Maximum current consumption in Sleep mode, code running from Flash or RAM*<br>– *Table 15: Typical and maximum current consumptions in Stop and Standby modes*<br>– *Table 18: Peripheral current consumption*<br>– *Table 29: EMS characteristics*<br>– *Table 30: EMI characteristics*<br>– *Table 47: TS characteristics*<br>*Section 5.3.12: I/O current injection characteristics* modified.<br>Added figures:<br>– *Figure 12: Maximum current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled*<br>– *Figure 13: Maximum current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled*<br>– *Figure 15: Typical current consumption in Stop mode with regulator in Run mode versus temperature at VDD = 3.3 V and 3.6 V*<br>– *Figure 16: Typical current consumption in Stop mode with regulator in Low-power mode versus temperature at VDD = 3.3 V and 3.6 V*<br>– *Figure 17: Typical current consumption in Standby mode versus temperature at VDD = 3.3 V and 3.6 V* |

**Table 55. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 08-Jun-2012 | 7 | Updated *Table 6: Current characteristics on page 34*<br>Updated *Table 39: I2C characteristics on page 64*<br>Corrected note “non-robust “ in *Section 5.3.17: 12-bit ADC characteristics on page 68*<br>Updated *Section 5.3.13: I/O port characteristics on page 57*<br>Updated *Section 2.2.20: GPIOs (general-purpose inputs/outputs) on page 20*<br>Updated *Table 4: Low & medium-density STM32F100xx pin definitions on page 24*<br>Updated *Section 5.3.1: General operating conditions on page 34*<br>Updated *Table 14: Maximum current consumption in Sleep mode, code running from Flash or RAM on page 39* |
| 08-Jun-2015 | 8 | Updated *Table 18: Peripheral current consumption*, *Table 31: ESD absolute maximum ratings*, *Table 48: LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data*, *Table 49: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data*, *Table 50: TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package mechanical data*, *Table 51: TFBGA64 recommended PCB design rules (0.5 mm pitch BGA)* and *Table 52: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data*.<br>Updated *Figure 37: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline*, *Figure 38: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint*, *Figure 40: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline*, *Figure 41: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint*, *Figure 43: TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch thin profile fine pitch ball grid array package outline*, *Figure 44: TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array, recommended footprint*, *Figure 46: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline* and *Figure 47: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint*.<br>Added *Figure 39: LQFP100 marking example (package top view)*, *Figure 42: LQFP64 marking example (package top view) Figure 45: TFBGA64 marking example (package top view)* and *Figure 48: LQFP48 marking example (package top view)*. |
| 21-Nov-2016 | 9 | Updated:<br>– *Figure 7: Memory map*<br>– *Figure 18: High-speed external clock source AC timing diagram*<br>– *Figure 19: Low-speed external clock source AC timing diagram*<br>– *Table 19: High-speed external user clock characteristics*<br>– *Table 20: Low-speed external user clock characteristics*<br>– *Table 42: ADC characteristics* |