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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f100r8t6btr

Contents

List of figures

Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard TIM timers which have the same architecture. The advanced control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIM2, TIM3, TIM4, TIM15, TIM16 & TIM17)

There are six synchronizable general-purpose timers embedded in the STM32F100xx devices (see *Table 3* for differences). Each general-purpose timers can be used to generate PWM outputs, or as simple time base.

TIM2, TIM3, TIM4

STM32F100xx devices feature three synchronizable 4-channels general-purpose timers. These timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2, TIM3, TIM4 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2, TIM3, TIM4 all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

TIM15, TIM16 and TIM17

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate with TIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16, and TIM17 have a complementary output with dead-time generation and independent DMA request generation

Figure 6. STM32F100xx value line TFBGA64 ballout

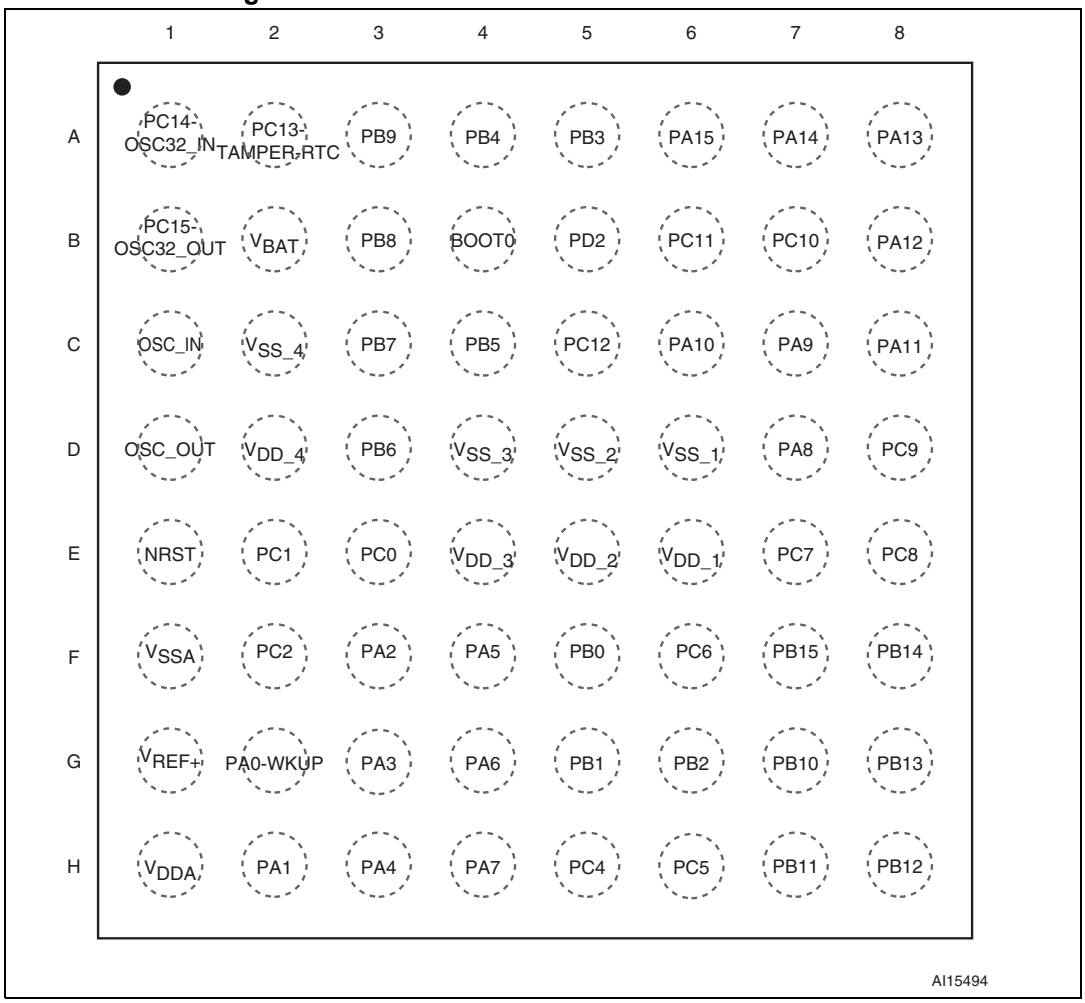


Table 4. Low & medium-density STM32F100xx pin definitions

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3)(4)	
LQFP100	LQFP64	TFBGA64	LQFP48					Default	Remap
1	-	-	-	PE2	I/O	FT	PE2	TRACECLK	-
2	-	-	-	PE3	I/O	FT	PE3	TRACED0	-
3	-	-	-	PE4	I/O	FT	PE4	TRACED1	-
4	-	-	-	PE5	I/O	FT	PE5	TRACED2	-
5	-	-	-	PE6	I/O	FT	PE6	TRACED3	-
6	1	B2	1	V_{BAT}	S	-	V_{BAT}	-	-
7	2	A2	2	PC13-TAMPER-RTC(5)	I/O	-	PC13(6)	TAMPER-RTC	-
8	3	A1	3	PC14-OSC32_IN(5)	I/O	-	PC14(6)	OSC32_IN	-

Table 4. Low & medium-density STM32F100xx pin definitions (continued)

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3)(4)	
LQFP100	LQFP64	TFBGA64	LQFP48					Default	Remap
9	4	B1	4	PC15-OSC32_OUT(5)	I/O	-	PC15(6)	OSC32_OUT	-
10	-	-	-	V_{SS_5}	S	-	V_{SS_5}	-	-
11	-	-	-	V_{DD_5}	S	-	V_{DD_5}	-	-
12	5	C1	5	OSC_IN	I	-	OSC_IN	-	PD0(7)
13	6	D1	6	OSC_OUT	O	-	OSC_OUT	-	PD1(7)
14	7	E1	7	NRST	I/O	-	NRST	-	-
15	8	E3	-	PC0	I/O	-	PC0	ADC1_IN10	-
16	9	E2	-	PC1	I/O	-	PC1	ADC1_IN11	-
17	10	F2	-	PC2	I/O	-	PC2	ADC1_IN12	-
18	11	-(8)	-	PC3	I/O	-	PC3	ADC1_IN13	-
19	12	F1	8	V_{SSA}	S	-	V_{SSA}	-	-
20	-	-	-	V_{REF-}	S	-	V_{REF-}	-	-
21	-	G1	-	V_{REF+}	S	-	V_{REF+}	-	-
22	13	H1	9	V_{DDA}	S	-	V_{DDA}	-	-
23	14	G2	10	PA0-WKUP	I/O	-	PA0	WKUP / USART2_CTS(12)/ ADC1_IN0 / TIM2_CH1_ETR(12)	-
24	15	H2	11	PA1	I/O	-	PA1	USART2_RTS(12)/ ADC1_IN1 / TIM2_CH2(12)	-
25	16	F3	12	PA2	I/O	-	PA2	USART2_TX(12)/ ADC1_IN2 / TIM2_CH3(12)/ TIM15_CH1(12)	-
26	17	G3	13	PA3	I/O	-	PA3	USART2_RX(12)/ ADC1_IN3 / TIM2_CH4(12) / TIM15_CH2(12)	-
27	18	C2	-	V_{SS_4}	S	-	V_{SS_4}	-	-
28	19	D2	-	V_{DD_4}	S	-	V_{DD_4}	-	-
29	20	H3	14	PA4	I/O	-	PA4	SPI1_NSS(12)/ADC1_IN4 USART2_CK(12) / DAC1_OUT	-
30	21	F4	15	PA5	I/O	-	PA5	SPI1_SCK(12)/ADC1_IN5 / DAC2_OUT	-
31	22	G4	16	PA6	I/O	-	PA6	SPI1_MISO(12)/ADC1_IN6 / TIM3_CH1(12)	TIM1_BKIN / TIM16_CH1
32	23	H4	17	PA7	I/O	-	PA7	SPI1_MOSI(12)/ADC1_IN7 / TIM3_CH2(12)	TIM1_CH1N / TIM17_CH1

Table 4. Low & medium-density STM32F100xx pin definitions (continued)

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3)(4)	
LQFP100	LQFP64	TFBGA64	LQFP48					Default	Remap
57	-	-	-	PD10	I/O	FT	PD10	-	USART3_CK
58	-	-	-	PD11	I/O	FT	PD11	-	USART3_CTS
59	-	-	-	PD12	I/O	FT	PD12	-	TIM4_CH1(11) / USART3_RTS
60	-	-	-	PD13	I/O	FT	PD13	-	TIM4_CH2(11)
61	-	-	-	PD14	I/O	FT	PD14	-	TIM4_CH3(11)
62	-	-	-	PD15	I/O	FT	PD15	-	TIM4_CH4(11)
63	37	F6	-	PC6	I/O	FT	PC6	-	TIM3_CH1
64	38	E7	-	PC7	I/O	FT	PC7	-	TIM3_CH2
65	39	E8	-	PC8	I/O	FT	PC8	-	TIM3_CH3
66	40	D8	-	PC9	I/O	FT	PC9	-	TIM3_CH4
67	41	D7	29	PA8	I/O	FT	PA8	USART1_CK / MCO / TIM1_CH1	-
68	42	C7	30	PA9	I/O	FT	PA9	USART1_TX(12) / TIM1_CH2 / TIM15_BKIN	-
69	43	C6	31	PA10	I/O	FT	PA10	USART1_RX(12) / TIM1_CH3 / TIM17_BKIN	-
70	44	C8	32	PA11	I/O	FT	PA11	USART1_CTS / TIM1_CH4	-
71	45	B8	33	PA12	I/O	FT	PA12	USART1_RTS / TIM1_ETR	-
72	46	A8	34	PA13	I/O	FT	JTMS-SWDIO	-	PA13
73	-	-	-	Not connected					-
74	47	D5	35	V_{SS_2}	S	-	V_{SS_2}	-	-
75	48	E5	36	V_{DD_2}	S	-	V_{DD_2}	-	-
76	49	A7	37	PA14	I/O	FT	JTCK/SWCLK	-	PA14
77	50	A6	38	PA15	I/O	FT	JTDI	-	TIM2_CH1_ETR/ PA15/ SPI1_NSS
78	51	B7	-	PC10	I/O	FT	PC10	-	USART3_TX

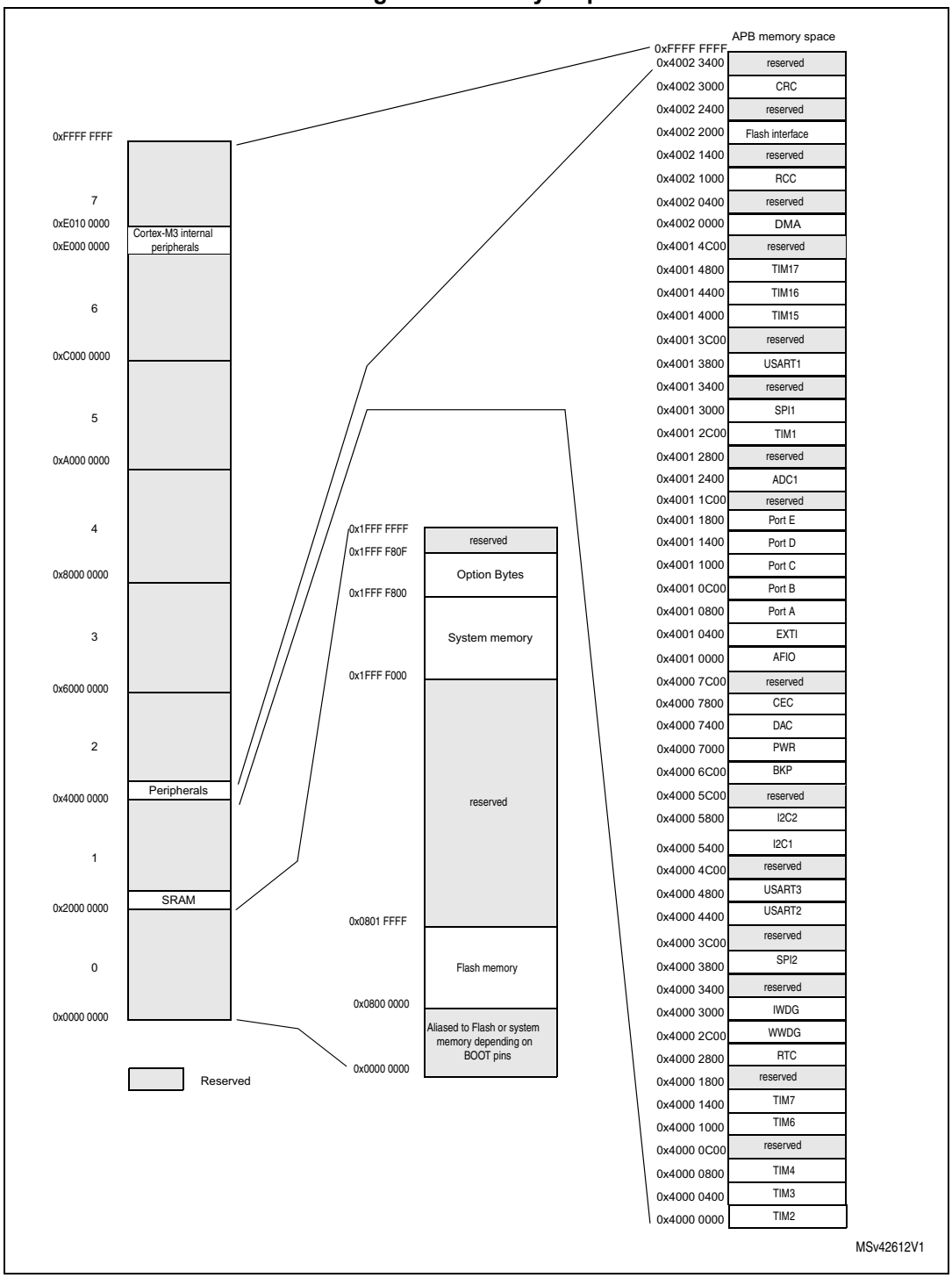
Table 4. Low & medium-density STM32F100xx pin definitions (continued)

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3)(4)	
LQFP100	LQFP64	TFBGA64	LQFP48					Default	Remap
79	52	B6	-	PC11	I/O	FT	PC11	-	USART3_RX
80	53	C5	-	PC12	I/O	FT	PC12	-	USART3_CK
81	-	C1	-	PD0	I/O	FT	PD0	-	-
82	-	D1	-	PD1	I/O	FT	PD1	-	-
83	54	B5	-	PD2	I/O	FT	PD2	TIM3_ETR	-
84	-	-	-	PD3	I/O	FT	PD3	-	USART2_CTS
85	-	-	-	PD4	I/O	FT	PD4	-	USART2_RTS
86	-	-	-	PD5	I/O	FT	PD5	-	USART2_TX
87	-	-	-	PD6	I/O	FT	PD6	-	USART2_RX
88	-	-	-	PD7	I/O	FT	PD7	-	USART2_CK
89	55	A5	39	PB3	I/O	FT	JTDO		TIM2_CH2 / PB3 TRACESWO SPI1_SCK
90	56	A4	40	PB4	I/O	FT	NJTRST	-	PB4 / TIM3_CH1 SPI1_MISO
91	57	C4	41	PB5	I/O	-	PB5	I2C1_SMBA / TIM16_BKIN	TIM3_CH2 / SPI1_MOSI
92	58	D3	42	PB6	I/O	FT	PB6	I2C1_SCL(12)/ TIM4_CH1(11)(12) TIM16_CH1N	USART1_TX
93	59	C3	43	PB7	I/O	FT	PB7	I2C1_SDA(12)/ TIM17_CH1N TIM4_CH2(11)(12)	USART1_RX
94	60	B4	44	BOOT0	I	-	BOOT0	-	-
95	61	B3	45	PB8	I/O	FT	PB8	TIM4_CH3(11)(12) / TIM16_CH1(12) / CEC(12)	I2C1_SCL
96	62	A3	46	PB9	I/O	FT	PB9	TIM4_CH4(11)(12) / TIM17_CH1(12)	I2C1_SDA
97	-	-	-	PE0	I/O	FT	PE0	TIM4_ETR(11)	-
98	-	-	-	PE1	I/O	FT	PE1	-	-
99	63	D4	47	V_{SS_3}	S	-	V_{SS_3}	-	-
100	64	E4	48	V_{DD_3}	S	-	V_{DD_3}	-	-

4 Memory mapping

The memory map is shown in *Figure 7*.

Figure 7. Memory map



5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 2 V ≤V_{DD} ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

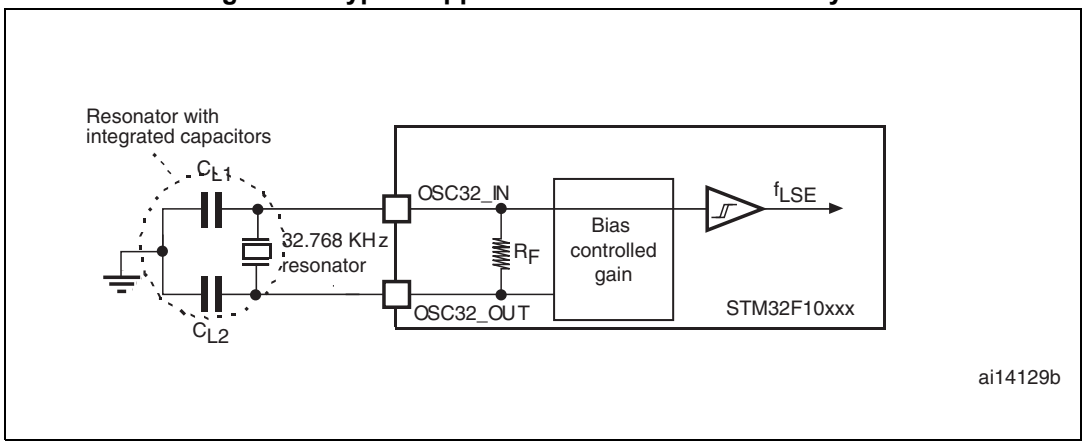
5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

Figure 21. Typical application with a 32.768 kHz crystal



5.3.7 Internal clock source characteristics

The parameters given in *Table 23* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

High-speed internal (HSI) RC oscillator

Table 23. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
$DuCy_{(HSI)}$	Duty cycle	-	45	-	55	%
ACC_{HSI}	Accuracy of HSI oscillator	T_A = –40 to 105 °C(2)	-2.4	-	2.5	%
		T_A = –10 to 85 °C(2)	-2.2	-	1.3	%
		T_A = 0 to 70 °C(2)	-1.9	-	1.3	%
		T_A = 25 °C	-1	-	1	%
$t_{su(HSI)}$(3)	HSI oscillator startup time	-	1	-	2	µs
$I_{DD(HSI)}$(3)	HSI oscillator power consumption	-	-	80	100	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C °C unless otherwise specified.
2. Guaranteed by characterization results.
3. Guaranteed by design. Not tested in production

5.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 33*

Table 33. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	-0	+0	mA
	Injected current on all FT pins	-5	+0	
	Injected current on any other pin	-5	+5	

Figure 22. Standard I/O input characteristics - CMOS port

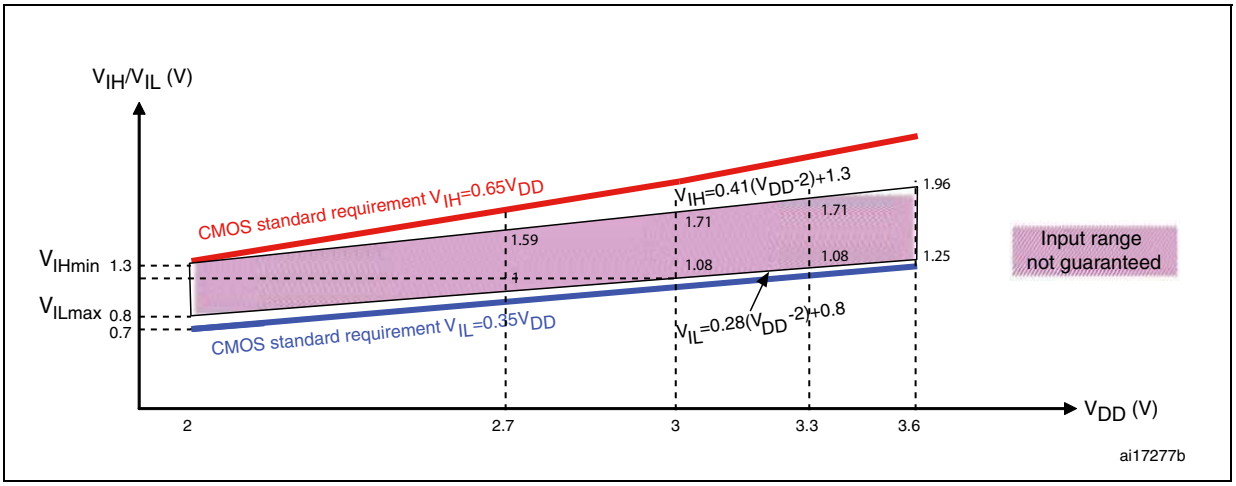
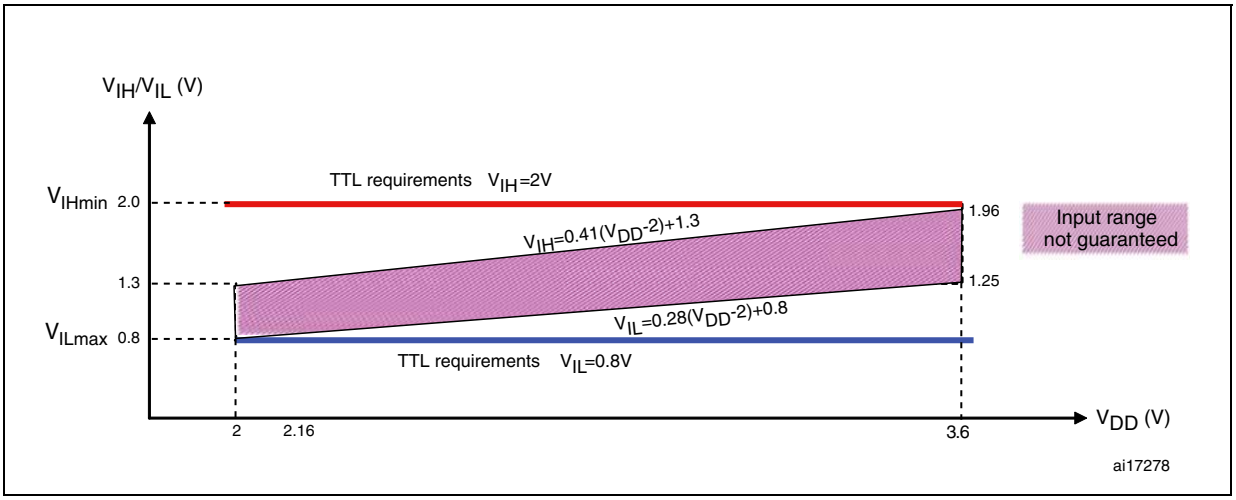


Figure 23. Standard I/O input characteristics - TTL port



Output voltage levels

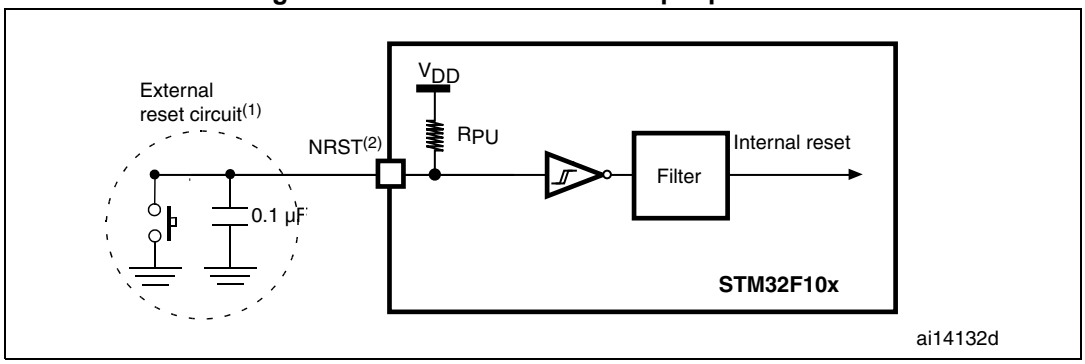
Unless otherwise specified, the parameters given in *Table 35* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*. All I/Os are CMOS and TTL compliant.

Table 35. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output Low level voltage for an I/O pin when 8 pins are sunk at the same time	CMOS port(2) I_{IO} = +8 mA, 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output High level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	TTL port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		2.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +20 mA(4) 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH} (3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–1.3	-	
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +6 mA(4) 2 V < V_{DD} < 2.7 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 6* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 6* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Based on characterization data, not tested in production.

Figure 27. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 37*. Otherwise the reset will not be taken into account by the device.

5.3.15 TIMx characteristics

The parameters given in *Table 38* are guaranteed by design.

Refer to *Section 5.3.12: I/O current injection characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 38. TIMx characteristics

Symbol	Parameter	Conditions(1)	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 24 MHz	41.7	-	ns
f_{EXT}	Timer external clock frequency on CHx(2)		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 24 MHz	0	12	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock period when the internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 24 MHz	-	2730	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 24 MHz	-	178	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3, TIM4, TIM15, TIM16 and TIM17 timers.
2. CHx is used as a general term to refer to CH1 to CH4 for TIM1, TIM2, TIM3 and TIM4, to the CH1 to CH2 for TIM15, and to CH1 for TIM16 and TIM17.

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 41* are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 8*.

Refer to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 41. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	12	MHz
		Slave mode	-	12	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		8	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	$2t_{PCLK}$	-	
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode, f_{PCLK} = 24 MHz, presc = 4	50	60	
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode	5	-	
		Slave mode	5	-	
$t_{h(MI)}$ (1)	Data input hold time	Master mode	5	-	
$t_{h(SI)}$ (1)		Slave mode	4	-	
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode, f_{PCLK} = 24 MHz	0	$3t_{PCLK}$	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	2	10	
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)	-	25	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-	5	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{h(MO)}$ (1)		Master mode (after enable edge)	2	-	

1. Guaranteed by characterization results.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Table 42. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
I_{VREF}	Current on the V_{REF} input pin	-	-	160(1)	220(1)	µA
f_{ADC}	ADC clock frequency	-	0.6	-	12	MHz
f_S(2)	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 12 MHz	-	-	705	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}(3)	Conversion voltage range	-	0 (V_{SSA} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* and *Table 43* for details	-	-	50	kΩ
R_{ADC}(2)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 12 MHz	6.9			µs
		-	83			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 12 MHz	-	-	0.25	µs
		-	-	-	3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 12 MHz	-	-	0.166	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 12 MHz	0.125	-	20.0	µs
			1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	0	0	1	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 12 MHz	1.17	-	21	µs
		-	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Based on characterization results, not tested in production.
2. Guaranteed by design.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Table 4: Low & medium-density STM32F100xx pin definitions* and *Figure 6* for further details.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 42*.

Equation 1: R_{AIN} max formula:

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

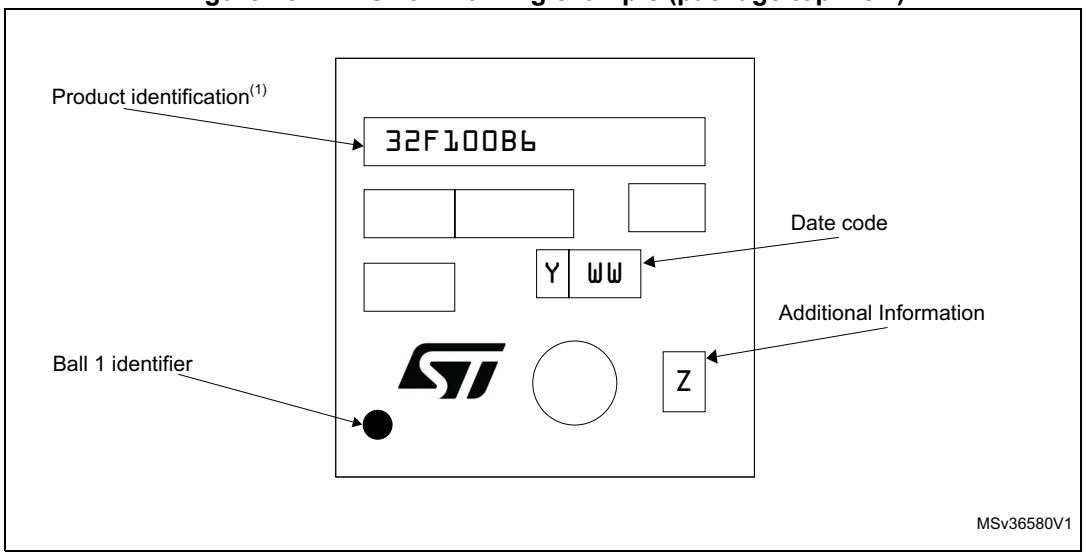
The above formula (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Device marking for TFBGA64

The following figure gives an example of topside marking and pin 1 position identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 45. TFBGA64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.