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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f100r8t7b

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2 Description

The STM32F100x4, STM32F100x6, STM32F100x8 and STM32F100xB microcontrollers incorporate the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a 24 MHz frequency, high-speed embedded memories (Flash memory up to 128 Kbytes and SRAM up to 8 Kbytes), and an extensive range of enhanced peripherals and I/Os connected to two APB buses. All devices offer standard communication interfaces (up to two I²Cs, two SPIs, one HDMI CEC, and up to three USARTs), one 12-bit ADC, two 12-bit DACs, up to six general-purpose 16-bit timers and an advanced-control PWM timer.

The STM32F100xx low- and medium-density devices operate in the – 40 to + 85 °C and – 40 to + 105 °C temperature ranges, from a 2.0 to 3.6 V power supply.

A comprehensive set of power-saving mode allows the design of low-power applications.

These microcontrollers include devices in three different packages ranging from 48 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included.

These features make these microcontrollers suitable for a wide range of applications such as application control and user interfaces, medical and hand-held equipment, PC and gaming peripherals, GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms, and HVACs.

2.1 Device overview

The description below gives an overview of the complete range of peripherals proposed in this family.

[Figure 1](#) shows the general block diagram of the device family.

Table 2. STM32F100xx features and peripheral counts

Peripheral		STM32F100Cx				STM32F100Rx				STM32F100Vx	
Flash - Kbytes		16	32	64	128	16	32	64	128	64	128
SRAM - Kbytes		4	4	8	8	4	4	8	8	8	8
Timers	Advanced-control	1		1		1		1		1	
	General-purpose	5 ⁽¹⁾		6		5 ⁽¹⁾		6		6	
Communication interfaces	SPI	1 ⁽²⁾		2		1 ⁽²⁾		2		2	
	I ² C	1 ⁽³⁾		2		1 ⁽³⁾		2		2	
	USART	2 ⁽⁴⁾		3		2 ⁽⁴⁾		3		3	
	CEC	1									
12-bit synchronized ADC number of channels		1 10 channels				1 16 channels				1 16 channels	
GPIOs		37				51				80	
12-bit DAC Number of channels		2 2									
CPU frequency		24 MHz									
Operating voltage		2.0 to 3.6 V									
Operating temperatures		Ambient operating temperature: −40 to +85 °C /−40 to +105 °C (see Table 8) Junction temperature: −40 to +125 °C (see Table 8)									
Packages		LQFP48				LQFP64, TFBGA64				LQFP100	

1. TIM4 not present.
2. SPI2 is not present.
3. I2C2 is not present.
4. USART3 is not present.

higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

2.2.11 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop mode
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode, providing high impedance output.

2.2.12 Low-power modes

The STM32F100xx value line supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**
In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Stop mode**
Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.
The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output or the RTC alarm.
- **Standby mode**
The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.
The device exits Standby mode when an external reset (NRST pin), a IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.2.13 DMA

The flexible 7-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

Table 6. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source) ⁽¹⁾	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink) ⁽¹⁾	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	-25	
$I_{INJ(PIN)}^{(2)}$	Injected current on five volt tolerant pins ⁽³⁾	-5 / +0	
	Injected current on any other pin ⁽⁴⁾	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) ⁽⁵⁾	± 25	

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See [Note: on page 70](#).
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to [Table 5: Voltage characteristics](#) for the maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to [Table 5: Voltage characteristics](#) for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 7. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	150	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 8. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	24	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	24	
f_{PCLK2}	Internal APB2 clock frequency	-	0	24	
V_{DD}	Standard operating voltage	-	2	3.6	V
$V_{DDA}^{(1)}$	Analog operating voltage (ADC not used)	Must be the same potential as V_{DD}	2	3.6	V
	Analog operating voltage (ADC used)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.8	3.6	V

Table 12. Maximum current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Max ⁽¹⁾		Unit
				$T_A = 85\text{ °C}$	$T_A = 105\text{ °C}$	
I_{DD}	Supply current in Run mode	External clock ⁽²⁾ , all peripherals enabled	24 MHz	15.4	15.7	mA
			16 MHz	11	11.5	
			8 MHz	6.7	6.9	
		External clock ⁽²⁾ , all peripherals disabled	24 MHz	10.3	10.5	
			16 MHz	7.8	8.1	
			8 MHz	5.1	5.3	

1. Guaranteed by characterization results.

2. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8\text{ MHz}$.

Table 13. Maximum current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max ⁽¹⁾		Unit
				$T_A = 85\text{ °C}$	$T_A = 105\text{ °C}$	
I_{DD}	Supply current in Run mode	External clock ⁽²⁾ , all peripherals enabled	24 MHz	14.5	15	mA
			16 MHz	10	10.5	
			8 MHz	6	6.3	
		External clock ⁽²⁾ all peripherals disabled	24MHz	9.3	9.7	
			16 MHz	6.8	7.2	
			8 MHz	4.4	4.7	

1. Guaranteed by characterization, tested in production at V_{DD} max, f_{HCLK} max.

2. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8\text{ MHz}$.

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

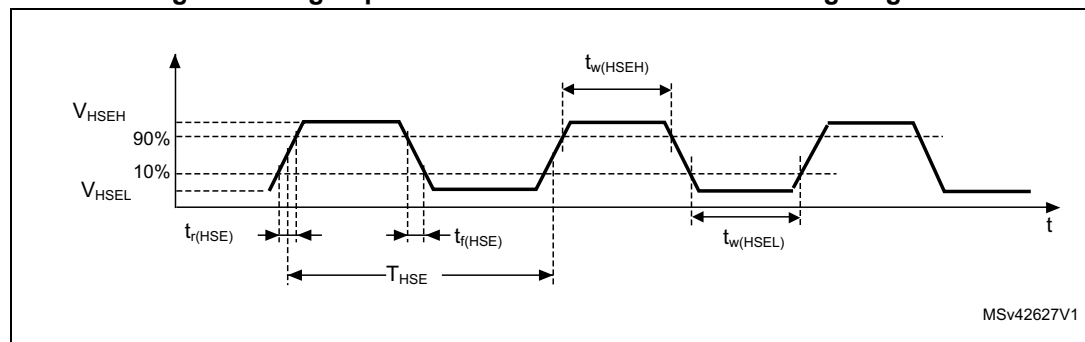
The characteristics given in [Table 19](#) result from tests performed using an high-speed external clock source, and under the ambient temperature and supply voltage conditions summarized in [Table 8](#).

Table 19. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency ⁽¹⁾	-	1	8	24	MHz
V_{HSEH}	OSC_IN input pin high level voltage ⁽¹⁾		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage ⁽¹⁾		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time ⁽¹⁾		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time ⁽¹⁾		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance ⁽¹⁾	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle ⁽¹⁾	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	± 1	μA

1. Guaranteed by design.

Figure 18. High-speed external clock source AC timing diagram



5.3.8 PLL characteristics

The parameters given in [Table 26](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 8](#).

Table 26. PLL characteristics

Symbol	Parameter	Value			Unit
		Min ⁽¹⁾	Typ	Max ⁽¹⁾	
f _{PLL_IN}	PLL input clock ⁽²⁾	1	8.0	24	MHz
	PLL input clock duty cycle	40	-	60	%
f _{PLL_OUT}	PLL multiplier output clock	16	-	24	MHz
t _{LOCK}	PLL lock time	-	-	200	μs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

1. Guaranteed by characterization results.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (Electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB: A Burst of Fast Transient voltage** (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 29](#). They are based on the EMS levels and classes defined in application note AN1709.

Table 29. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, $T_A = +25\text{ °C}$, $f_{HCLK} = 24\text{ MHz}$, LQFP100 package, conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, $T_A = +25\text{ °C}$, $f_{HCLK} = 24\text{ MHz}$, LQFP100 package, conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

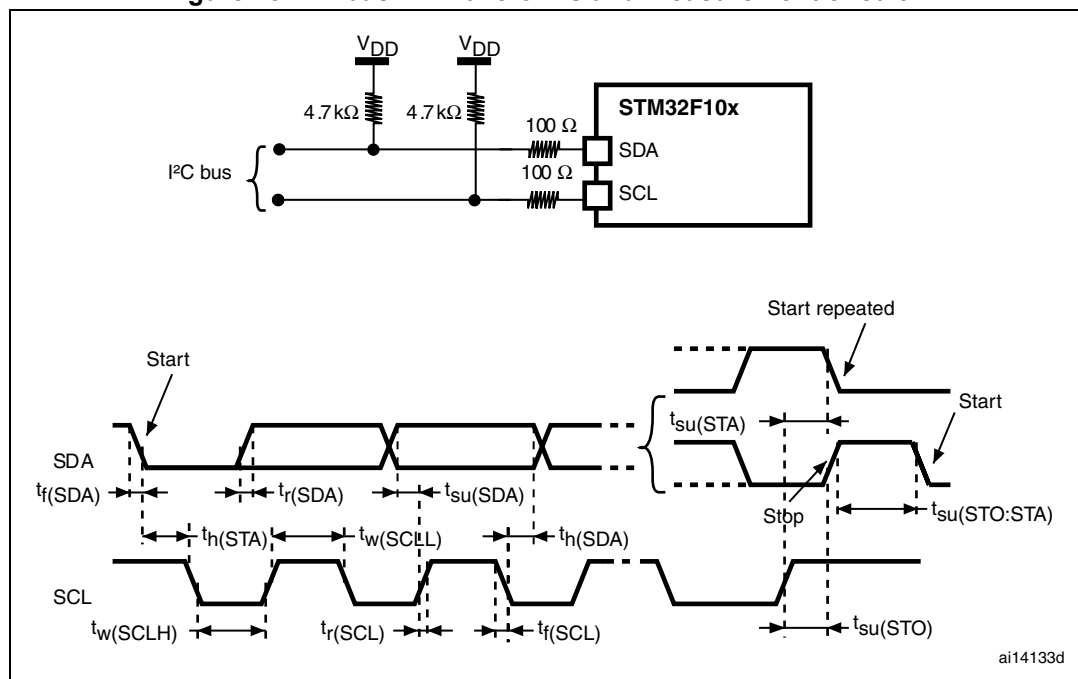
Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second. To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Figure 28. I²C bus AC waveforms and measurement circuit⁽¹⁾

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 40. SCL frequency ($f_{PCLK1} = 24 \text{ MHz}$, $V_{DD} = 3.3 \text{ V}$)⁽¹⁾⁽²⁾

$f_{SCL} \text{ (kHz)}^{(3)}$	I2C_CCR value
	$R_P = 4.7 \text{ k}\Omega$
400	0x8011
300	0x8016
200	0x8021
100	0x0064
50	0x00C8
20	0x01F4

- R_P = External pull-up resistance, f_{SCL} = I²C speed,
- For speeds around 400 kHz, the tolerance on the achieved speed is of $\pm 2\%$. For other speed ranges, the tolerance on the achieved speed $\pm 1\%$. These variations depend on the accuracy of the external components used to design the application.
- Guaranteed by design.

Table 43. R_{AIN} max for $f_{ADC} = 12\text{ MHz}^{(1)}$

T_s (cycles)	t_s (μs)	R_{AIN} max ($k\Omega$)
1.5	0.125	0.4
7.5	0.625	5.9
13.5	1.125	11.4
28.5	2.375	25.2
41.5	3.45	37.2
55.5	4.625	50
71.5	5.96	NA
239.5	20	NA

1. Guaranteed by design.

Table 44. ADC accuracy - limited test conditions⁽¹⁾⁽²⁾

Symbol	Parameter	Test conditions	Typ	Max	Unit
ET	Total unadjusted error	$f_{PCLK2} = 24\text{ MHz}$, $f_{ADC} = 12\text{ MHz}$, $R_{AIN} < 10\text{ k}\Omega$, $V_{DDA} = 3\text{ V to } 3.6\text{ V}$, $V_{REF+} = V_{DDA}$, $T_A = 25\text{ }^\circ\text{C}$ Measurements made after ADC calibration	± 1.3	± 2.2	LSB
EO	Offset error		± 1	± 1.5	
EG	Gain error		± 0.5	± 1.5	
ED	Differential linearity error		± 0.7	± 1	
EL	Integral linearity error		± 0.8	± 1.5	

1. ADC DC accuracy values are measured after internal calibration.

2. Guaranteed by characterization results.

Table 45. ADC accuracy^{(1) (2) (3)}

Symbol	Parameter	Test conditions	Typ	Max	Unit
ET	Total unadjusted error	$f_{PCLK2} = 24\text{ MHz}$, $f_{ADC} = 12\text{ MHz}$, $R_{AIN} < 10\text{ k}\Omega$, $V_{DDA} = 2.4\text{ V to } 3.6\text{ V}$, $T_A = \text{Full operating range}$ Measurements made after ADC calibration	± 2	± 5	LSB
EO	Offset error		± 1.5	± 2.5	
EG	Gain error		± 1.5	± 3	
ED	Differential linearity error		± 1	± 2	
EL	Integral linearity error		± 1.5	± 3	

1. ADC DC accuracy values are measured after internal calibration.

2. Better performance could be achieved in restricted V_{DD} , frequency, V_{REF} and temperature ranges.

3. Guaranteed by characterization results.

Note: ADC accuracy vs. negative injection current: Injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in [Section 5.3.12](#) does not affect the ADC accuracy.

Figure 32. ADC accuracy characteristics

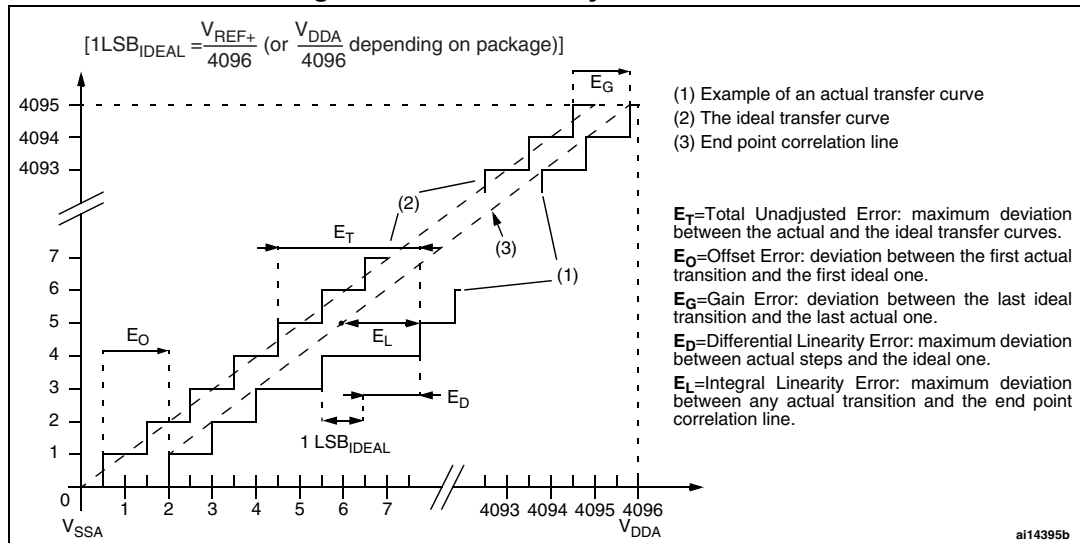
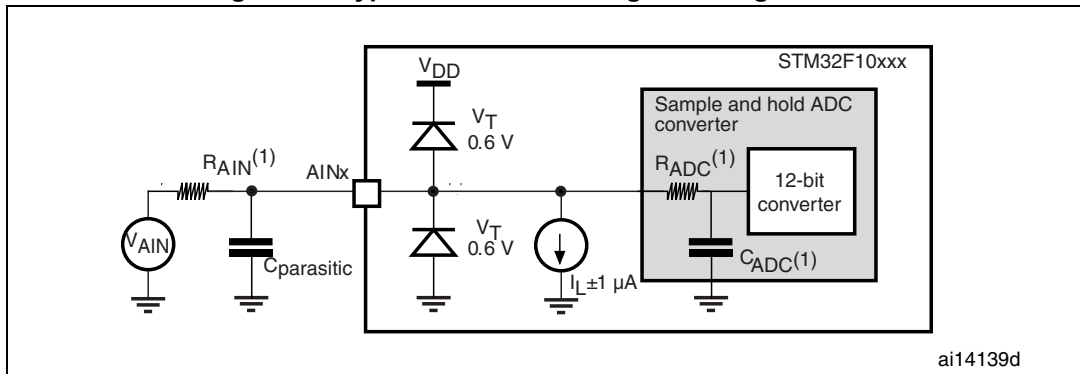


Figure 33. Typical connection diagram using the ADC



1. Refer to [Table 42](#) for the values of R_{AIN} , R_{ADC} and C_{ADC} .
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in [Figure 34](#) or [Figure 35](#), depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

5.3.18 DAC electrical specifications

Table 46. DAC characteristics

Symbol	Parameter	Min	Typ	Max ⁽¹⁾	Unit	Comments
V _{DDA}	Analog supply voltage	2.4	-	3.6	V	-
V _{REF+}	Reference supply voltage	2.4	-	3.6	V	V _{REF+} must always be below V _{DDA}
V _{SSA}	Ground	0	-	0	V	-
R _{LOAD} ⁽²⁾	Resistive load with buffer ON	5	-	-	kΩ	-
R _O ⁽¹⁾	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V _{SS} to have a 1% accuracy is 1.5 MΩ
C _{LOAD} ⁽¹⁾	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min ⁽¹⁾	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V _{REF+} = 3.6 V and (0x155) and (0xEAB) at V _{REF+} = 2.4 V
DAC_OUT max ⁽¹⁾	Higher DAC_OUT voltage with buffer ON	-	-	V _{DDA} - 0.2	V	
DAC_OUT min ⁽¹⁾	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max ⁽¹⁾	Higher DAC_OUT voltage with buffer OFF	-	-	V _{REF+} - 1LSB	V	
I _{DDVREF+}	DAC DC current consumption in quiescent mode (Standby mode)	-	-	220	μA	With no load, worst code (0xF1C) at V _{REF+} = 3.6 V in terms of DC consumption on the inputs
I _{DDA}	DAC DC current consumption in quiescent mode (Standby mode)	-	-	380	μA	With no load, middle code (0x800) on the inputs
		-	-	480	μA	With no load, worst code (0xF1C) at V _{REF+} = 3.6 V in terms of DC consumption on the inputs
DNL ⁽¹⁾	Differential non linearity Difference between two consecutive code-1LSB)	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration
		-	-	±2	LSB	Given for the DAC in 12-bit configuration
INL ⁽¹⁾	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	±1	LSB	Given for the DAC in 10-bit configuration
		-	-	±4	LSB	Given for the DAC in 12-bit configuration

5.3.19 Temperature sensor characteristics

Table 47. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	V_{SENSE} linearity with temperature	-	± 1	± 2	$^{\circ}\text{C}$
Avg_Slope ⁽¹⁾	Average slope	4.0	4.3	4.6	mV/ $^{\circ}\text{C}$
$V_{25}^{(1)}$	Voltage at 25 $^{\circ}\text{C}$	1.32	1.41	1.50	V
$t_{START}^{(2)}$	Startup time	4	-	10	μs
$T_{S_temp}^{(3)(2)}$	ADC sampling time when reading the temperature	-	-	17.1	μs

1. Guaranteed by characterization results.

2. Guaranteed by design.

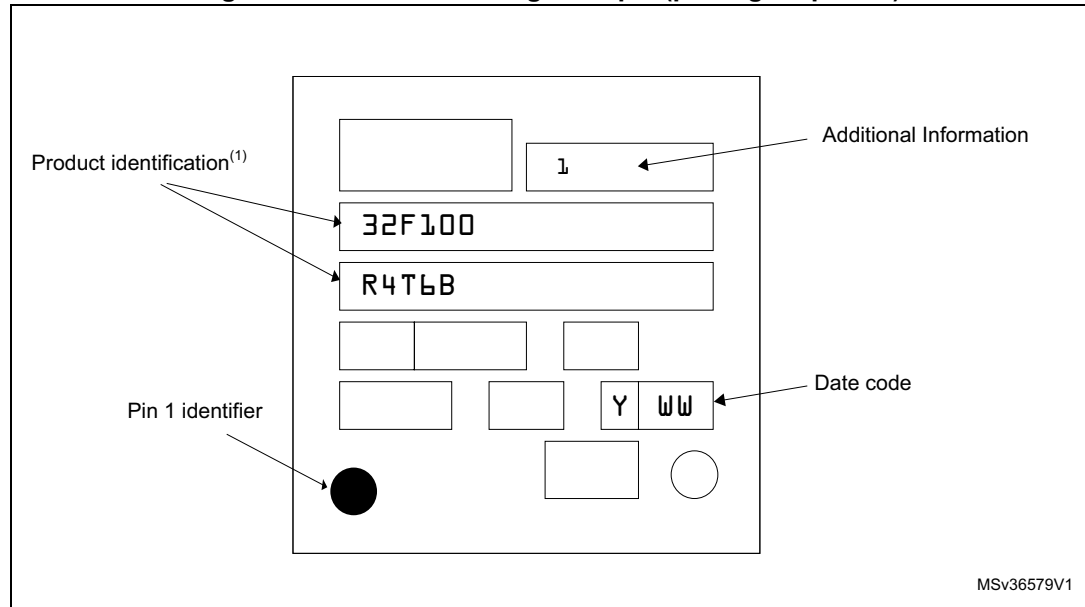
3. Shortest sampling time can be determined in the application by multiple iterations.

Device marking for LQFP64

The following figure gives an example of topside marking and pin 1 position identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 42. LQFP64 marking example (package top view)

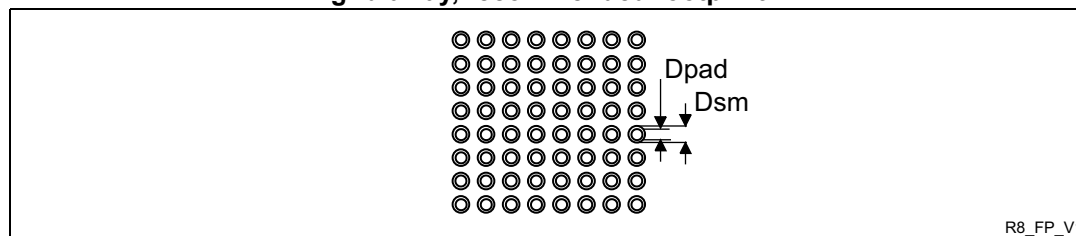


1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 50. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
E1	-	3.500	-	-	0.1378	-
e	-	0.500	-	-	0.0197	-
F	-	0.750	-	-	0.0295	-
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 44. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array, recommended footprint**Table 51. TFBGA64 recommended PCB design rules (0.5 mm pitch BGA)**

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 1.125 mm
Pad trace width	0.100 mm

6.5.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in [Table 54: Ordering information scheme](#).

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F10xxx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example: high-performance application

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax} = 82\text{ }^{\circ}\text{C}$ (measured according to JESD51-2),
 $I_{DDmax} = 50\text{ mA}$, $V_{DD} = 3.5\text{ V}$, maximum 20 I/Os used at the same time in output at low level with $I_{OL} = 8\text{ mA}$, $V_{OL} = 0.4\text{ V}$ and maximum 8 I/Os used at the same time in output mode at low level with $I_{OL} = 20\text{ mA}$, $V_{OL} = 1.3\text{ V}$

$$P_{INTmax} = 50\text{ mA} \times 3.5\text{ V} = 175\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} + 8 \times 20\text{ mA} \times 1.3\text{ V} = 272\text{ mW}$$

$$\text{This gives: } P_{INTmax} = 175\text{ mW and } P_{IOmax} = 272\text{ mW}$$

$$P_{Dmax} = 175 + 272 = 447\text{ mW}$$

$$\text{Thus: } P_{Dmax} = 447\text{ mW}$$

Using the values obtained in [Table 53](#) T_{Jmax} is calculated as follows:

– For LQFP64, $45\text{ }^{\circ}\text{C/W}$

$$T_{Jmax} = 82\text{ }^{\circ}\text{C} + (45\text{ }^{\circ}\text{C/W} \times 447\text{ mW}) = 82\text{ }^{\circ}\text{C} + 20.1\text{ }^{\circ}\text{C} = 102.1\text{ }^{\circ}\text{C}$$

This is within the range of the suffix 6 version parts ($-40 < T_J < 105\text{ }^{\circ}\text{C}$).

In this case, parts must be ordered at least with the temperature range suffix 6 (see [Table 54: Ordering information scheme](#)).

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax} = 115\text{ }^{\circ}\text{C}$ (measured according to JESD51-2),
 $I_{DDmax} = 20\text{ mA}$, $V_{DD} = 3.5\text{ V}$, maximum 20 I/Os used at the same time in output at low level with $I_{OL} = 8\text{ mA}$, $V_{OL} = 0.4\text{ V}$

$$P_{INTmax} = 20\text{ mA} \times 3.5\text{ V} = 70\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} = 64\text{ mW}$$

$$\text{This gives: } P_{INTmax} = 70\text{ mW and } P_{IOmax} = 64\text{ mW:}$$

$$P_{Dmax} = 70 + 64 = 134\text{ mW}$$

$$\text{Thus: } P_{Dmax} = 134\text{ mW}$$