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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f100r8t7btr

List of tables

2.1 Device overview

The description below gives an overview of the complete range of peripherals proposed in this family.

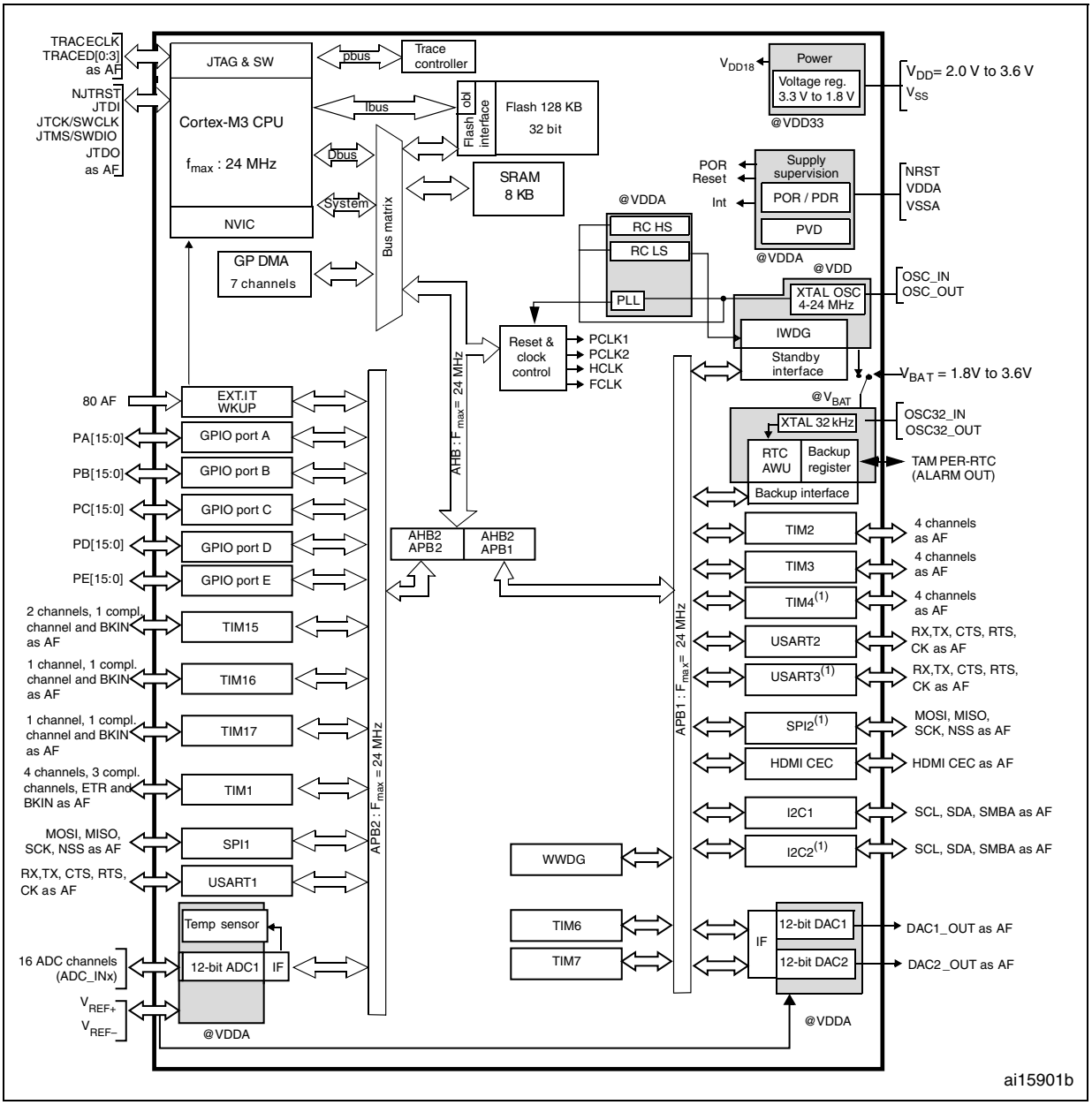
Figure 1 shows the general block diagram of the device family.

Table 2. STM32F100xx features and peripheral counts

Peripheral		STM32F100Cx				STM32F100Rx				STM32F100Vx	
Flash - Kbytes		16	32	64	128	16	32	64	128	64	128
SRAM - Kbytes		4	4	8	8	4	4	8	8	8	8
Timers	Advanced-control	1		1		1		1		1	
	General-purpose	5(1)		6		5(1)		6		6	
Communication interfaces	**SPI**	1(2)		2		1(2)		2		2	
	I^2C	1(3)		2		1(3)		2		2	
	USART	2(4)		3		2(4)		3		3	
	CEC	1									
12-bit synchronized ADC number of channels		1 10 channels				1 16 channels				1 16 channels	
GPIOs		37				51				80	
12-bit DAC Number of channels		2 2									
CPU frequency		24 MHz									
Operating voltage		2.0 to 3.6 V									
Operating temperatures		Ambient operating temperature: –40 to +85 °C /–40 to +105 °C (see *Table 8*) Junction temperature: –40 to +125 °C (see *Table 8*)									
Packages		LQFP48				LQFP64, TFBGA64				LQFP100	

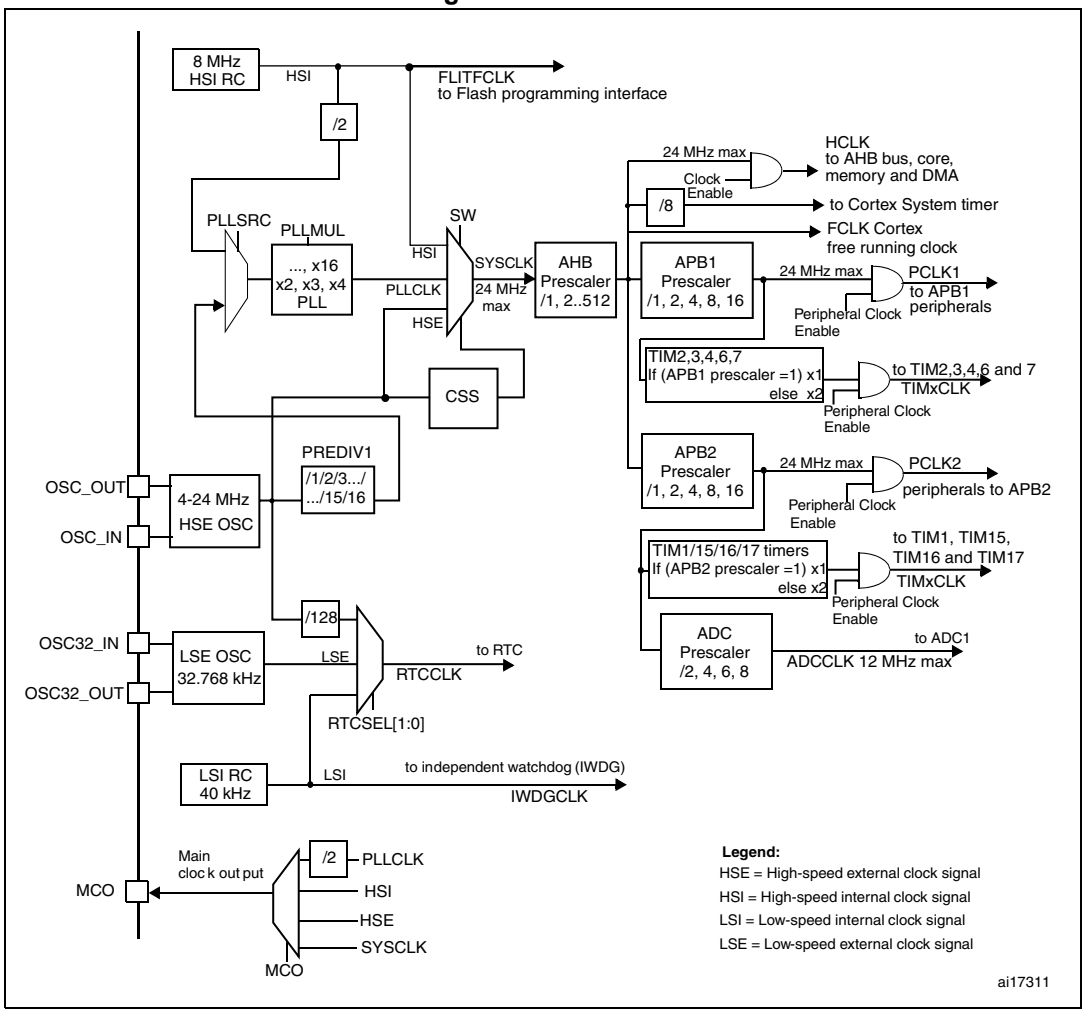
1. TIM4 not present.
2. SPI2 is not present.
3. I2C2 is not present.
4. USART3 is not present.

Figure 1. STM32F100xx value line block diagram



1. Peripherals not present in low-density value line devices.
2. AF = alternate function on I/O port pin.
3. T_A = –40 °C to +85 °C (junction temperature up to 105 °C) or T_A = –40 °C to +105 °C (junction temperature up to 125 °C).

Figure 2. Clock tree



1. To have an ADC conversion time of 1.2 µs, APB2 must be at 24 MHz.

2.2 Overview

2.2.1 ARM® Cortex®-M3 core with embedded Flash and SRAM

The ARM® Cortex®-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex®-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F100xx value line family having an embedded ARM core, is therefore compatible with all ARM tools and software.

2.2.2 Embedded Flash memory

Up to 128 Kbytes of embedded Flash memory is available for storing programs and data.

2.2.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.2.4 Embedded SRAM

Up to 8 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.2.5 Nested vectored interrupt controller (NVIC)

The STM32F100xx value line embeds a nested vectored interrupt controller able to handle up to 41 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.2.6 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 18 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 80 GPIOs can be connected to the 16 external interrupt lines.

2.2.7 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-24 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 24 MHz.

2.2.8 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1. For further details please refer to AN2606.

2.2.9 Power supply schemes

- V_{DD} = 2.0 to 3.6 V: External power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: External analog power supplies for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC or DAC is used).
  V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8 to 3.6 V: Power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

2.2.10 Power supply supervisor

The device has an integrated power on reset (POR)/power down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is

Their counters can be frozen in debug mode.

Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.2.16 I²C bus

The I²C bus interface can operate in multimaster and slave modes. It can support standard and fast modes.

It supports dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.
The interface can be served by DMA and it supports SM Bus 2.0/PM Bus.

2.2.17 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F100xx value line embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

The available USART interfaces communicate at up to 3 Mbit/s. They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode and have LIN Master/Slave capability.

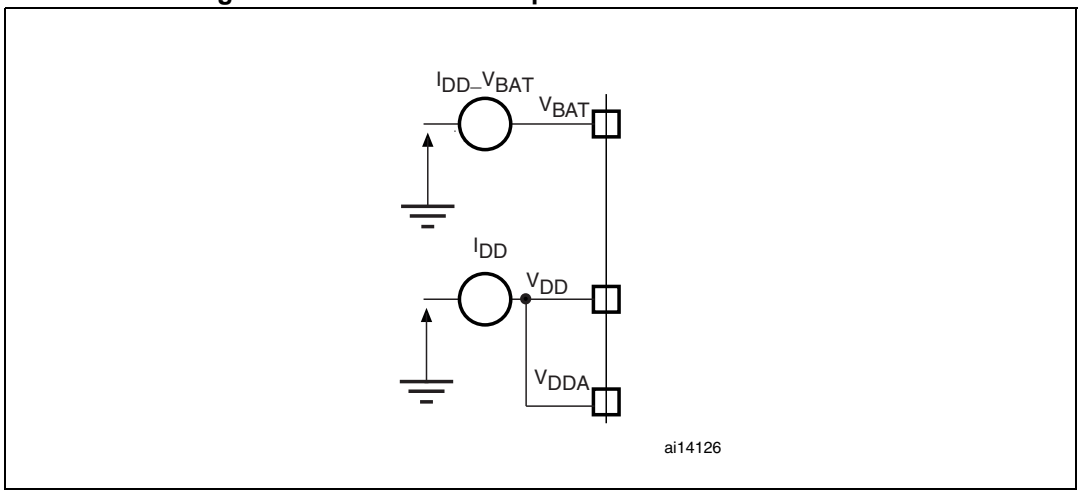
The USART interfaces can be served by the DMA controller.

Table 4. Low & medium-density STM32F100xx pin definitions (continued)

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3)(4)	
LQFP100	LQFP64	TFBGA64	LQFP48					Default	Remap
9	4	B1	4	PC15-OSC32_OUT(5)	I/O	-	PC15(6)	OSC32_OUT	-
10	-	-	-	V_{SS_5}	S	-	V_{SS_5}	-	-
11	-	-	-	V_{DD_5}	S	-	V_{DD_5}	-	-
12	5	C1	5	OSC_IN	I	-	OSC_IN	-	PD0(7)
13	6	D1	6	OSC_OUT	O	-	OSC_OUT	-	PD1(7)
14	7	E1	7	NRST	I/O	-	NRST	-	-
15	8	E3	-	PC0	I/O	-	PC0	ADC1_IN10	-
16	9	E2	-	PC1	I/O	-	PC1	ADC1_IN11	-
17	10	F2	-	PC2	I/O	-	PC2	ADC1_IN12	-
18	11	-(8)	-	PC3	I/O	-	PC3	ADC1_IN13	-
19	12	F1	8	V_{SSA}	S	-	V_{SSA}	-	-
20	-	-	-	V_{REF-}	S	-	V_{REF-}	-	-
21	-	G1	-	V_{REF+}	S	-	V_{REF+}	-	-
22	13	H1	9	V_{DDA}	S	-	V_{DDA}	-	-
23	14	G2	10	PA0-WKUP	I/O	-	PA0	WKUP / USART2_CTS(12)/ ADC1_IN0 / TIM2_CH1_ETR(12)	-
24	15	H2	11	PA1	I/O	-	PA1	USART2_RTS(12)/ ADC1_IN1 / TIM2_CH2(12)	-
25	16	F3	12	PA2	I/O	-	PA2	USART2_TX(12)/ ADC1_IN2 / TIM2_CH3(12)/ TIM15_CH1(12)	-
26	17	G3	13	PA3	I/O	-	PA3	USART2_RX(12)/ ADC1_IN3 / TIM2_CH4(12) / TIM15_CH2(12)	-
27	18	C2	-	V_{SS_4}	S	-	V_{SS_4}	-	-
28	19	D2	-	V_{DD_4}	S	-	V_{DD_4}	-	-
29	20	H3	14	PA4	I/O	-	PA4	SPI1_NSS(12)/ADC1_IN4 USART2_CK(12) / DAC1_OUT	-
30	21	F4	15	PA5	I/O	-	PA5	SPI1_SCK(12)/ADC1_IN5 / DAC2_OUT	-
31	22	G4	16	PA6	I/O	-	PA6	SPI1_MISO(12)/ADC1_IN6 / TIM3_CH1(12)	TIM1_BKIN / TIM16_CH1
32	23	H4	17	PA7	I/O	-	PA7	SPI1_MOSI(12)/ADC1_IN7 / TIM3_CH2(12)	TIM1_CH1N / TIM17_CH1

5.1.7 Current consumption measurement

Figure 11. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 5: Voltage characteristics*, *Table 6: Current characteristics*, and *Table 7: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD} –V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}(2)	Input voltage on five volt tolerant pin	V_{SS} –0.3	V_{DD} +4.0	
	Input voltage on any other pin	V_{SS} –0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 5.3.11: Absolute maximum ratings (electrical sensitivity)*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 6: Current characteristics* for the maximum allowed injected current values.

5.3.4 Embedded reference voltage

The parameters given in *Table 11* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 11. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.16	1.20	1.26	V
		–40 °C < T_A < +85 °C	1.16	1.20	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	-	5.1	17.1(2)	µs
V_{RERINT}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3 V ±10 mV	-	-	10	mV
T_{Coeff}(2)	Temperature coefficient	-	-	-	100	ppm/°C

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 11: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if it is explicitly mentioned
- Prefetch in on (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}$

The parameters given in *Table 12* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Figure 12. Maximum current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled

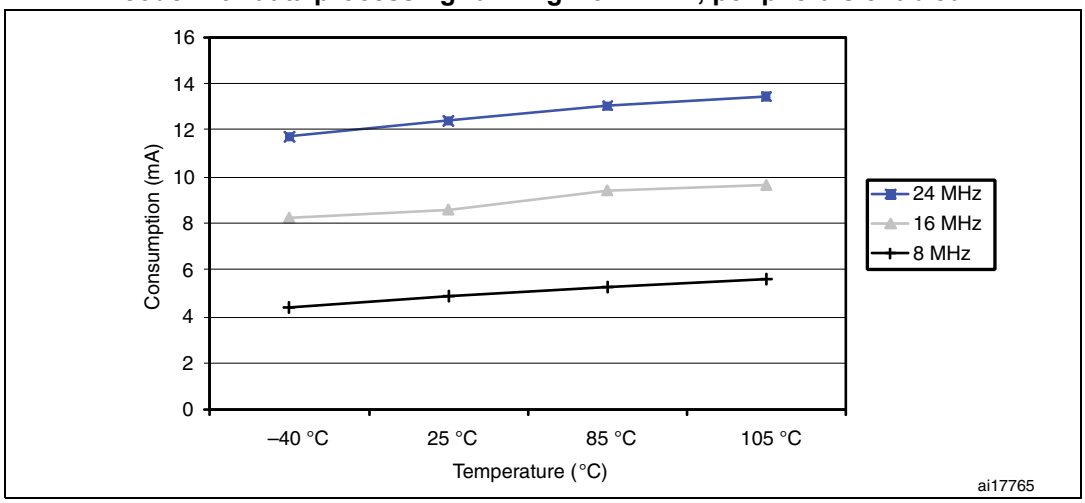


Figure 13. Maximum current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled

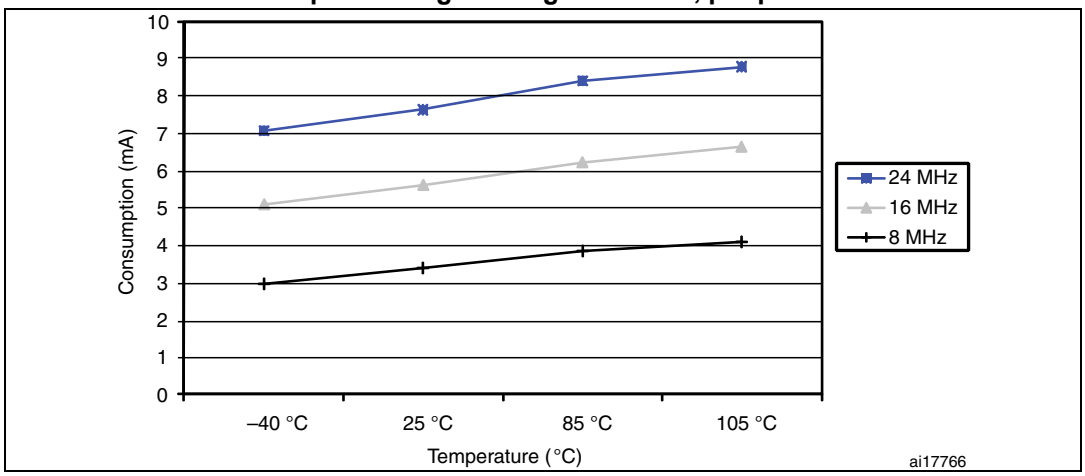


Table 14. Maximum current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	External clock(2) all peripherals enabled	24 MHz	9.6	10	mA
			16 MHz	7.1	7.5	
			8 MHz	4.5	4.8	
		External clock(2), all peripherals disabled	24 MHz	3.8	4	
			16 MHz	3.3	3.5	
			8 MHz	2.7	3	

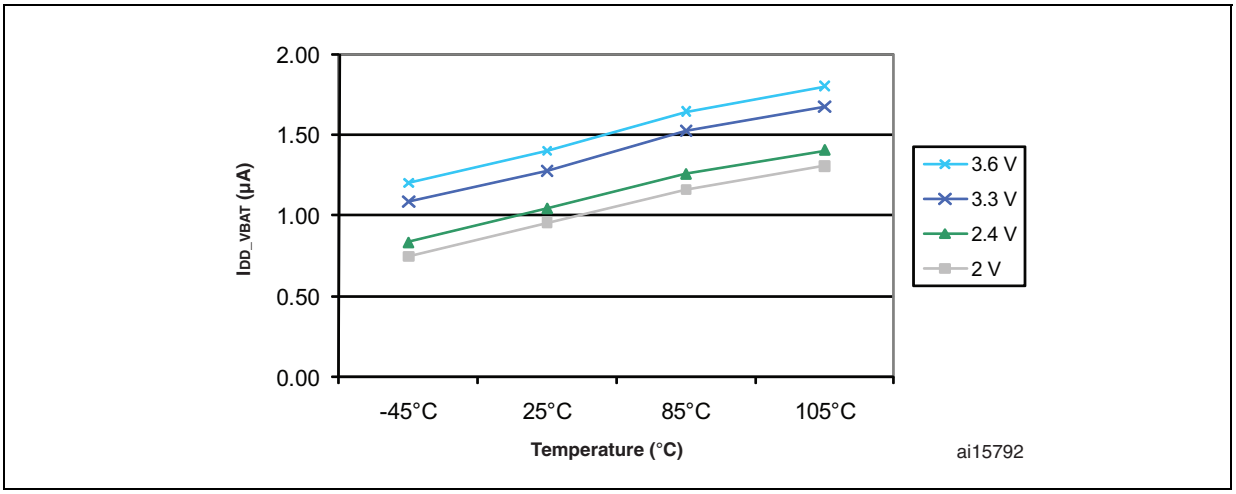
1. Guaranteed by characterization, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 15. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)			Max		Unit
			V_{DD}/ V_{BAT} = 2.0 V	V_{DD}/ V_{BAT} = 2.4 V	V_{DD}/ V_{BAT} = 3.3 V	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in Run mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	23.5	24	190	350	µA
		Regulator in Low-Power mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	13.5	14	170	330	
	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog ON	-	2.6	3.4	-	-	
		Low-speed internal RC oscillator ON, independent watchdog OFF	-	2.4	3.2	-	-	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	-	1.7	2	4	5	
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	0.9	1.1	1.4	1.9	2.2	

1. Typical values are measured at T_A = 25 °C.

Figure 14. Typical current consumption on V_{BAT} with RTC on vs. temperature at different V_{BAT} values



Low-speed external user clock generated from an external source

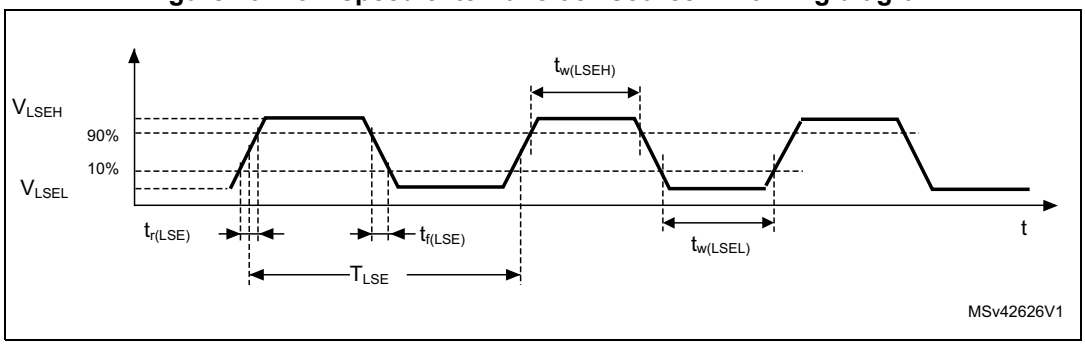
The characteristics given in *Table 20* result from tests performed using an low-speed external clock source, and under the ambient temperature and supply voltage conditions summarized in *Table 8*.

Table 20. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage(1)		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage(1)		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)		-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle(1)		30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

Figure 19. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 21*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Low-speed internal (LSI) RC oscillator

Table 24. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	60	kHz
$\Delta f_{LSI(T)}$	Temperature-related frequency drift(2)	-9	-	9	%
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.65	1.2	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C °C unless otherwise specified.
2. Guaranteed by characterization results.
3. Guaranteed by design.

Wakeup time from low-power mode

The wakeup times given in *Table 25* are measured on a wakeup phase with an 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

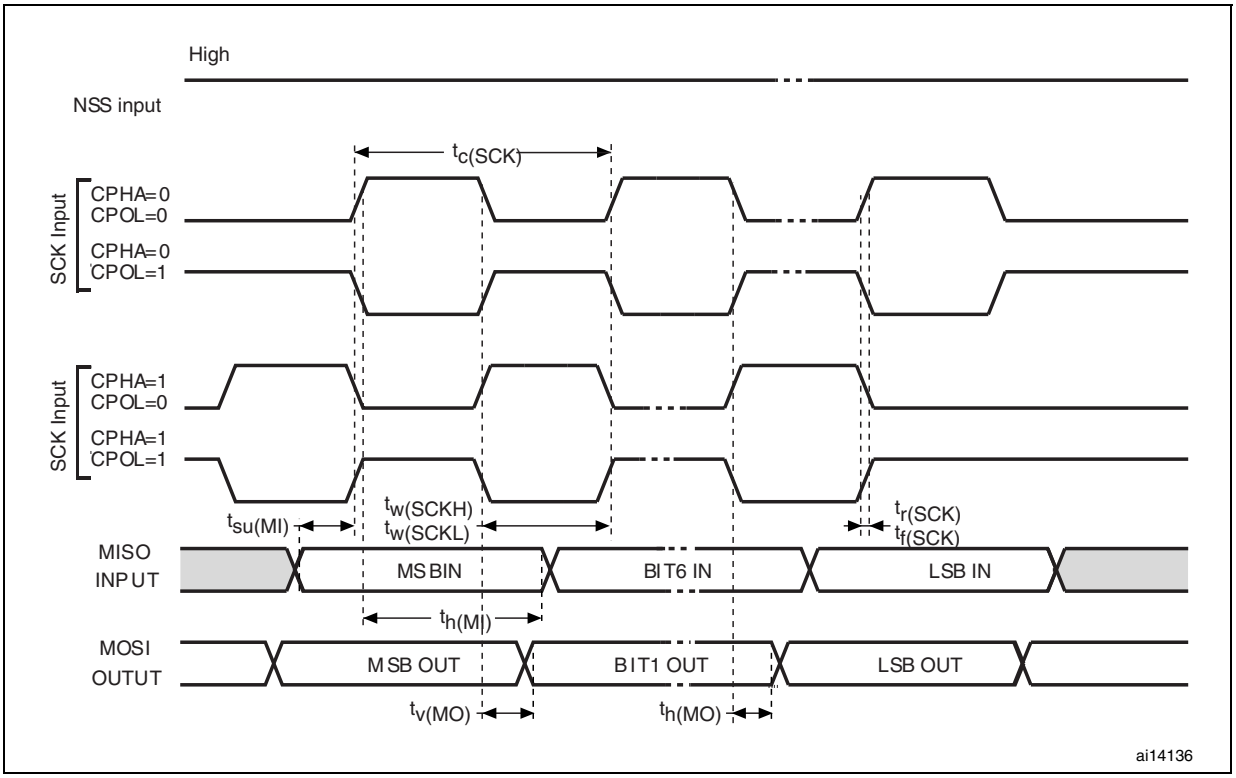
All timings are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 25. Low-power mode wakeup timings

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	1.8	µs
t_{WUSTOP}(1)	Wakeup from Stop mode (regulator in run mode)	3.6	µs
	Wakeup from Stop mode (regulator in low-power mode)	5.4	
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	50	µs

1. The wakeup times are measured from the wakeup event to the point at which the user application code reads the first instruction.

Figure 31. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

HDMI consumer electronics control (CEC)

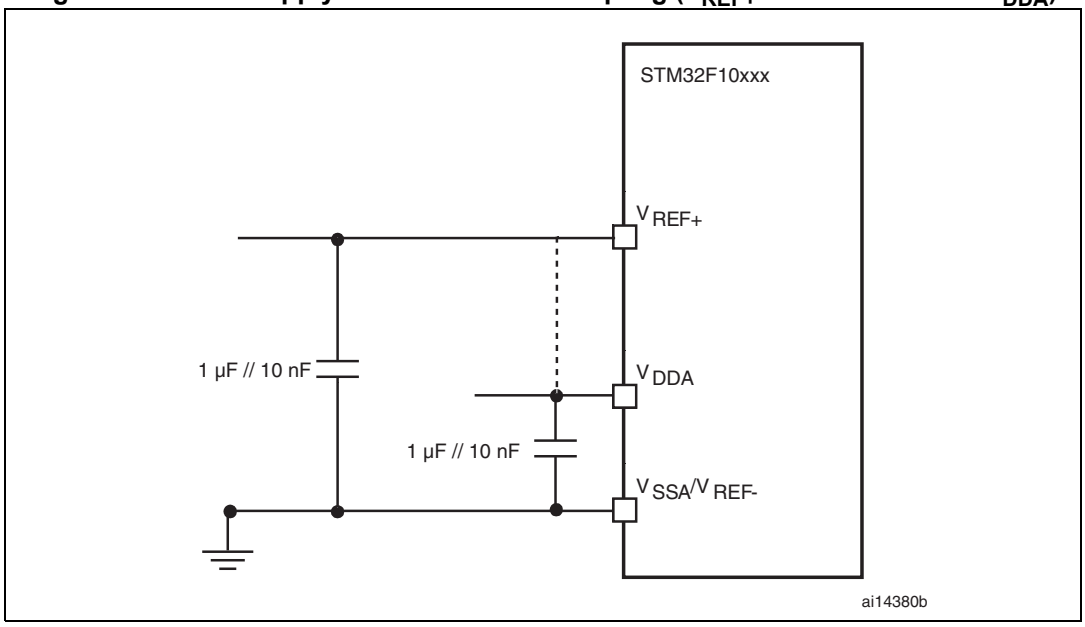
Refer to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics.

5.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 42* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 8*.

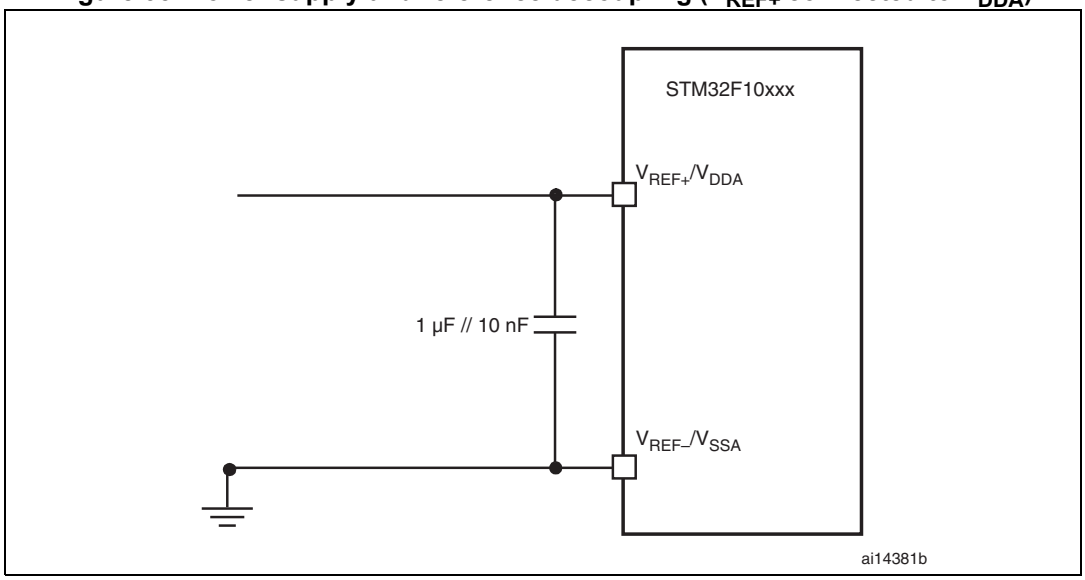
Note: It is recommended to perform a calibration after each power-up.

Figure 34. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} is available on 100-pin packages and on TFBGA64 packages. V_{REF-} is available on 100-pin packages only.

Figure 35. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



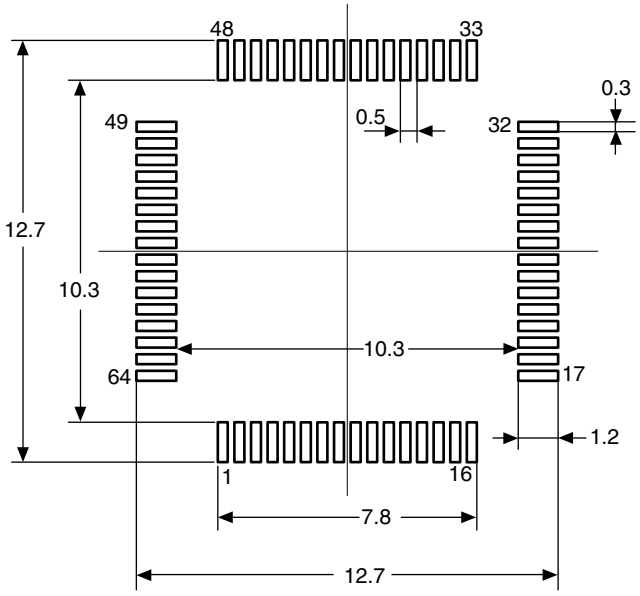
1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

Table 49. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 41.LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint



1. Dimensions are in millimeters.

Table 50. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	-	3.500	-	-	0.1378	-
e	-	0.500	-	-	0.0197	-
F	-	0.750	-	-	0.0295	-
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 44. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array, recommended footprint

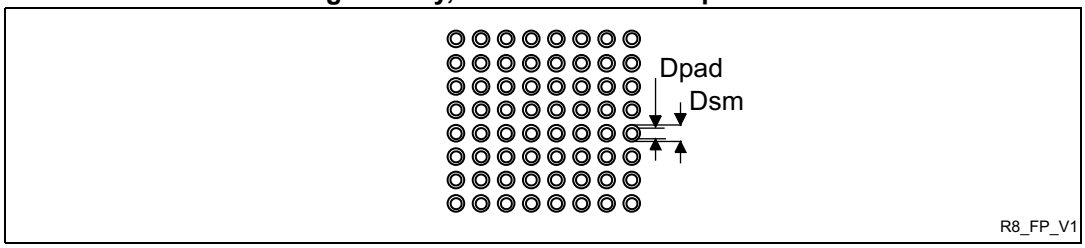
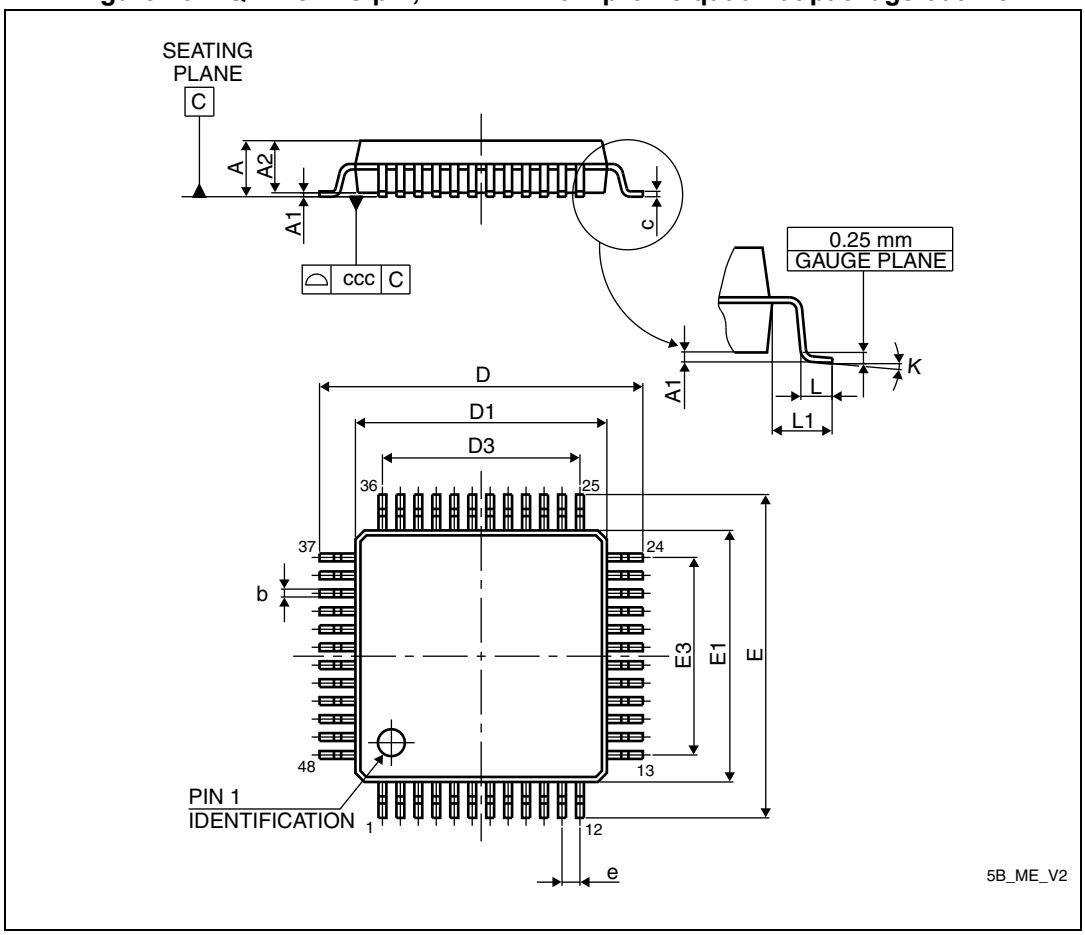


Table 51. TFBGA64 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 1.125 mm
Pad trace width	0.100 mm

6.4 LQFP48 package information

Figure 46. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 52. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622

8 Revision history

Table 55. Document revision history

Date	Revision	Changes
12-Oct-2009	1	Initial release.
26-Feb-2010	2	TFBGA64 package added (see *Table 50* and *Table 41*). *Note 5* modified in *Table 4: Low & medium-density STM32F100xx pin definitions*. $I_{INJ(PIN)}$ modified in *Table 6: Current characteristics*. Conditions removed from *Table 25: Low-power mode wakeup timings*. Notes modified in *Table 34: I/O static characteristics*. *Figure 27: Recommended NRST pin protection* modified. Note modified in *Table 39: I2C characteristics*. *Figure 28: I2C bus AC waveforms and measurement circuit(1)* modified. *Table 46: DAC characteristics* modified. *Figure 36: 12-bit buffered /non-buffered DAC* added. *TIM2, TIM3, TIM4* and *TIM15, TIM16 and TIM17* updated. HDMI-CEC electrical characteristics added. Values added to: – *Table 12: Maximum current consumption in Run mode, code with data processing running from Flash* – *Table 13: Maximum current consumption in Run mode, code with data processing running from RAM* – *Table 14: Maximum current consumption in Sleep mode, code running from Flash or RAM* – *Table 15: Typical and maximum current consumptions in Stop and Standby modes* – *Table 18: Peripheral current consumption* – *Table 29: EMS characteristics* – *Table 30: EMI characteristics* – *Table 47: TS characteristics* *Section 5.3.12: I/O current injection characteristics* modified. Added figures: – *Figure 12: Maximum current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled* – *Figure 13: Maximum current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled* – *Figure 15: Typical current consumption in Stop mode with regulator in Run mode versus temperature at VDD = 3.3 V and 3.6 V* – *Figure 16: Typical current consumption in Stop mode with regulator in Low-power mode versus temperature at VDD = 3.3 V and 3.6 V* – *Figure 17: Typical current consumption in Standby mode versus temperature at VDD = 3.3 V and 3.6 V*