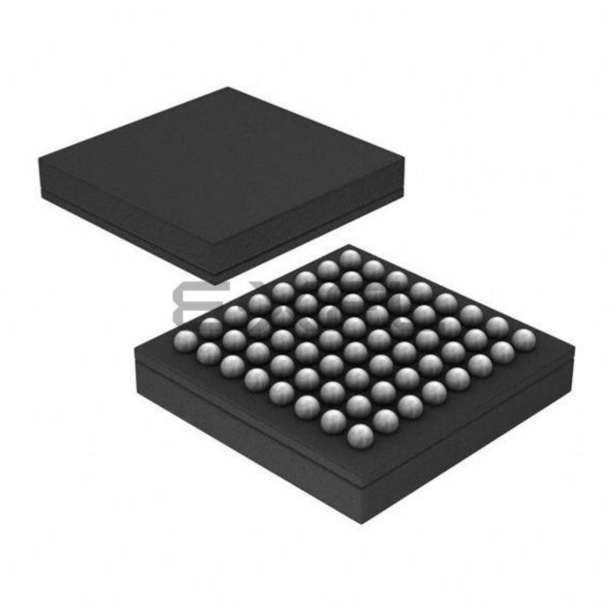
# STMicroelectronics - STM32F100RBH6BTR Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 24MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT |
| Number of I/O | 51 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 16x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-TFBGA |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f100rbh6btr |

# List of figures

## 2.1 Device overview

The description below gives an overview of the complete range of peripherals proposed in this family.

*Figure 1* shows the general block diagram of the device family.

Table 2. STM32F100xx features and peripheral counts

| **Peripheral** | | **STM32F100Cx** | | | | **STM32F100Rx** | | | | **STM32F100Vx** | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Flash - Kbytes** | | 16 | 32 | 64 | 128 | 16 | 32 | 64 | 128 | 64 | 128 |
| **SRAM - Kbytes** | | 4 | 4 | 8 | 8 | 4 | 4 | 8 | 8 | 8 | 8 |
| **Timers** | Advanced-control | 1 | | 1 | | 1 | | 1 | | 1 | |
| | **General-purpose** | 5(1) | | 6 | | 5(1) | | 6 | | 6 | |
| **Communication interfaces** | **SPI** | 1(2) | | 2 | | 1(2) | | 2 | | 2 | |
| | **I$^2$C** | 1(3) | | 2 | | 1(3) | | 2 | | 2 | |
| | **USART** | 2(4) | | 3 | | 2(4) | | 3 | | 3 | |
| | **CEC** | 1 | | | | | | | | | |
| **12-bit synchronized ADC<br>number of channels** | | 1<br>10 channels | | | | 1<br>16 channels | | | | 1<br>16 channels | |
| **GPIOs** | | 37 | | | | 51 | | | | 80 | |
| **12-bit DAC<br>Number of channels** | | 2<br>2 | | | | | | | | | |
| **CPU frequency** | | 24 MHz | | | | | | | | | |
| **Operating voltage** | | 2.0 to 3.6 V | | | | | | | | | |
| **Operating temperatures** | | Ambient operating temperature: –40 to +85 °C /–40 to +105 °C (see *Table 8*)<br>Junction temperature: –40 to +125 °C (see *Table 8*) | | | | | | | | | |
| **Packages** | | LQFP48 | | | | LQFP64, TFBGA64 | | | | LQFP100 | |

1. TIM4 not present.
2. SPI2 is not present.
3. I2C2 is not present.
4. USART3 is not present.

## 2.2 Overview

### 2.2.1 ARM® Cortex®-M3 core with embedded Flash and SRAM

The ARM® Cortex®-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex®-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F100xx value line family having an embedded ARM core, is therefore compatible with all ARM tools and software.

### 2.2.2 Embedded Flash memory

Up to 128 Kbytes of embedded Flash memory is available for storing programs and data.

### 2.2.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

### 2.2.4 Embedded SRAM

Up to 8 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

### 2.2.5 Nested vectored interrupt controller (NVIC)

The STM32F100xx value line embeds a nested vectored interrupt controller able to handle up to 41 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

Their counters can be frozen in debug mode.

### Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

### Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

### Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

### SysTick timer

This timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

## 2.2.16 I²C bus

The I²C bus interface can operate in multimaster and slave modes. It can support standard and fast modes.

It supports dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode.
A hardware CRC generation/verification is embedded.
The interface can be served by DMA and it supports SM Bus 2.0/PM Bus.

## 2.2.17 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F100xx value line embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

The available USART interfaces communicate at up to 3 Mbit/s. They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode and have LIN Master/Slave capability.

The USART interfaces can be served by the DMA controller.

Figure 4. STM32F100xx value line LQFP64 pinout

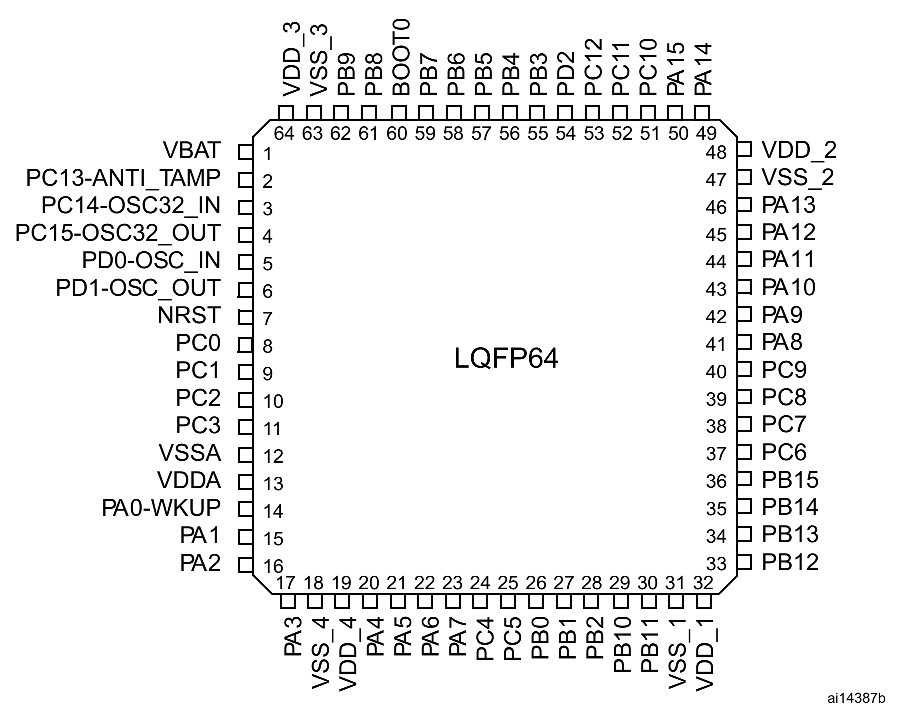


Figure 5. STM32F100xx value line LQFP48 pinout

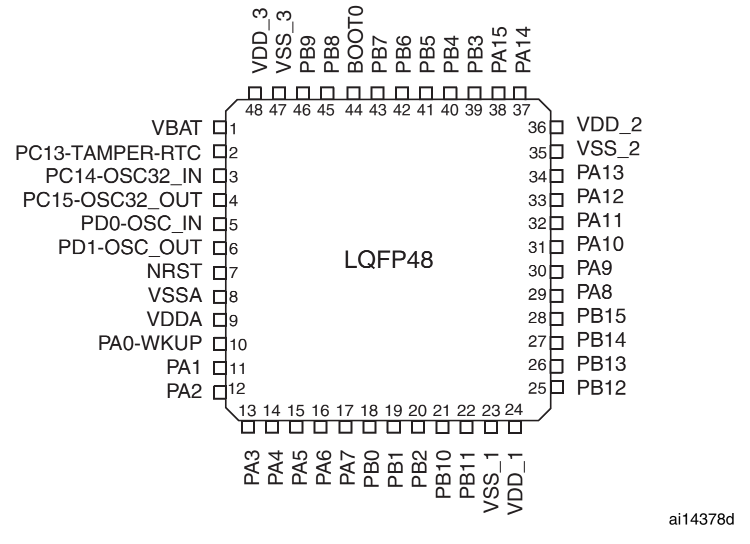
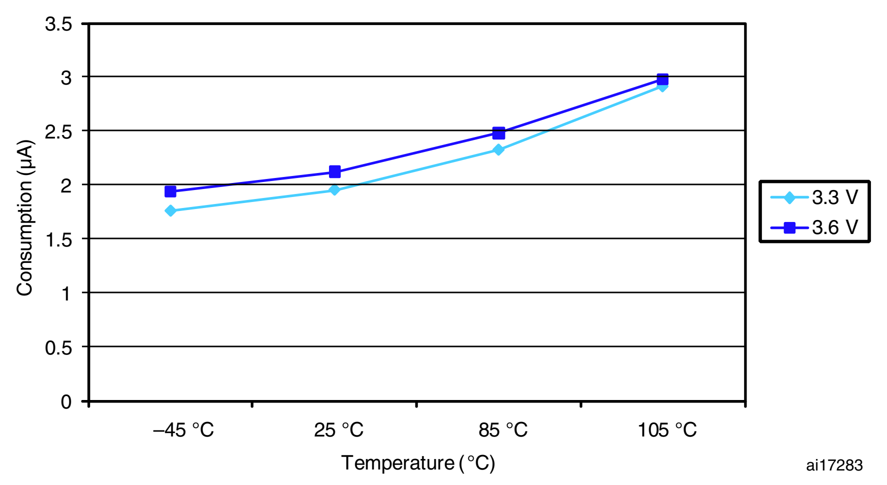


Figure 17. Typical current consumption in Standby mode versus temperature at $V_{DD}$ = 3.3 V and 3.6 V



### Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)
- All peripherals are disabled except if it is explicitly mentioned
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK2} = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$

The parameters given in *Table 16* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 8*.

### Table 17. Typical current consumption in Sleep mode, code running from Flash or RAM

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typical values[1] |  | Unit |
|---|---|---|---|---|---|---|
|  |  |  |  | All peripherals enabled[2] | All peripherals disabled |  |
| $I_{DD}$ | Supply current in Sleep mode | Running on high-speed external clock with an 8 MHz crystal[3] | 24 MHz | 7.3 | 2.6 | mA |
|  |  |  | 16 MHz | 5.2 | 2 |  |
|  |  |  | 8 MHz | 2.8 | 1.3 |  |
|  |  |  | 4 MHz | 2 | 1.1 |  |
|  |  |  | 2 MHz | 1.5 | 1.1 |  |
|  |  |  | 1 MHz | 1.25 | 1 |  |
|  |  |  | 500 kHz | 1.1 | 1 |  |
|  |  |  | 125 kHz | 1.05 | 0.95 |  |
|  |  | Running on high-speed internal RC (HSI) | 24 MHz | 6.65 | 1.9 |  |
|  |  |  | 16 MHz | 4.5 | 1.4 |  |
|  |  |  | 8 MHz | 2.2 | 0.7 |  |
|  |  |  | 4 MHz | 1.35 | 0.55 |  |
|  |  |  | 2 MHz | 0.85 | 0.45 |  |
|  |  |  | 1 MHz | 0.6 | 0.41 |  |
|  |  |  | 500 kHz | 0.5 | 0.39 |  |
|  |  |  | 125 kHz | 0.4 | 0.37 |  |

1. Typical values are measures at $T_A$ = 25 °C, $V_{DD}$ = 3.3 V.
2. Add an additional power consumption of 0.8 mA for the ADC and of 0.5 mA for the DAC analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. An 8 MHz crystal is used as the external clock source. The AHB prescaler is used to reduce the frequency when $f_{HCLK}$ > 8 MHz, the PLL is used when $f_{HCLK}$ > 8 MHz.

## On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 18*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and $V_{DD}$ supply voltage conditions summarized in *Table 5*.

**Table 18. Peripheral current consumption(1)**

| Peripheral | | Current consumption (µA/MHz) |
|---|---|---|
| AHB (up to 24MHz) | DMA1 | 22.92 |
| | CRC | 2,08 |
| | BusMatrix(2) | 4,17 |
| APB1 (up to 24MHz) | APB1-Bridge | 2,92 |
| | TIM2 | 18,75 |
| | TIM3 | 17,92 |
| | TIM4 | 18,33 |
| | TIM6 | 5,00 |
| | TIM7 | 5,42 |
| | SPI2/I2S2 | 4,17 |
| | USART2 | 12,08 |
| | USART3 | 12,92 |
| | I2C1 | 10,83 |
| | I2C2 | 10,83 |
| | CEC | 5,83 |
| | DAC(3) | 8,33 |
| | WWDG | 2,50 |
| | PWR | 2,50 |
| | BKP | 3,33 |
| | IWDG | 7,50 |
| APB2 (up to 24MHz) | APB2-Bridge | 3.75 |
| | GPIOA | 6,67 |
| | GPIOB | 6,25 |
| | GPIOC | 7,08 |
| | GPIOD | 6,67 |
| | GPIOE | 6,25 |
| | SPI1 | 4,17 |
| | USART1 | 11,67 |
| | TIM1 | 22,92 |
| | TIM15 | 14,58 |
| | TIM16 | 11,67 |
| | TIM17 | 10.83 |
| | ADC1(4) | 15.83 |

1. $f_{HCLK}$ = 24 MHz, $f_{APB1}$ = $f_{HCLK}$, fAPB2 = $f_{HCLK}$, default prescaler value for each peripheral.
2. The BusMatrix is automatically active when at least one master is ON.
3. When DAC_OUT1 or DAC_OU2 is enabled a current consumption equal to 0,5 mA must be added
4. Specific conditions for ADC: $f_{HCLK}$ = 24 MHz, $f_{APB1}$ = $f_{HCLK}$, $f_{APB2}$ = $f_{HCLK}$, $f_{ADCCLK}$ = $f_{APB2}$/2. When ADON bit in the ADC_CR2 register is set to 1, a current consumption equal to 0, 1mA must be added.

### Low-speed external user clock generated from an external source

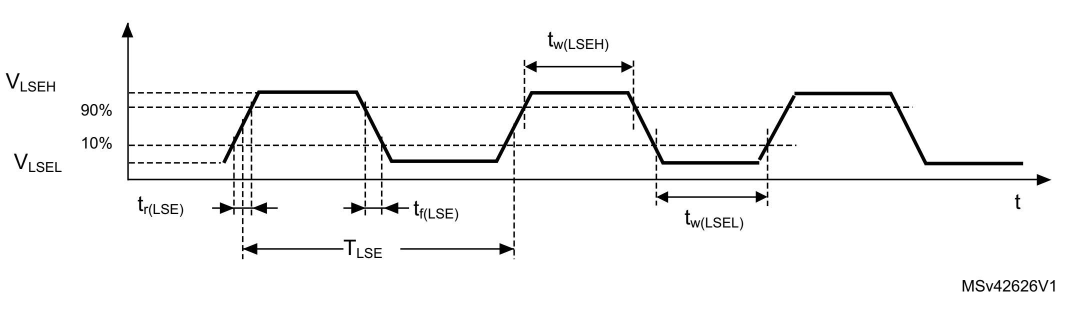
The characteristics given in *Table 20* result from tests performed using an low-speed external clock source, and under the ambient temperature and supply voltage conditions summarized in *Table 8*.

**Table 20. Low-speed external user clock characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSE\_ext}$ | User external clock source frequency(1) | - | - | 32.768 | 1000 | kHz |
| $V_{LSEH}$ | OSC32_IN input pin high level voltage(1) | | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| $V_{LSEL}$ | OSC32_IN input pin low level voltage(1) | | $V_{SS}$ | - | $0.3V_{DD}$ | |
| $t_{w(LSEH)}$<br>$t_{w(LSEL)}$ | OSC32_IN high or low time(1) | | 450 | - | - | ns |
| $t_{r(LSE)}$<br>$t_{f(LSE)}$ | OSC32_IN rise or fall time(1) | | - | - | 50 | |
| $C_{in(LSE)}$ | OSC32_IN input capacitance(1) | | - | 5 | - | pF |
| $DuCy_{(LSE)}$ | Duty cycle(1) | | 30 | - | 70 | % |
| $I_L$ | OSC32_IN Input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | - | - | ±1 | µA |

1. Guaranteed by design.

**Figure 19. Low-speed external clock source AC timing diagram**



### High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 21*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Figure 24. 5 V tolerant I/O input characteristics - CMOS port

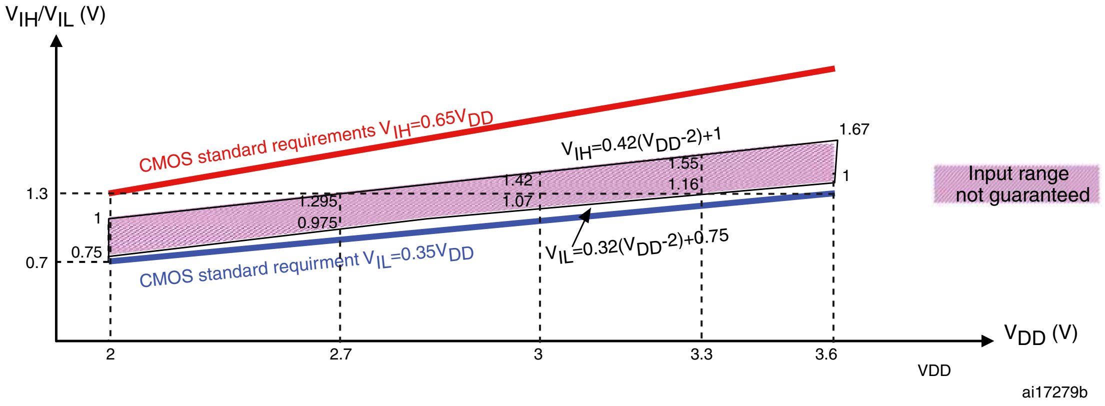
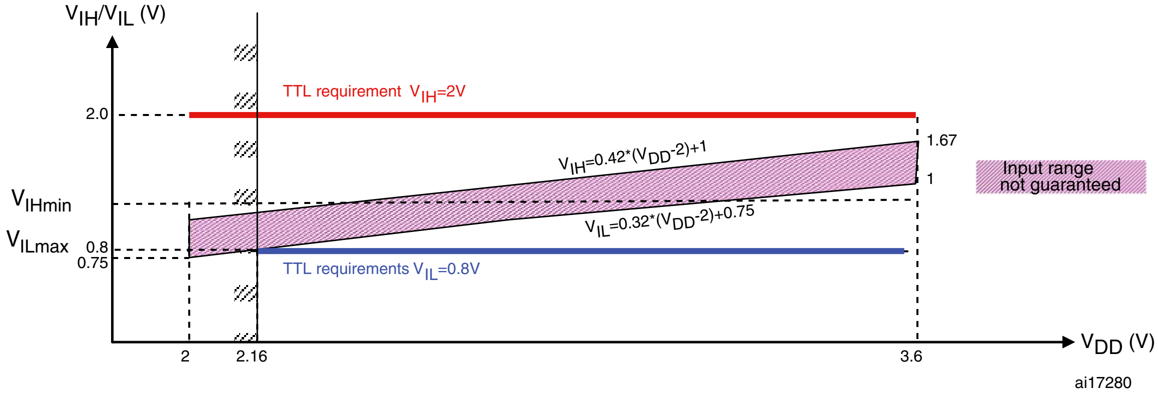


Figure 25. 5 V tolerant I/O input characteristics - TTL port



## Output driving current

The GPIOs (general-purpose inputs/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed $V_{OL}/V_{OH}$).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $I_{VDD}$ (see *Table 6*).
- The sum of the currents sunk by all the I/Os on $V_{SS}$ plus the maximum Run consumption of the MCU sunk on $V_{SS}$ cannot exceed the absolute maximum rating $I_{VSS}$ (see *Table 6*).

### Output voltage levels

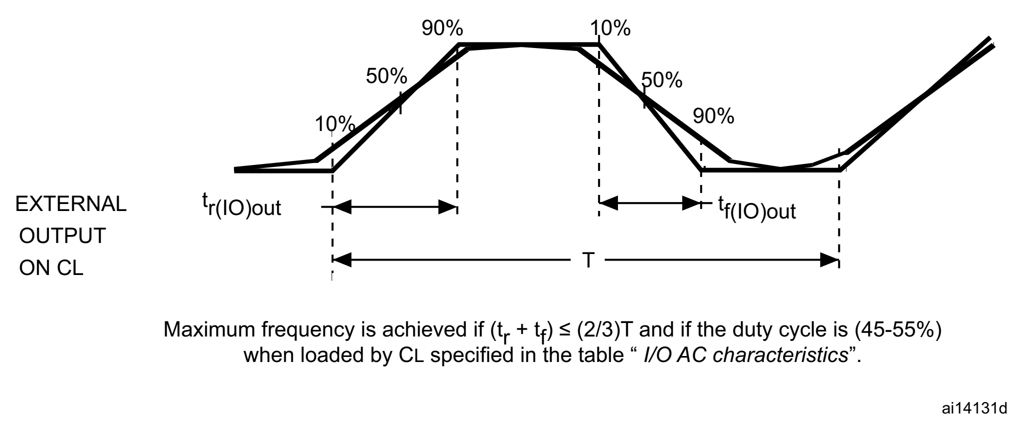
Unless otherwise specified, the parameters given in *Table 35* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 8*. All I/Os are CMOS and TTL compliant.

**Table 35. Output voltage characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$(1) | Output Low level voltage for an I/O pin when 8 pins are sunk at the same time | CMOS port(2)<br>$I_{IO}$ = +8 mA,<br>2.7 V < $V_{DD}$ < 3.6 V | - | 0.4 | V |
| $V_{OH}$(3) | Output High level voltage for an I/O pin when 8 pins are sourced at the same time | | $V_{DD}$–0.4 | - | |
| $V_{OL}$(1) | Output low level voltage for an I/O pin when 8 pins are sunk at the same time | TTL port(2)<br>$I_{IO}$ = +8 mA<br>2.7 V < $V_{DD}$ < 3.6 V | - | 0.4 | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin when 8 pins are sourced at the same time | | 2.4 | - | |
| $V_{OL}$(1) | Output low level voltage for an I/O pin when 8 pins are sunk at the same time | $I_{IO}$ = +20 mA(4)<br>2.7 V < $V_{DD}$ < 3.6 V | - | 1.3 | V |
| $V_{OH}$ (3) | Output high level voltage for an I/O pin when 8 pins are sourced at the same time | | $V_{DD}$–1.3 | - | |
| $V_{OL}$(1) | Output low level voltage for an I/O pin when 8 pins are sunk at the same time | $I_{IO}$ = +6 mA(4)<br>2 V < $V_{DD}$ < 2.7 V | - | 0.4 | V |
| $V_{OH}$(3) | Output high level voltage for an I/O pin when 8 pins are sourced at the same time | | $V_{DD}$–0.4 | - | |

1. The $I_{IO}$ current sunk by the device must always respect the absolute maximum rating specified in *Table 6* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The $I_{IO}$ current sourced by the device must always respect the absolute maximum rating specified in *Table 6* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VDD}$.
4. Based on characterization data, not tested in production.

Figure 26. I/O AC characteristics definition



## 5.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, $R_{PU}$ (see *Table 34*).

Unless otherwise specified, the parameters given in *Table 37* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 8*.

Table 37. NRST pin characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$(1) | NRST Input low level voltage | - | –0.5 | - | 0.8 | V |
| $V_{IH(NRST)}$(1) | NRST Input high level voltage | - | 2 | - | $V_{DD}$+0.5 | |
| $V_{hys(NRST)}$ | NRST Schmitt trigger voltage hysteresis | - | - | 200 | - | mV |
| $R_{PU}$ | Weak pull-up equivalent resistor(2) | $V_{IN} = V_{SS}$ | 30 | 40 | 50 | kΩ |
| $V_{F(NRST)}$(1) | NRST Input filtered pulse | - | - | - | 100 | ns |
| $V_{NF(NRST)}$(1) | NRST Input not filtered pulse | - | 300 | - | - | ns |

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Table 42. ADC characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Power supply | - | 2.4 | - | 3.6 | V |
| $V_{REF+}$ | Positive reference voltage | - | 2.4 | - | $V_{DDA}$ | V |
| $I_{VREF}$ | Current on the $V_{REF}$ input pin | - | - | 160(1) | 220(1) | µA |
| $f_{ADC}$ | ADC clock frequency | - | 0.6 | - | 12 | MHz |
| $f_S$(2) | Sampling rate | - | 0.05 | - | 1 | MHz |
| $f_{TRIG}$(2) | External trigger frequency | $f_{ADC}$ = 12 MHz | - | - | 705 | kHz |
| | | - | - | - | 17 | 1/$f_{ADC}$ |
| $V_{AIN}$(3) | Conversion voltage range | - | 0 ($V_{SSA}$ tied to ground) | - | $V_{REF+}$ | V |
| $R_{AIN}$(2) | External input impedance | See *Equation 1* and *Table 43* for details | - | - | 50 | kΩ |
| $R_{ADC}$(2) | Sampling switch resistance | - | - | - | 1 | kΩ |
| $C_{ADC}$(2) | Internal sample and hold capacitor | - | - | - | 8 | pF |
| $t_{CAL}$(2) | Calibration time | $f_{ADC}$ = 12 MHz | 6.9 | | | µs |
| | | - | 83 | | | 1/$f_{ADC}$ |
| $t_{lat}$(2) | Injection trigger conversion latency | $f_{ADC}$ = 12 MHz | - | - | 0.25 | µs |
| | | - | - | - | 3(4) | 1/$f_{ADC}$ |
| $t_{latr}$(2) | Regular trigger conversion latency | $f_{ADC}$ = 12 MHz | - | - | 0.166 | µs |
| | | - | - | - | 2(4) | 1/$f_{ADC}$ |
| $t_S$(2) | Sampling time | $f_{ADC}$ = 12 MHz | 0.125 | - | 20.0 | µs |
| | | | 1.5 | - | 239.5 | 1/$f_{ADC}$ |
| $t_{STAB}$(2) | Power-up time | - | 0 | 0 | 1 | µs |
| $t_{CONV}$(2) | Total conversion time (including sampling time) | $f_{ADC}$ = 12 MHz | 1.17 | - | 21 | µs |
| | | - | 14 to 252 ($t_S$ for sampling +12.5 for successive approximation) | | | 1/$f_{ADC}$ |

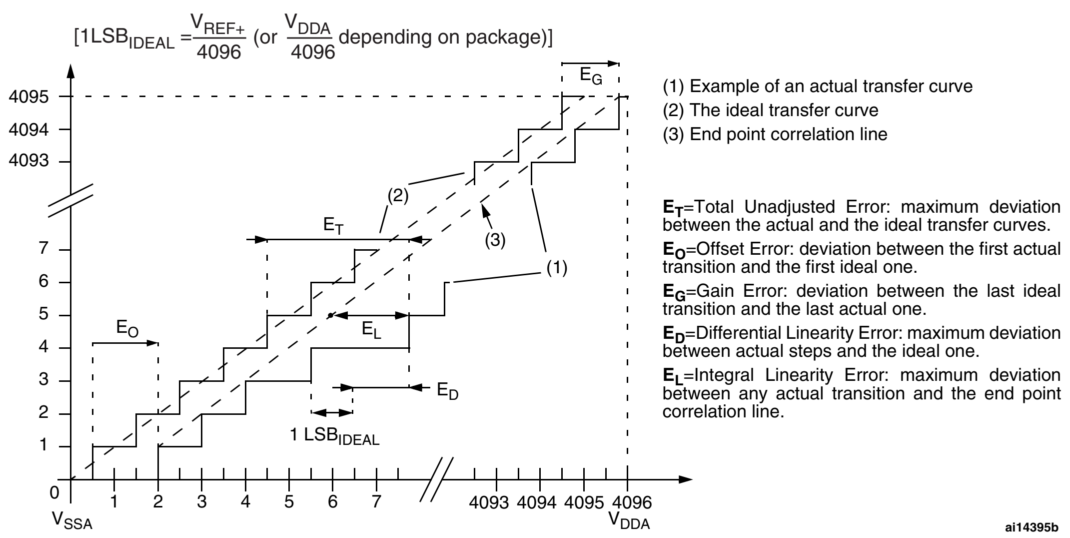
1. Based on characterization results, not tested in production.
2. Guaranteed by design.
3. $V_{REF+}$ can be internally connected to $V_{DDA}$ and $V_{REF-}$ can be internally connected to $V_{SSA}$, depending on the package. Refer to *Table 4: Low & medium-density STM32F100xx pin definitions* and *Figure 6* for further details.
4. For external triggers, a delay of 1/$f_{PCLK2}$ must be added to the latency specified in *Table 42*.

**Equation 1: $R_{AIN}$ max formula:**

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above formula (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Figure 32. ADC accuracy characteristics



$E_T$=Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.

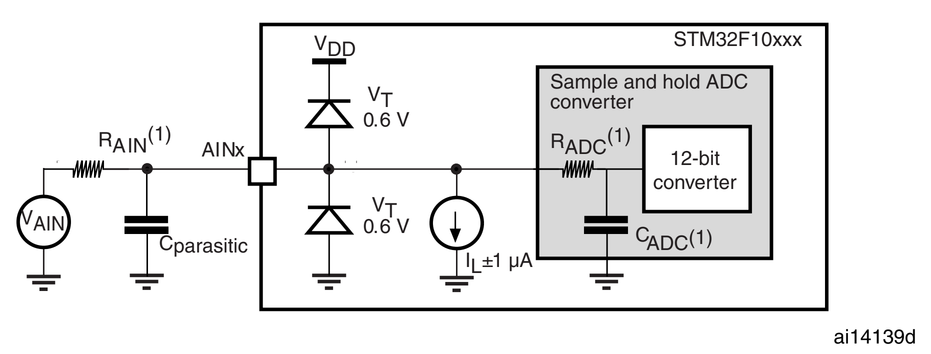
$E_O$=Offset Error: deviation between the first actual transition and the first ideal one.

$E_G$=Gain Error: deviation between the last ideal transition and the last actual one.

$E_D$=Differential Linearity Error: maximum deviation between actual steps and the ideal one.

$E_L$=Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 33. Typical connection diagram using the ADC



1. Refer to *Table 42* for the values of $R_{AIN}$, $R_{ADC}$ and $C_{ADC}$.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

## General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 34* or *Figure 35*, depending on whether $V_{REF+}$ is connected to $V_{DDA}$ or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

### 5.3.18 DAC electrical specifications

**Table 46. DAC characteristics**

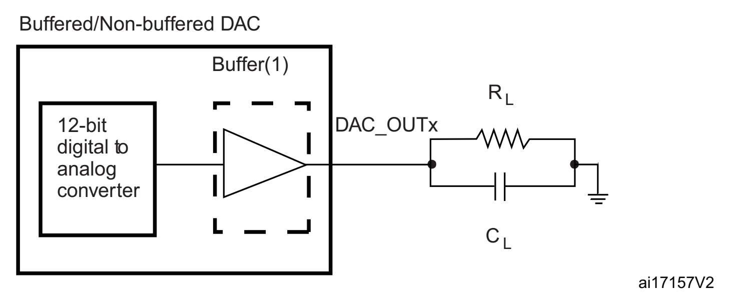
| Symbol | Parameter | Min | Typ | Max(1) | Unit | Comments |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | 2.4 | - | 3.6 | V | - |
| $V_{REF+}$ | Reference supply voltage | 2.4 | - | 3.6 | V | $V_{REF+}$ must always be below $V_{DDA}$ |
| $V_{SSA}$ | Ground | 0 | - | 0 | V | - |
| $R_{LOAD}$(2) | Resistive load with buffer ON | 5 | - | - | kΩ | - |
| $R_O$(1) | Impedance output with buffer OFF | - | - | 15 | kΩ | When the buffer is OFF, the Minimum resistive load between DAC_OUT and $V_{SS}$ to have a 1% accuracy is 1.5 MΩ |
| $C_{LOAD}$(1) | Capacitive load | - | - | 50 | pF | Maximum capacitive load at DAC_OUT pin (when the buffer is ON). |
| DAC_OUT min(1) | Lower DAC_OUT voltage with buffer ON | 0.2 | - | - | V | It gives the maximum output excursion of the DAC.<br>It corresponds to 12-bit input code (0x0E0) to (0xF1C) at $V_{REF+}$ = 3.6 V and (0x155) and (0xEAB) at $V_{REF+}$ = 2.4 V |
| DAC_OUT max(1) | Higher DAC_OUT voltage with buffer ON | - | - | $V_{DDA} - 0.2$ | V | |
| DAC_OUT min(1) | Lower DAC_OUT voltage with buffer OFF | - | 0.5 | - | mV | It gives the maximum output excursion of the DAC. |
| DAC_OUT max(1) | Higher DAC_OUT voltage with buffer OFF | - | - | $V_{REF+}$ – 1LSB | V | |
| $I_{DDVREF+}$ | DAC DC current consumption in quiescent mode (Standby mode) | - | - | 220 | µA | With no load, worst code (0xF1C) at $V_{REF+}$ = 3.6 V in terms of DC consumption on the inputs |
| $I_{DDA}$ | DAC DC current consumption in quiescent mode (Standby mode) | - | - | 380 | µA | With no load, middle code (0x800) on the inputs |
| | | - | - | 480 | µA | With no load, worst code (0xF1C) at $V_{REF+}$ = 3.6 V in terms of DC consumption on the inputs |
| DNL(1) | Differential non linearity Difference between two consecutive code-1LSB) | - | - | ±0.5 | LSB | Given for the DAC in 10-bit configuration |
| | | - | - | ±2 | LSB | Given for the DAC in 12-bit configuration |
| INL(1) | Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023) | - | - | ±1 | LSB | Given for the DAC in 10-bit configuration |
| | | - | - | ±4 | LSB | Given for the DAC in 12-bit configuration |

**Table 46. DAC characteristics (continued)**

| Symbol | Parameter | Min | Typ | Max[(1)] | Unit | Comments |
|---|---|---|---|---|---|---|
| Offset[(1)] | Offset error<br>(difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$) | - | - | ±10 | mV | Given for the DAC in 12-bit configuration |
| | | - | - | ±3 | LSB | Given for the DAC in 10-bit at $V_{REF+}$ = 3.6 V |
| | | - | - | ±12 | LSB | Given for the DAC in 12-bit at $V_{REF+}$ = 3.6 V |
| Gain error[(1)] | Gain error | - | - | ±0.5 | % | Given for the DAC in 12bit configuration |
| $t_{SETTLING}$[(1)] | Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB | - | 3 | 4 | µs | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ |
| Update rate[(1)] | Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB) | - | - | 1 | MS/s | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ |
| $t_{WAKEUP}$[(1)] | Wakeup time from off state (Setting the ENx bit in the DAC Control register) | - | 6.5 | 10 | µs | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ<br>input code between lowest and highest possible ones. |
| PSRR+ [(1)] | Power supply rejection ratio (to $V_{DDA}$) (static DC measurement | - | –67 | –40 | dB | No $R_{LOAD}$, $C_{LOAD}$ = 50 pF |

1. Guaranteed by characterization results.
2. Guaranteed by design.

**Figure 36. 12-bit buffered /non-buffered DAC**



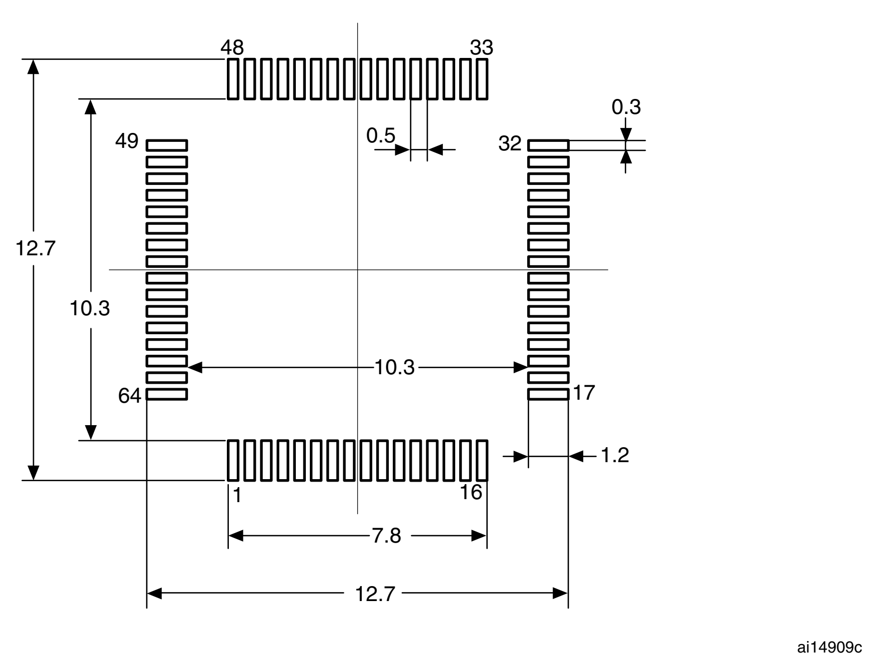
1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

### Table 49. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

| Symbol | millimeters | | | inches[(1)] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| e | - | 0.500 | - | - | 0.0197 | - |
| K | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

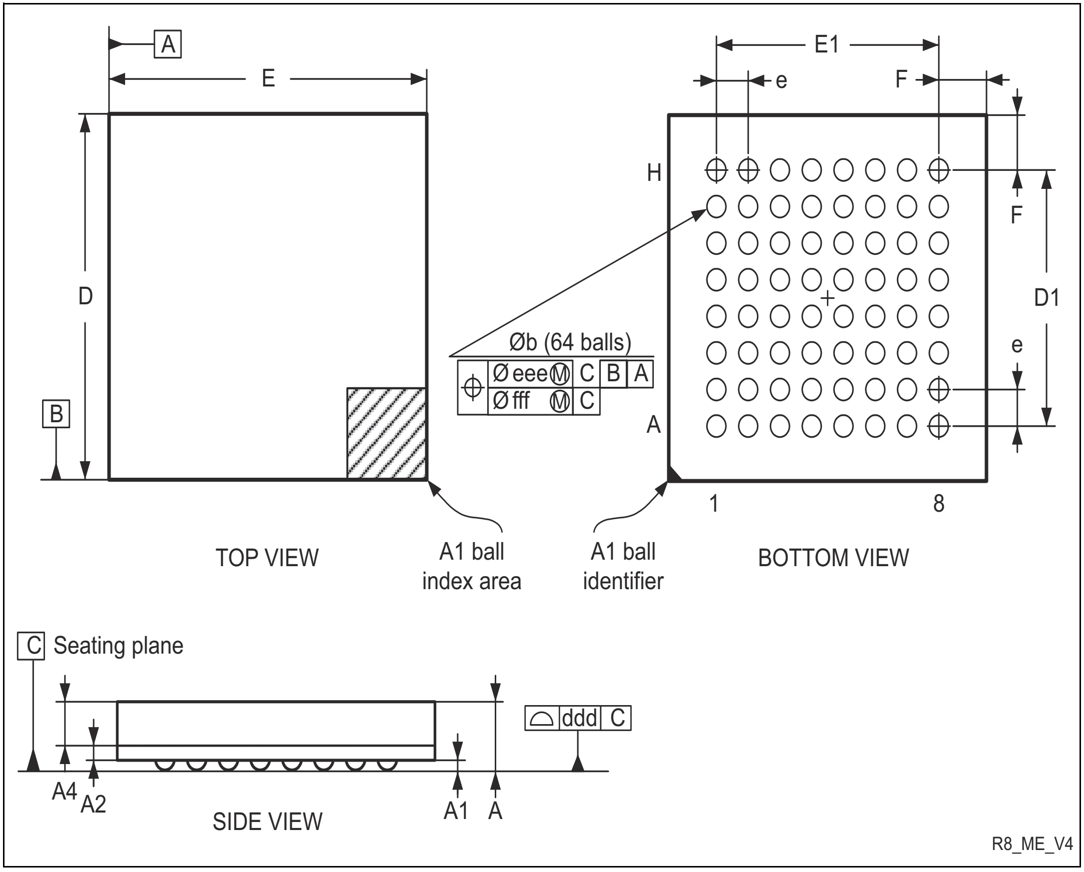
### Figure 41.LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint



1. Dimensions are in millimeters.

## 6.3 TFBGA64 package information

**Figure 43. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch thin profile fine pitch ball grid array package outline**



1. Drawing is not to scale.

**Table 50. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package mechanical data**

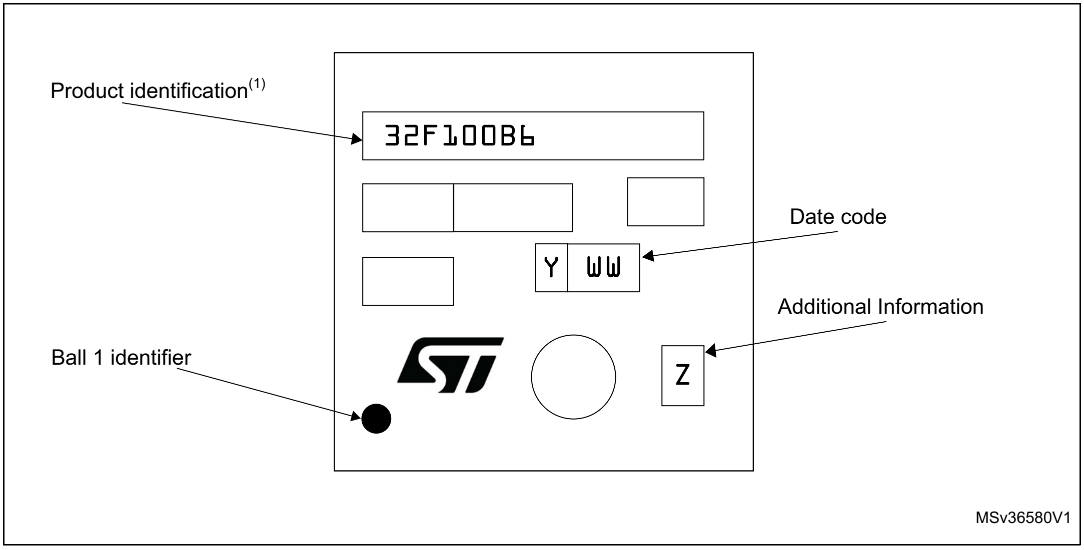
| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.200 | - | - | 0.0472 |
| A1 | 0.150 | - | - | 0.0059 | - | - |
| A2 | - | 0.200 | - | - | 0.0079 | - |
| A4 | - | - | 0.600 | - | - | 0.0236 |
| b | 0.250 | 0.300 | 0.350 | 0.0098 | 0.0118 | 0.0138 |
| D | 4.850 | 5.000 | 5.150 | 0.1909 | 0.1969 | 0.2028 |
| D1 | - | 3.500 | - | - | 0.1378 | - |
| E | 4.850 | 5.000 | 5.150 | 0.1909 | 0.1969 | 0.2028 |

## Device marking for TFBGA64

The following figure gives an example of topside marking and pin 1 position identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 45. TFBGA64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

### 6.5.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 54: Ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F10xxx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

#### Example: high-performance application

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax}$ = 82 °C (measured according to JESD51-2), $I_{DDmax}$ = 50 mA, $V_{DD}$ = 3.5 V, maximum 20 I/Os used at the same time in output at low level with $I_{OL}$ = 8 mA, $V_{OL}$= 0.4 V and maximum 8 I/Os used at the same time in output mode at low level with $I_{OL}$ = 20 mA, $V_{OL}$= 1.3 V

$P_{INTmax} = 50\ mA \times 3.5\ V = 175\ mW$

$P_{IOmax} = 20 \times 8\ mA \times 0.4\ V + 8 \times 20\ mA \times 1.3\ V = 272\ mW$

This gives: $P_{INTmax}$ = 175 mW and $P_{IOmax}$ = 272 mW

$P_{Dmax} = 175 + 272 = 447\ mW$

Thus: $P_{Dmax}$ = 447 mW

Using the values obtained in *Table 53* $T_{Jmax}$ is calculated as follows:

– For LQFP64, 45 °C/W

$T_{Jmax}$ = 82 °C + (45 °C/W × 447 mW) = 82 °C + 20.1 °C = 102.1 °C

This is within the range of the suffix 6 version parts ($–40 < T_J < 105$ °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Table 54: Ordering information scheme*).

#### Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature $T_J$ remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax}$ = 115 °C (measured according to JESD51-2), $I_{DDmax}$ = 20 mA, $V_{DD}$ = 3.5 V, maximum 20 I/Os used at the same time in output at low level with $I_{OL}$ = 8 mA, $V_{OL}$= 0.4 V

$P_{INTmax} = 20\ mA \times 3.5\ V = 70\ mW$

$P_{IOmax} = 20 \times 8\ mA \times 0.4\ V = 64\ mW$

This gives: $P_{INTmax}$ = 70 mW and $P_{IOmax}$ = 64 mW:

$P_{Dmax} = 70 + 64 = 134\ mW$

Thus: $P_{Dmax}$ = 134 mW