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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f100rbt6btr

higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

2.2.11 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop mode
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode, providing high impedance output.

2.2.12 Low-power modes

The STM32F100xx value line supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop** mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.
  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output or the RTC alarm.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), a IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.2.13 DMA

The flexible 7-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

2.2.23 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in noninverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- up to 10-bit output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channels' independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the STM32F100xx. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

2.2.24 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < V_{DDA} < 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.2.25 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

Figure 4. STM32F100xx value line LQFP64 pinout

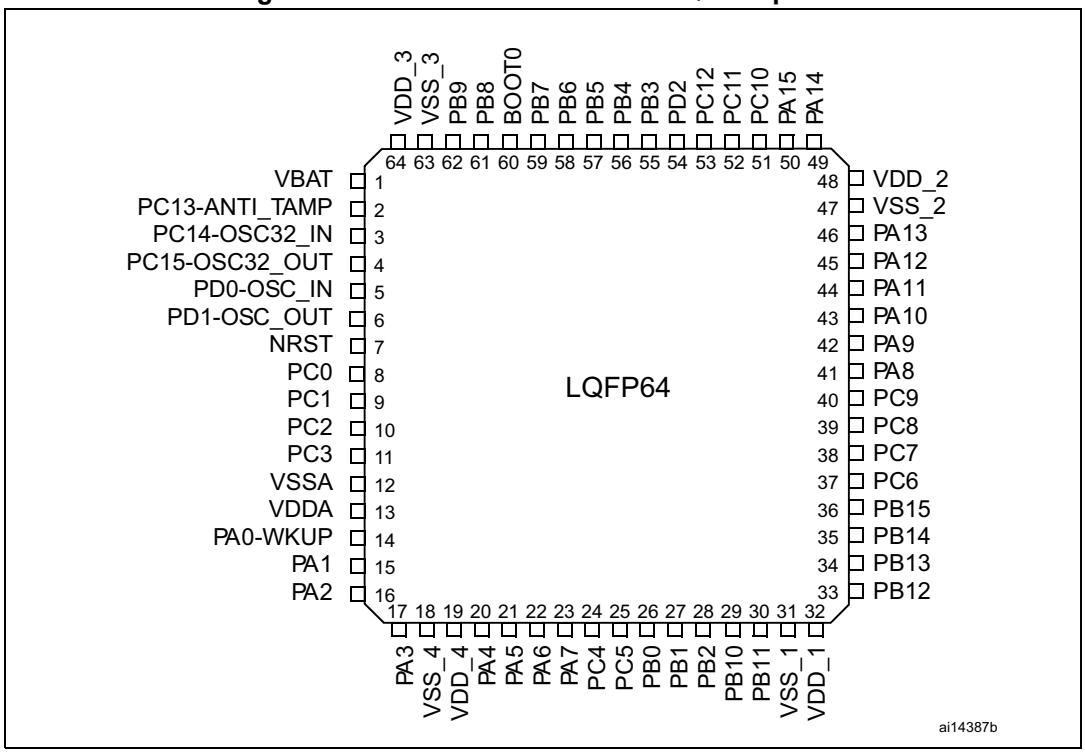


Figure 5. STM32F100xx value line LQFP48 pinout

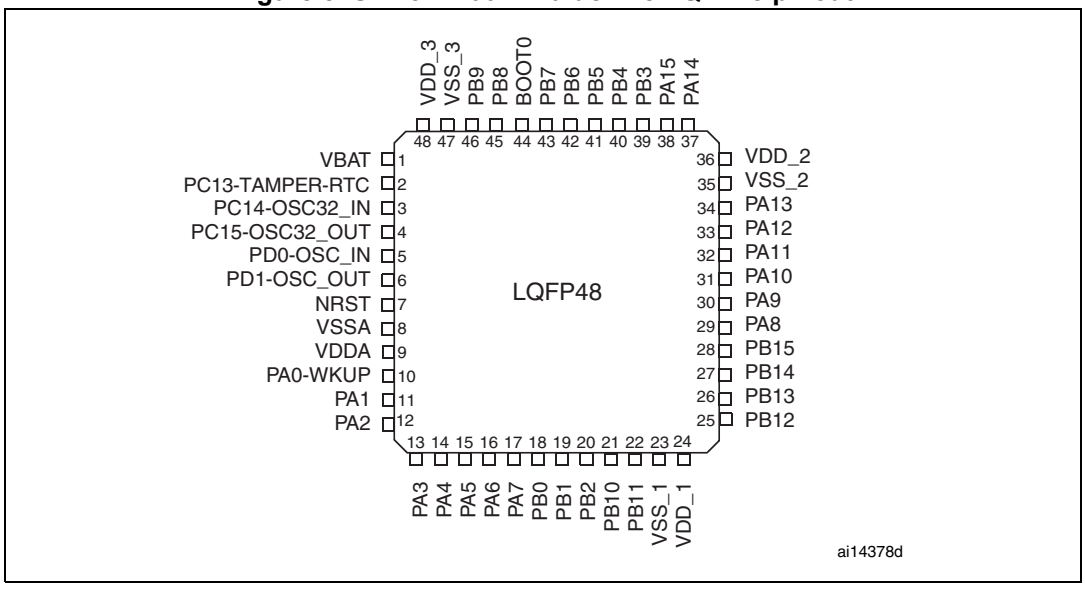


Figure 6. STM32F100xx value line TFBGA64 ballout

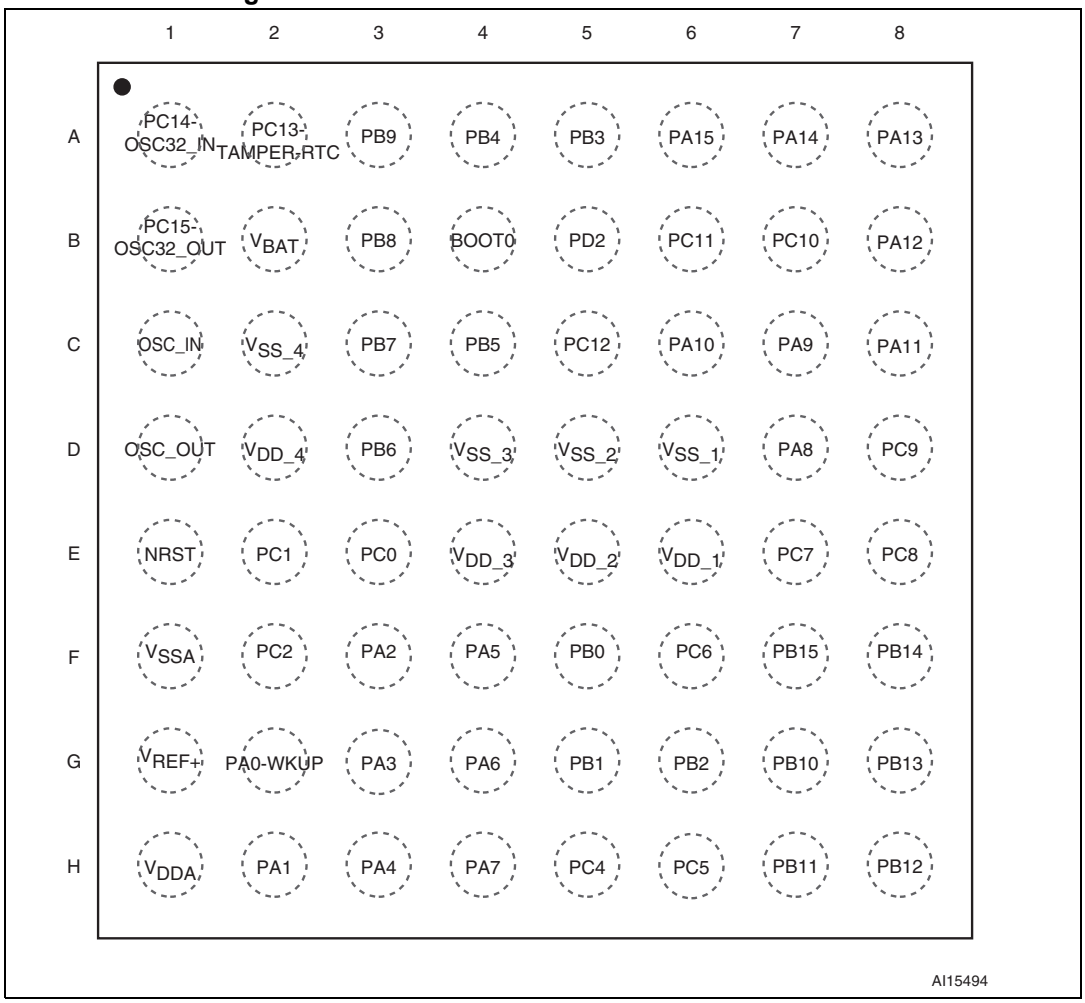


Table 4. Low & medium-density STM32F100xx pin definitions

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3)(4)	
LQFP100	LQFP64	TFBGA64	LQFP48					Default	Remap
1	-	-	-	PE2	I/O	FT	PE2	TRACECLK	-
2	-	-	-	PE3	I/O	FT	PE3	TRACED0	-
3	-	-	-	PE4	I/O	FT	PE4	TRACED1	-
4	-	-	-	PE5	I/O	FT	PE5	TRACED2	-
5	-	-	-	PE6	I/O	FT	PE6	TRACED3	-
6	1	B2	1	V_{BAT}	S	-	V_{BAT}	-	-
7	2	A2	2	PC13-TAMPER-RTC(5)	I/O	-	PC13(6)	TAMPER-RTC	-
8	3	A1	3	PC14-OSC32_IN(5)	I/O	-	PC14(6)	OSC32_IN	-

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 2 V ≤V_{DD} ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

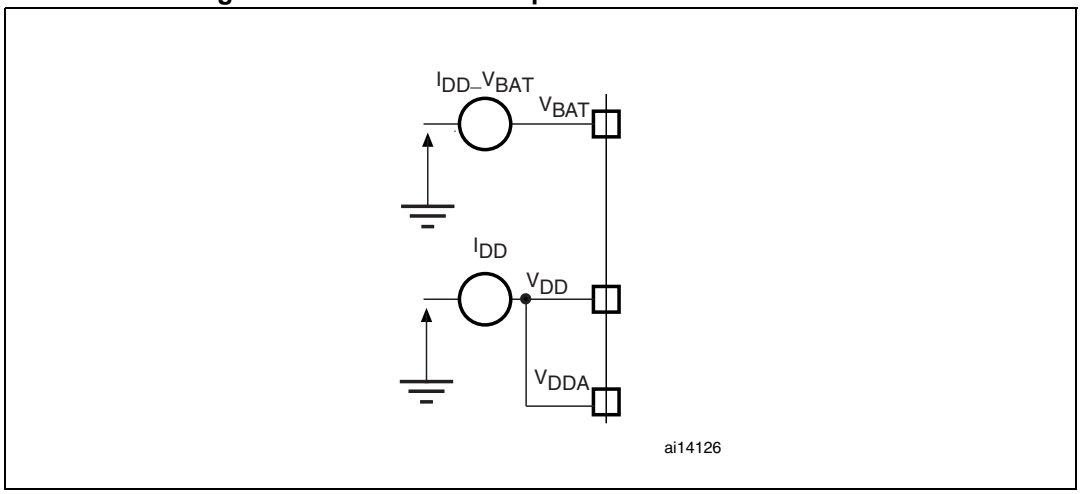
The loading conditions used for pin parameter measurement are shown in *Figure 8*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

5.1.7 Current consumption measurement

Figure 11. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 5: Voltage characteristics*, *Table 6: Current characteristics*, and *Table 7: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD} –V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}(2)	Input voltage on five volt tolerant pin	V_{SS} –0.3	V_{DD} +4.0	
	Input voltage on any other pin	V_{SS} –0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 5.3.11: Absolute maximum ratings (electrical sensitivity)*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 6: Current characteristics* for the maximum allowed injected current values.

Figure 12. Maximum current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled

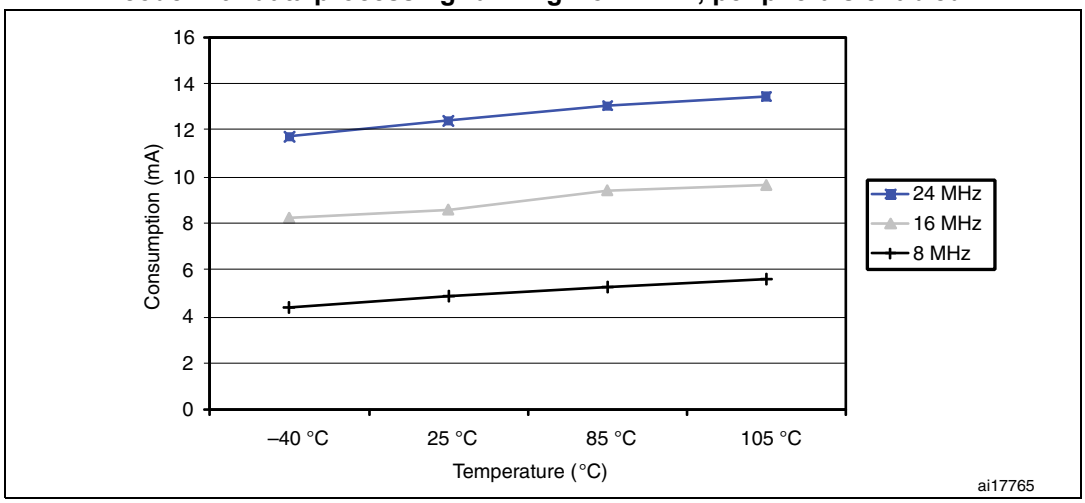


Figure 13. Maximum current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled

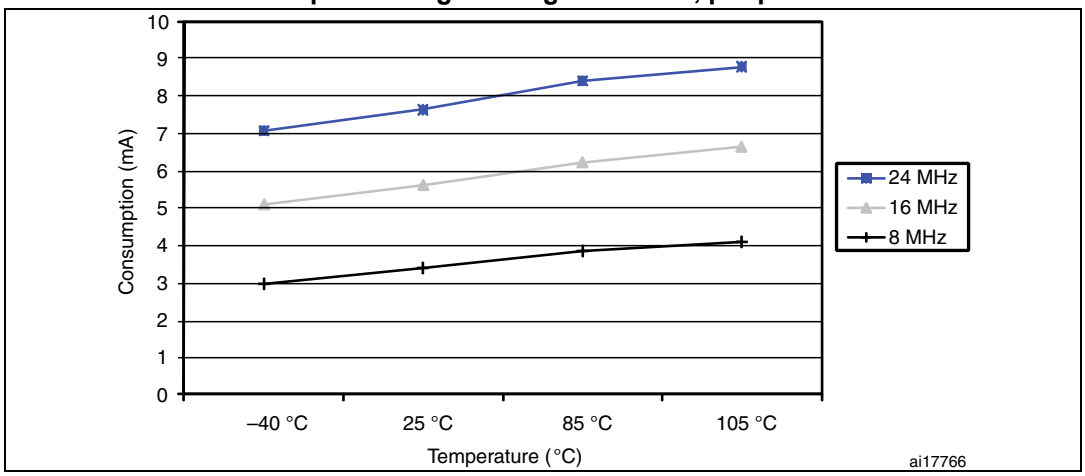


Table 14. Maximum current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	External clock(2) all peripherals enabled	24 MHz	9.6	10	mA
			16 MHz	7.1	7.5	
			8 MHz	4.5	4.8	
		External clock(2), all peripherals disabled	24 MHz	3.8	4	
			16 MHz	3.3	3.5	
			8 MHz	2.7	3	

1. Guaranteed by characterization, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Figure 15. Typical current consumption in Stop mode with regulator in Run mode versus temperature at V_{DD} = 3.3 V and 3.6 V

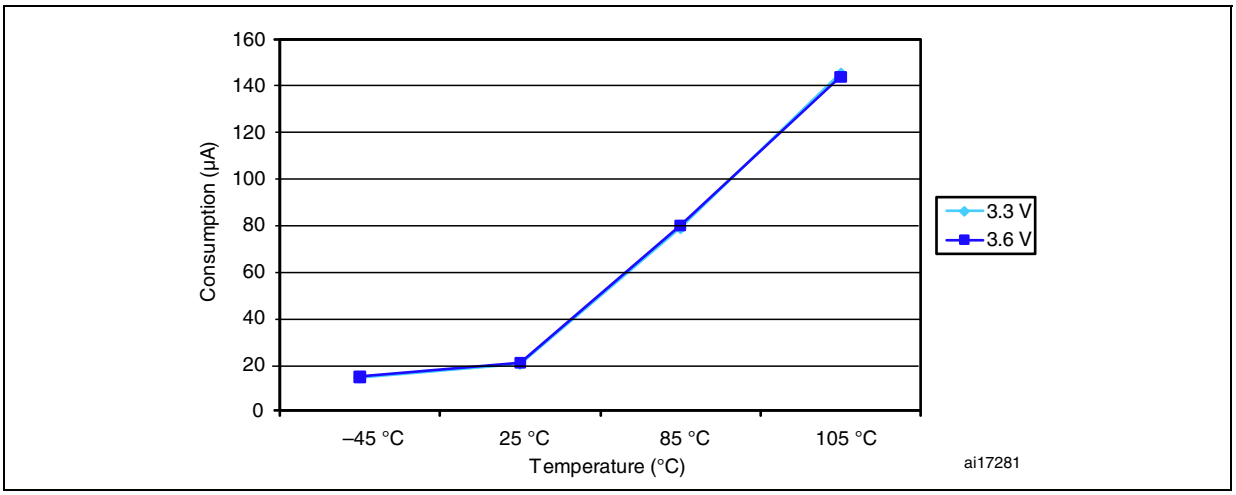


Figure 16. Typical current consumption in Stop mode with regulator in Low-power mode versus temperature at V_{DD} = 3.3 V and 3.6 V

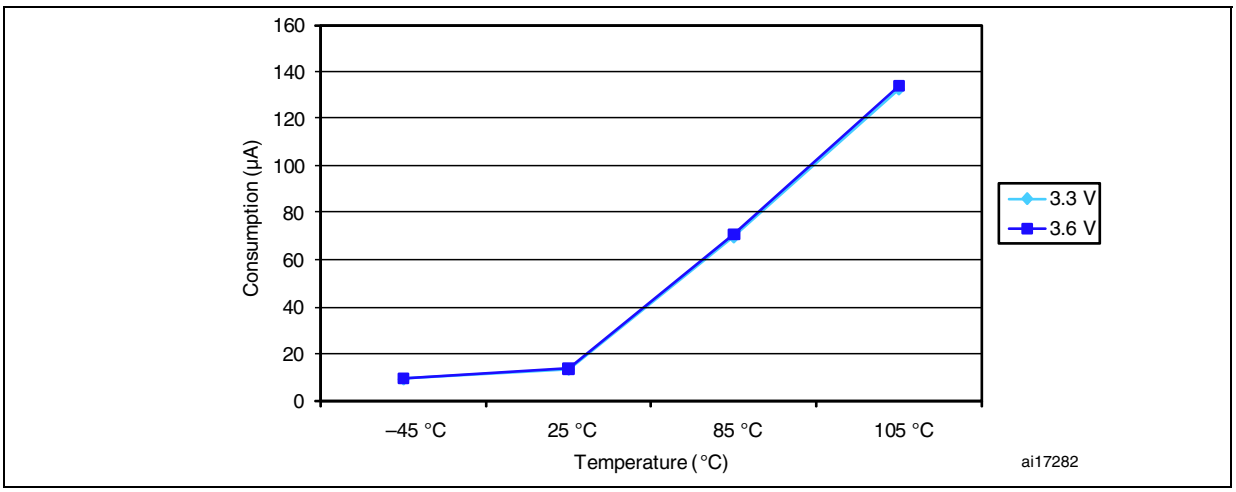


Table 16. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typical values(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Run mode	Running on high-speed external clock with an 8 MHz crystal(3)	24 MHz	12.8	9.3	mA
			16 MHz	9.3	6.6	
			8 MHz	5.1	3.9	
			4 MHz	3.2	2.5	
			2 MHz	2.1	1.75	
			1 MHz	1.55	1.4	
			500 kHz	1.3	1.2	
			125 kHz	1.1	1.05	
		Running on high-speed internal RC (HSI)	24 MHz	12.2	8.6	
			16 MHz	8.5	6	
			8 MHz	4.6	3.3	
			4 MHz	2.6	1.9	
			2 MHz	1.5	1.15	
			1 MHz	0.9	0.8	
			500 kHz	0.65	0.6	
			125 kHz	0.45	0.43	

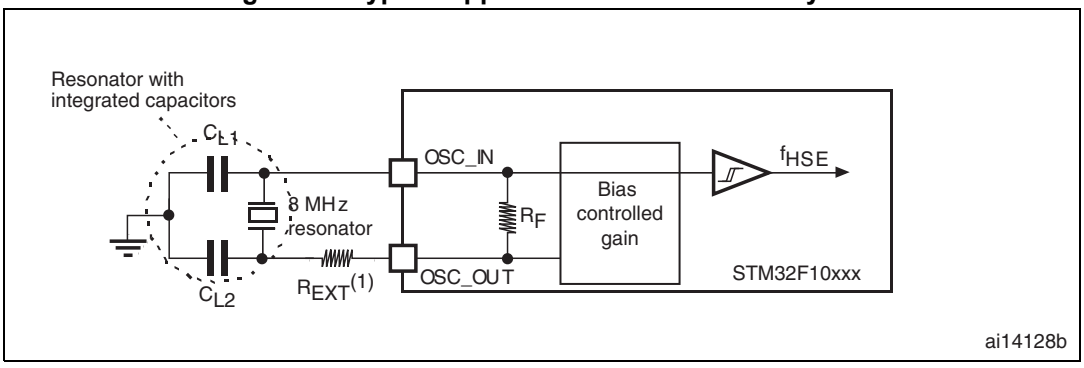
1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA for the ADC and of 0.5 mA for the DAC analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. An 8 MHz crystal is used as the external clock source. The AHB prescaler is used to reduce the frequency when f_{HCLK} < 8 MHz, the PLL is used when f_{HCLK} > 8 MHz.

Table 21. HSE 4-24 MHz oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	24	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
C_{L1} C_{L2}(3)	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(4)	R_S = 30 Ω	-	30	-	pF
i_2	HSE driving current	V_{DD} = 3.3 V V_{IN} = V_{SS} with 30 pF load	-	-	1	mA
g_m	Oscillator transconductance	Startup	25	-	-	mA/V
$t_{SU(HSE)}$ (5)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results.
3. It is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.
4. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
5. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Figure 20. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 22*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Note: For C_{L1} and C_{L2} it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.
Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.
For further details, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF) it is strongly recommended to use a resonator with a load capacitance $C_L \leq 7$ pF. Never use a resonator with a load capacitance of 12.5 pF.
Example: if you choose a resonator with a load capacitance of C_L = 6 pF, and C_{stray} = 2 pF, then $C_{L1} = C_{L2}$ = 8 pF.

Table 22. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_F	Feedback resistor	-		-	5	-	MΩ
C_{L1} C_{L2}(2)	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 KΩ		-	-	15	pF
I_2	LSE driving current	V_{DD} = 3.3 V V_{IN} = V_{SS}		-	-	1.4	µA
g_m	Oscillator transconductance	-		5	-	-	µA/V
$t_{SU(LSE)}$(4)	Startup time	V_{DD} is stabilized	T_A = 50 °C	-	1.5	-	s
			T_A = 25 °C	-	2.5	-	
			T_A = 10 °C	-	4	-	
			T_A = 0 °C	-	6	-	
			T_A = -10 °C	-	10	-	
			T_A = -20 °C	-	17	-	
			T_A = -30 °C	-	32	-	
			T_A = -40 °C	-	60	-	

1. Guaranteed by characterization results.
2. Refer to the note and caution paragraphs above the table.
3. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value for example MSIV-TIN32.768 kHz. Refer to crystal manufacturer for more details
4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Low-speed internal (LSI) RC oscillator

Table 24. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	60	kHz
$\Delta f_{LSI(T)}$	Temperature-related frequency drift(2)	-9	-	9	%
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.65	1.2	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C °C unless otherwise specified.
2. Guaranteed by characterization results.
3. Guaranteed by design.

Wakeup time from low-power mode

The wakeup times given in *Table 25* are measured on a wakeup phase with an 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 25. Low-power mode wakeup timings

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	1.8	µs
t_{WUSTOP}(1)	Wakeup from Stop mode (regulator in run mode)	3.6	µs
	Wakeup from Stop mode (regulator in low-power mode)	5.4	
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	50	µs

1. The wakeup times are measured from the wakeup event to the point at which the user application code reads the first instruction.

5.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 27. Flash memory characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	52.5	70	µs
t_{ERASE}	Page (1 KB) erase time	T_A = –40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Read mode f_{HCLK} = 24 MHz, V_{DD} = 3.3 V	-	-	20	mA
		Write / Erase modes f_{HCLK} = 24 MHz, V_{DD} = 3.3 V	-	-	5	mA
		Power-down mode / Halt, V_{DD} = 3.0 to 3.6 V	-	-	50	µA
V_{prog}	Programming voltage	-	2	-	3.6	V

1. Guaranteed by design.

Table 28. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value			Unit
			Min(1)	Typ	Max	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	-	-	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	-	-	Years
		1 kcycle(2) at T_A = 105 °C	10	-	-	
		10 kcycles(2) at T_A = 55 °C	20	-	-	

1. Based on characterization not tested in production.
2. Cycling performed over the whole temperature range.

5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (Electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 29*. They are based on the EMS levels and classes defined in application note AN1709.

Table 29. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 24 MHz, LQFP100 package, conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 24 MHz, LQFP100 package, conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second. To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

5.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 34* are derived from tests performed under the conditions summarized in *Table 8*. All I/Os are CMOS and TTL compliant.

Table 34. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard I/O input low level voltage	-	–0.3	-	0.28*(V_{DD}–2 V)+0.8 V	V
	I/O FT(1) input low level voltage		–0.3	-	0.32*(V_{DD}–2 V)+0.75 V	
V_{IH}	Standard I/O input high level voltage		0.41*(V_{DD}–2 V) +1.3 V	-	V_{DD}+0.3	
	I/O FT(1) input high level voltage	V_{DD} > 2 V	0.42*(V_{DD}–2)+1 V	-	5.5	
		V_{DD} ≤2 V			5.2	
V_{hys}	Standard I/O Schmitt trigger voltage hysteresis(2)	-	200	-	-	mV
	I/O FT Schmitt trigger voltage hysteresis(2)		5% V_{DD}(3)	-	-	mV
I_{lkg}	Input leakage current(4)	V_{SS} ≤V_{IN} ≤V_{DD} Standard I/Os	-	-	±1	µA
		V_{IN} = 5 V I/O FT	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(5)	V_{IN} = V_{SS}	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	V_{IN} = V_{DD}	30	40	50	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. FT = 5V tolerant. To sustain a voltage higher than V_{DD}+0.3 the internal pull-up/pull-down resistors must be disabled.
2. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by design.
3. With a minimum of 100 mV.
4. Leakage could be higher than max. if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 22* and *Figure 23* for standard I/Os, and in *Figure 24* and *Figure 25* for 5 V tolerant I/Os.

Table 42. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
I_{VREF}	Current on the V_{REF} input pin	-	-	160(1)	220(1)	µA
f_{ADC}	ADC clock frequency	-	0.6	-	12	MHz
f_S(2)	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 12 MHz	-	-	705	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}(3)	Conversion voltage range	-	0 (V_{SSA} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* and *Table 43* for details	-	-	50	kΩ
R_{ADC}(2)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 12 MHz	6.9			µs
		-	83			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 12 MHz	-	-	0.25	µs
		-	-	-	3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 12 MHz	-	-	0.166	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 12 MHz	0.125	-	20.0	µs
			1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	0	0	1	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 12 MHz	1.17	-	21	µs
		-	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Based on characterization results, not tested in production.
2. Guaranteed by design.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Table 4: Low & medium-density STM32F100xx pin definitions* and *Figure 6* for further details.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 42*.

Equation 1: R_{AIN} max formula:

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above formula (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 43. R_{AIN} max for f_{ADC} = 12 MHz(1)

T_s (cycles)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.125	0.4
7.5	0.625	5.9
13.5	1.125	11.4
28.5	2.375	25.2
41.5	3.45	37.2
55.5	4.625	50
71.5	5.96	NA
239.5	20	NA

1. Guaranteed by design.

Table 44. ADC accuracy - limited test conditions(1)(2)

Symbol	Parameter	Test conditions	Typ	Max	Unit
ET	Total unadjusted error	f_{PCLK2} = 24 MHz, f_{ADC} = 12 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3 V to 3.6 V V_{REF+} = V_{DDA} T_A = 25 °C Measurements made after ADC calibration	±1.3	±2.2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	

1. ADC DC accuracy values are measured after internal calibration.
2. Guaranteed by characterization results.

Table 45. ADC accuracy(1) (2) (3)

Symbol	Parameter	Test conditions	Typ	Max	Unit
ET	Total unadjusted error	f_{PCLK2} = 24 MHz, f_{ADC} = 12 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V T_A = Full operating range Measurements made after ADC calibration	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted V_{DD}, frequency, V_{REF} and temperature ranges.
3. Guaranteed by characterization results.

Note: ADC accuracy vs. negative injection current: Injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.12* does not affect the ADC accuracy.

5.3.19 Temperature sensor characteristics

Table 47. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L (1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope (1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25} (1)	Voltage at 25°C	1.32	1.41	1.50	V
t_{START} (2)	Startup time	4	-	10	µs
T_{S_temp} (3)(2)	ADC sampling time when reading the temperature	-	-	17.1	µs

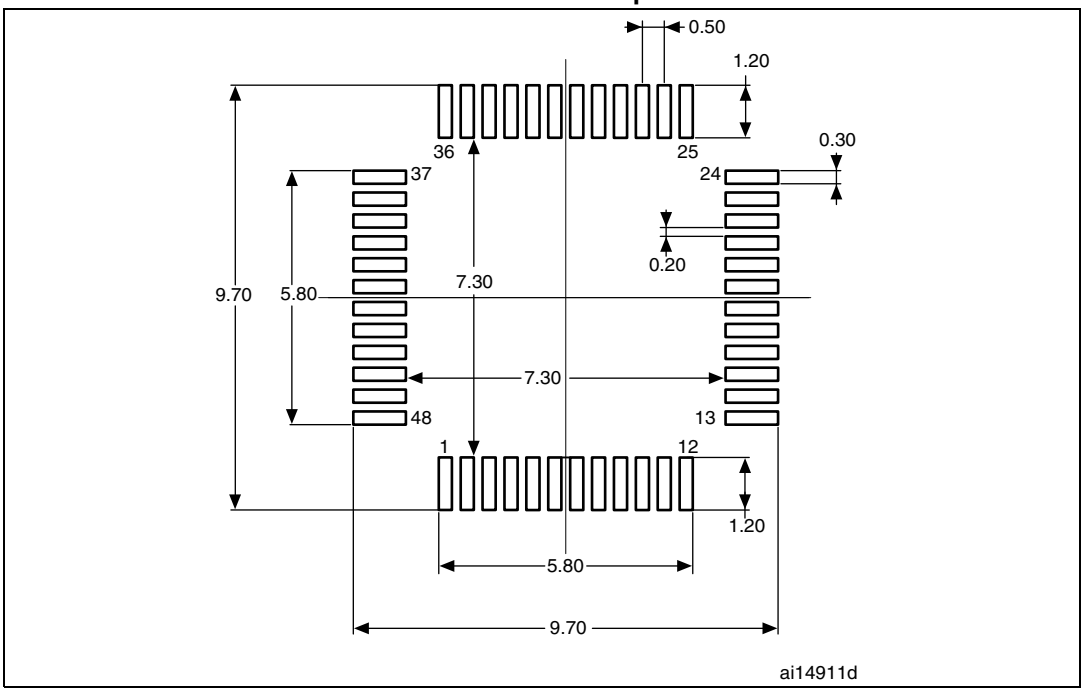
1. Guaranteed by characterization results.
2. Guaranteed by design.
3. Shortest sampling time can be determined in the application by multiple iterations.

Table 52. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 47. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

6.5 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 8: General operating conditions on page 34*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 53. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP 100 - 14 × 14 mm / 0.5 mm pitch	46	°C/W
	Thermal resistance junction-ambient LQFP 64 - 10 × 10 mm / 0.5 mm pitch	45	
	Thermal resistance junction-ambient TFBGA64 - 5 × 5 mm / 0.5 mm pitch	65	
	Thermal resistance junction-ambient LQFP 48 - 7 × 7 mm / 0.5 mm pitch	55	

6.5.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.