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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f100rct7b

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2 Description

The STM32F100x4, STM32F100x6, STM32F100x8 and STM32F100xB microcontrollers incorporate the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a 24 MHz frequency, high-speed embedded memories (Flash memory up to 128 Kbytes and SRAM up to 8 Kbytes), and an extensive range of enhanced peripherals and I/Os connected to two APB buses. All devices offer standard communication interfaces (up to two I²Cs, two SPIs, one HDMI CEC, and up to three USARTs), one 12-bit ADC, two 12-bit DACs, up to six general-purpose 16-bit timers and an advanced-control PWM timer.

The STM32F100xx low- and medium-density devices operate in the -40 to +85 °C and -40 to +105 °C temperature ranges, from a 2.0 to 3.6 V power supply.

A comprehensive set of power-saving mode allows the design of low-power applications.

These microcontrollers include devices in three different packages ranging from 48 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included.

These features make these microcontrollers suitable for a wide range of applications such as application control and user interfaces, medical and hand-held equipment, PC and gaming peripherals, GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms, and HVACs.



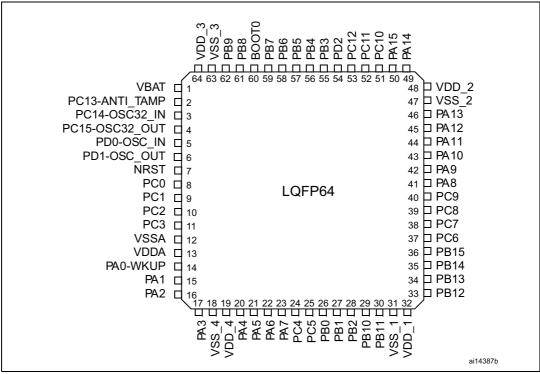


Figure 4. STM32F100xx value line LQFP64 pinout



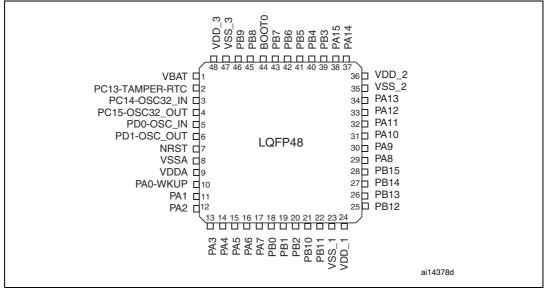


Table 4. Low & medium-density STM32F100xx pin definitions (continued)

	Pi	ns				ຄ		Alternate function	s ⁽³⁾⁽⁴⁾
LQFP100	LQFP64	TFBGA64	LQFP48	Pin name	Type ⁽¹⁾	I / O level ⁽²⁾	Main function ⁽³⁾ (after reset)	Default	Remap
33	24	H5	-	PC4	I/O	-	PC4	ADC1_IN14	-
34	25	Н6	-	PC5	I/O	-	PC5	ADC1_IN15	-
35	26	F5	18	PB0	I/O	-	PB0	ADC1_IN8/TIM3_CH3 ⁽¹²⁾	TIM1_CH2N
36	27	G5	19	PB1	I/O	-	PB1	ADC1_IN9/TIM3_CH4 ⁽¹²⁾	TIM1_CH3N
37	28	G6	20	PB2	I/O	FT	PB2/BOOT1	-	-
38	-	-	-	PE7	I/O	FT	PE7	-	TIM1_ETR
39	-	-	-	PE8	I/O	FT	PE8	-	TIM1_CH1N
40	-	-	-	PE9	I/O	FT	PE9	-	TIM1_CH1
41	-	-	-	PE10	I/O	FT	PE10	-	TIM1_CH2N
42	-	-	-	PE11	I/O	FT	PE11	-	TIM1_CH2
43	-	-	-	PE12	I/O	FT	PE12	-	TIM1_CH3N
44	-	-	-	PE13	I/O	FT	PE13	-	TIM1_CH3
45	-	-	-	PE14	I/O	FT	PE14	-	TIM1_CH4
46	-	-	-	PE15	I/O	FT	PE15	-	TIM1_BKIN
47	29	G7	21	PB10	I/O	FT	PB10	I2C2_SCL ⁽⁹⁾ /USART3_TX	TIM2_CH3 / HDMI_CEC
48	30	H7	22	PB11	I/O	FT	PB11	I2C2_SDA ⁽⁹⁾ /USART3_RX ⁽	TIM2_CH4
49	31	D6	23	V _{SS_1}	S	-	V _{SS_1}	-	-
50	32	E6	24	V _{DD_1}	S	-	V _{DD_1}	-	-
51	33	Н8	25	PB12	I/O	FT	PB12	SPI2_NSS ⁽¹⁰⁾ / I2C2_SMBA ⁽⁹⁾ / TIM1_BKIN ⁽¹²⁾ /USART3_C K ⁽¹²⁾	-
52	34	G8	26	PB13	I/O	FT	PB13	SPI2_SCK ⁽¹⁰⁾ /TIM1_CH1N ⁽¹²⁾ USART3_CTS ⁽¹²⁾	-
53	35	F8	27	PB14	I/O	FT	PB14	SPI2_MISO ⁽¹⁰⁾ / TIM1_CH2N ⁽¹²⁾ / USART3_RTS ⁽¹²⁾	TIM15_CH1
54	36	F7	28	PB15	I/O	FT	PB15	SPI2_MOSI ⁽¹⁰⁾ / TIM1_CH3N / TIM15_CH1N ⁽¹²⁾	TIM15_CH2
55	-	-	-	PD8	I/O	FT	PD8	-	USART3_TX
56	-	-	-	PD9	I/O	FT	PD9	-	USART3_RX

0x4000 4C00

0x4000 4800

0x4000 4400

0x4000 3C00

0x4000 3400

0x4000 3000

0x4000 2800

0x4000 1800

0x4000 1400

0x4000 1000

0x4000 0C00 0x4000 0800

0x4000 0400 0x4000 0000 USART3

USART2

reserved

reserved

WWDG RTC

TIM7

TIM6

reserved

TIM3

4 Memory mapping

The memory map is shown in Figure 7.

OxFEEE FEEE 0x4002 3000 CRC 0x4002 2400 0x4002 2000 Flash interface 0x4002 1400 0x4002 1000 0x4002 0400 reserved 0xE010 0000 0x4002 0000 Cortex-M3 internal 0xE000 0000 0x4001 4C00 TIM17 0x4001 4800 0x4001 4400 TIM16 0x4001 4000 TIM15 0xC000 0000 USART1 0x4001 3800 0x4001 3400 reserved 0x4001 3000 SPI1 TIM1 0x4001 2800 0xA000 0000 0x4001 2400 ADC1 0x4001 1C00 reserved 0x4001 1800 Port E 0x1FFF FFFF reserved 0x4001 1400 Port D 0x1FFF F80F 0x4001 1000 Port C 0x8000 0000 Option Bytes 0x4001 0C00 0x1FFF F800 0x4001 0800 Port A 0x4001 0400 EXTI System memory 0x4001 0000 0x1FFF F000 0x4000 7C00 0x4000 7800 CEC 0x4000 7400 DAC 0x4000 7000 0x4000 6C00 Peripherals 0x4000 5C00 reserved 0x4000 0000 0x4000 5800 12C2 I2C1 0x4000 5400

Flash memory

Aliased to Flash or system memory depending on BOOT pins

0x0801 FFFF

0x0000 0000

Figure 7. Memory map



MSv42612V1

30/96 DocID16455 Rev 9

SRAM

Reserved

0x2000 0000

0x0000 0000

0

5.3.4 Embedded reference voltage

The parameters given in *Table 11* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
	lada wali wafa wa a walio wa	-40 °C < T _A < +105 °C	1.16	1.20	1.26	V
V _{REFINT}	Internal reference voltage	-40 °C < T _A < +85 °C	1.16	1.20	1.24	V
T _{S_vrefint} (1)	ADC sampling time when reading the internal reference voltage	-	-	5.1	17.1 ⁽²⁾	μs
V _{RERINT} ⁽²⁾	Internal reference voltage spread over the temperature range	V _{DD} = 3 V ±10 mV	-	-	10	mV
T _{Coeff} ⁽²⁾	Temperature coefficient	-	-	-	100	ppm/°C

Table 11. Embedded internal reference voltage

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 11: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if it is explicitly mentioned
- Prefetch in on (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled f_{PCLK1} = f_{HCLK}/2, f_{PCLK2} = f_{HCLK}

The parameters given in *Table 12* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

^{1.} Shortest sampling time can be determined in the application by multiple iterations.

^{2.} Guaranteed by design.

Table 12. Maximum current consumption in Run mode, code with data processing running from Flash

Cumbal	Doromotor	Conditions		Ма	Unit	
Symbol	Parameter		f _{HCLK}	T _A = 85 °C	T _A = 105 °C	Unit
		(2)	24 MHz	15.4	15.7	
		External clock ⁽²⁾ , all peripherals enabled	16 MHz	11	11.5	
	Supply current in		8 MHz	6.7	6.9	mA
IDD	Run mode		24 MHz	10.3	10.5	ША
		External clock ⁽²⁾ , all peripherals disabled	16 MHz	7.8	8.1	
		F - F	8 MHz	5.1	5.3	

- 1. Guaranteed by characterization results.
- 2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 13. Maximum current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions	•	Ma	Unit	
Symbol	Parameter	Conditions	f _{HCLK}	T _A = 85 °C	$T_A = 85 ^{\circ}C$ $T_A = 105 ^{\circ}C$	
		(2)	24 MHz	14.5	15	
		External clock ⁽²⁾ , all peripherals enabled	16 MHz	10	10.5	
	Supply current		8 MHz	6	6.3	mA
IDD	in Run mode	(2)	24MHz	9.3	9.7	IIIA
		External clock ⁽²⁾ all peripherals disabled	16 MHz	6.8	7.2	
		, , , , , , , , , , , , , , , , , , ,	8 MHz	4.4	4.7	

- 1. Guaranteed by characterization, tested in production at $V_{\mbox{\scriptsize DD}}\,\mbox{\scriptsize max},\,f_{\mbox{\scriptsize HCLK}}\,\mbox{\scriptsize max}.$
- 2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.



Table 15. Typical and maximum current consumptions in Stop and Standby modes

				Typ ⁽¹⁾		M	lax	
Symbol	Parameter	Conditions	V _{DD} / V _{BAT} = 2.0 V	V _{DD} / V _{BAT} = 2.4 V	V _{DD} / V _{BAT} = 3.3 V	T _A = 85 °C	T _A = 105 °C	Unit
Supply		Regulator in Run mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	23.5	24	190	350	
current in Stop mode		Regulator in Low-Power mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	13.5	14	170	330	
I _{DD}		Low-speed internal RC oscillator and independent watchdog ON	-	2.6	3.4	-	-	μА
	Supply current in Standby	Low-speed internal RC oscillator ON, independent watchdog OFF	-	2.4	3.2	-	-	
	mode	Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	-	1.7	2	4	5	
I _{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	0.9	1.1	1.4	1.9	2.2	

^{1.} Typical values are measured at T_A = 25 °C.

Figure 14. Typical current consumption on $\rm V_{BAT}$ with RTC on vs. temperature at different $\rm V_{BAT}$ values

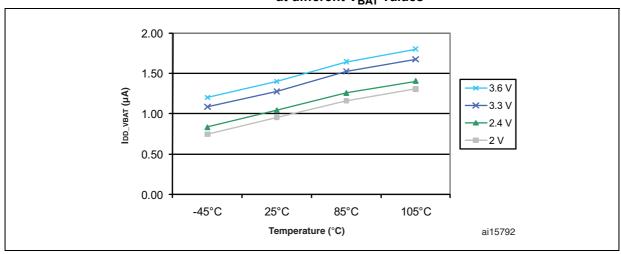


Table 16. Typical current consumption in Run mode, code with data processing running from Flash

				Typical	values ⁽¹⁾	
Symbol	Parameter Conditions f _{HCLK}		f _{HCLK}	All peripherals enabled ⁽²⁾	All peripherals disabled	Unit
			24 MHz	12.8	9.3	
			16 MHz	9.3	6.6	
			8 MHz	5.1	3.9	
		Running on high-speed external clock with an	4 MHz	3.2	2.5	
		8 MHz crystal ⁽³⁾	2 MHz	2.1	1.75	
			1 MHz	1.55	1.4	
			500 kHz	1.3	1.2	
	Supply current in		125 kHz	1.1	1.05	mA
I _{DD}	Run mode		24 MHz	12.2	8.6	IIIA
			16 MHz	8.5	6	
			8 MHz	4.6	3.3	
		Running on high-speed	4 MHz	2.6	1.9	
		internal RC (HSI)	2 MHz	1.5	1.15	
			1 MHz	0.9	0.8	
			500 kHz	0.65	0.6	
			125 kHz	0.45	0.43	

^{1.} Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.

^{2.} Add an additional power consumption of 0.8 mA for the ADC and of 0.5 mA for the DAC analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).

^{3.} An 8 MHz crystal is used as the external clock source. The AHB prescaler is used to reduce the frequency when f_{HCLK} < 8 MHz, the PLL is used when f_{HCLK} > 8 MHz.

Low-speed external user clock generated from an external source

The characteristics given in *Table 20* result from tests performed using an low-speed external clock source, and under the ambient temperature and supply voltage conditions summarized in *Table 8*.

Symbol **Parameter Conditions** Min Тур Max Unit User external clock source 32.768 1000 kHz f_{LSE ext} frequency⁽¹⁾ OSC32 IN input pin high level $0.7V_{DD}$ V_{LSEH} V_{DD} voltage⁽¹⁾ V OSC32 IN input pin low level $0.3V_{DD}$ V_{ISFI} V_{SS} voltage⁽¹⁾ tw(LSEH) OSC32 IN high or low time⁽¹⁾ 450 t_{w(LSEL)} ns $t_{r(LSE)}$ OSC32 IN rise or fall time⁽¹⁾ 50 t_{f(LSE)} OSC32_IN input capacitance⁽¹⁾ C_{in(LSE)} 5 рF DuCy_(LSE) Duty cycle⁽¹⁾ 30 70 % OSC32 IN Input leakage current $V_{SS} \leq V_{IN} \leq V_{DD}$ ±1 μΑ I_{L}

Table 20. Low-speed external user clock characteristics

^{1.} Guaranteed by design.

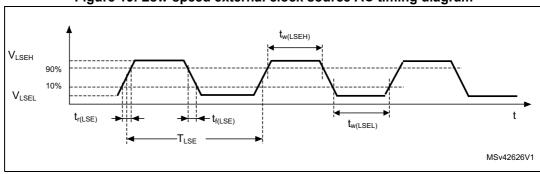


Figure 19. Low-speed external clock source AC timing diagram

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 21*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).



5.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = -40 to 105 $^{\circ}\text{C}$ unless otherwise specified.

Table 27. Flash memory characteristics

Symbol	Parameter	Conditions	Min ⁽¹⁾	Тур	Max ⁽¹⁾	Unit
t _{prog}	16-bit programming time	$T_A = -40 \text{ to } +105 ^{\circ}\text{C}$	40	52.5	70	μs
t _{ERASE}	Page (1 KB) erase time	$T_A = -40 \text{ to } +105 ^{\circ}\text{C}$	20	-	40	ms
t _{ME}	Mass erase time	$T_A = -40 \text{ to } +105 ^{\circ}\text{C}$	20	-	40	ms
		Read mode f _{HCLK} = 24 MHz, V _{DD} = 3.3 V	-	-	20	mA
I _{DD}	Supply current	Write / Erase modes f _{HCLK} = 24 MHz, V _{DD} = 3.3 V	-	-	5	mA
		Power-down mode / Halt, V _{DD} = 3.0 to 3.6 V	-	-	50	μΑ
V _{prog}	Programming voltage	-	2	-	3.6	V

^{1.} Guaranteed by design.

Table 28. Flash memory endurance and data retention

Symbol	Parameter Conditions			Unit		
Symbol	Farameter	Conditions	Min ⁽¹⁾	Тур	Max	Ollit
N _{END}	Endurance	$T_A = -40$ to +85 °C (6 suffix versions) $T_A = -40$ to +105 °C (7 suffix versions)	10	-	-	kcycles
		1 kcycle ⁽²⁾ at T _A = 85 °C	30	-	-	
t _{RET} Data retention		1 kcycle ⁽²⁾ at T _A = 105 °C	10	-	-	Years
		10 kcycles ⁽²⁾ at T_A = 55 °C	20	-	ı	

^{1.} Based on characterization not tested in production.

^{2.} Cycling performed over the whole temperature range.

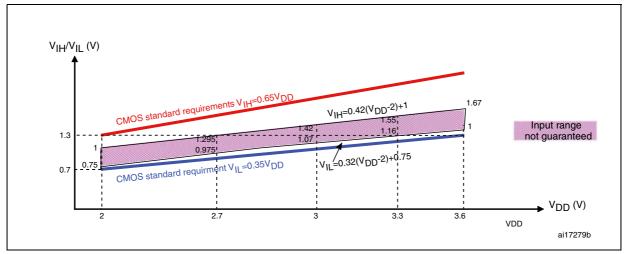
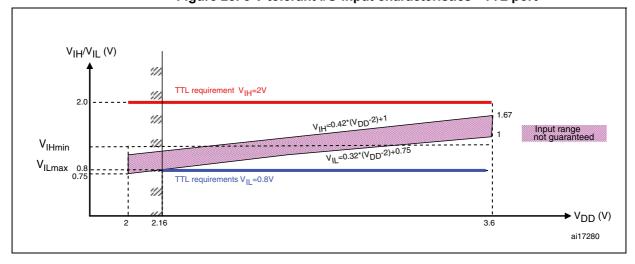


Figure 24. 5 V tolerant I/O input characteristics - CMOS port

Figure 25. 5 V tolerant I/O input characteristics - TTL port



Output driving current

The GPIOs (general-purpose inputs/outputs) can sink or source up to ± 8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OH}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on V_{DD} , plus the maximum Run consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating I_{VDD} (see *Table 6*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 6*).

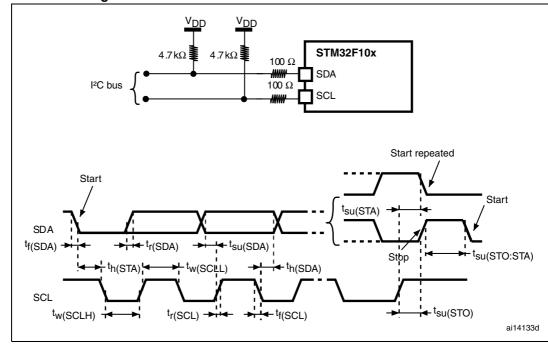


Figure 28. I²C bus AC waveforms and measurement circuit⁽¹⁾

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 40. SCL frequency (f_{PCLK1} = 24 MHz, V_{DD} = 3.3 V)⁽¹⁾⁽²⁾

f _{SCL} (kHz) ⁽³⁾	I2C_CCR value
ISCL (KIIZ)	$R_P = 4.7 \text{ k}\Omega$
400	0x8011
300	0x8016
200	0x8021
100	0x0064
50	0x00C8
20	0x01F4

^{1.} R_P = External pull-up resistance, f_{SCL} = I^2C speed,

^{2.} For speeds around 400 kHz, the tolerance on the achieved speed is of ±2%. For other speed ranges, the tolerance on the achieved speed ±1%. These variations depend on the accuracy of the external components used to design the application.

^{3.} Guaranteed by design.

5.3.18 DAC electrical specifications

Table 46. DAC characteristics

Symbol	Parameter	Min	Тур	Max ⁽¹⁾	Unit	Comments
V_{DDA}	Analog supply voltage	2.4	-	3.6	٧	-
V _{REF+}	Reference supply voltage	2.4	-	3.6	٧	V _{REF+} must always be below V _{DDA}
V _{SSA}	Ground	0	-	0	V	-
R _{LOAD} ⁽²⁾	Resistive load with buffer ON	5	-	-	kΩ	-
R _O ⁽¹⁾	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 M Ω
C _{LOAD} ⁽¹⁾	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at
DAC_OUT max ⁽¹⁾	Higher DAC_OUT voltage with buffer ON	ı	-	V _{DDA} – 0.2	٧	$V_{REF+} = 3.6 \text{ V and } (0x155) \text{ and } (0xEAB) \text{ at } V_{REF+} = 2.4 \text{ V}$
DAC_OUT min ⁽¹⁾	Lower DAC_OUT voltage with buffer OFF	ı	0.5	-	mV	It gives the maximum output
DAC_OUT max ⁽¹⁾	Higher DAC_OUT voltage with buffer OFF	-	-	V _{REF+} – 1LSB	V	excursion of the DAC.
I _{DDVREF+}	DAC DC current consumption in quiescent mode (Standby mode)	-	-	220	μA	With no load, worst code (0xF1C) at V _{REF+} = 3.6 V in terms of DC consumption on the inputs
		ı	-	380	μA	With no load, middle code (0x800) on the inputs
I _{DDA}	DAC DC current consumption in quiescent mode (Standby mode)	ı	1	480	μA	With no load, worst code (0xF1C) at V _{REF+} = 3.6 V in terms of DC consumption on the inputs
DNL ⁽¹⁾	Differential non linearity Difference between two	1	-	±0.5	LSB	Given for the DAC in 10-bit configuration
	consecutive code-1LSB)	1	-	±2	LSB	Given for the DAC in 12-bit configuration
INII (1)	Integral non linearity (difference between measured value at	ı	-	±1	LSB	Given for the DAC in 10-bit configuration
INL ⁽¹⁾	Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	±4	LSB	Given for the DAC in 12-bit configuration



Symbol	Parameter	Min	Тур	Max ⁽¹⁾	Unit	Comments	
Offset ⁽¹⁾	Offset error (difference between measured value at Code (0x800) and the ideal value = V _{REF+} /2)	-	-	±10	mV	Given for the DAC in 12-bit configuration	
		-	-	±3	LSB	Given for the DAC in 10-bit at V _{REF+} = 3.6 V	
		-	-	±12	LSB	Given for the DAC in 12-bit at V _{REF+} = 3.6 V	
Gain error ⁽¹⁾	Gain error	-	-	±0.5	%	Given for the DAC in 12bit configuration	
t _{SETTLING} ⁽¹⁾	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	-	3	4	μs	$C_{LOAD} \le 50 \text{ pF, } R_{LOAD} \ge 5 \text{ k}\Omega$	
Update rate ⁽¹⁾	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	ı	ı	1	MS/s	$C_{LOAD} \le 50 \text{ pF, } R_{LOAD} \ge 5 \text{ k}\Omega$	
t _{WAKEUP} (1)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	μs	$C_{LOAD} \le 50$ pF, $R_{LOAD} \ge 5$ k Ω input code between lowest and highest possible ones.	
PSRR+ (1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement	-	– 67	-40	dB	No R _{LOAD} , C _{LOAD} = 50 pF	

Table 46. DAC characteristics (continued)

- Guaranteed by characterization results.
- 2. Guaranteed by design.

Buffer(1)

Figure 36. 12-bit buffered /non-buffered DAC

Buffered/Non-buffered DAC R_L 12-bit digital to analog DAC_OUTx converter C_L ai17157V2

The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Table 48. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

Sumb a!		millimeters		inches ⁽¹⁾			
Symbol	Min	Тур	Max	Min	Тур	Max	
А	-	-	1.600	-	-	0.0630	
A1	0.050	-	0.150	0.0020	-	0.0059	
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571	
b	0.170	0.220	0.270	0.0067	0.0087	0.0106	
С	0.090	-	0.200	0.0035	-	0.0079	
D	15.800	16.000	16.200	0.6220	0.6299	0.6378	
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591	
D3	-	12.000	-	-	0.4724	-	
E	15.800	16.000	16.200	0.6220	0.6299	0.6378	
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591	
E3	-	12.000	-	-	0.4724	-	
е	-	0.500	-	-	0.0197	-	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295	
L1	-	1.000	-	-	0.0394	-	
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°	
ccc	-	-	0.080	-	-	0.0031	

^{1.} Values in inches are converted from mm and rounded to 4 decimal digits.



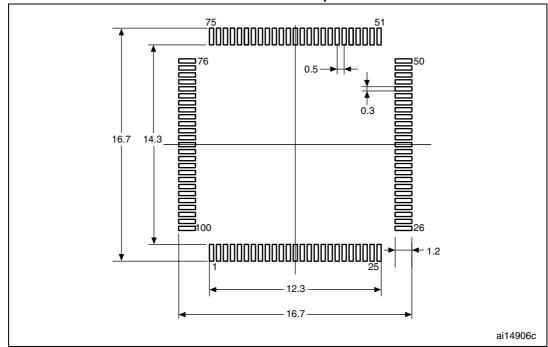


Figure 38. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint

1. Dimensions are in millimeters.

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6.2 LQFP64 package information

SEATING PLANE

O.25 mm

GAUGE PLANE

D1

D3

33

D3

TOTAL PLANE

D1

TOTAL PLANE

SW_ME_V3

Figure 40.LQFP64 - 10 x 10 mm 64 pin low-profile quad flat package outline

1. Drawing is not in scale.

Table 49. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

mechanical data								
Symbol		millimeters		inches ⁽¹⁾				
	Min	Тур	Max	Min	Тур	Max		
Α	-	-	1.600	-	-	0.0630		
A1	0.050	-	0.150	0.0020	-	0.0059		
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571		
b	0.170	0.220	0.270	0.0067	0.0087	0.0106		
С	0.090	-	0.200	0.0035	-	0.0079		
D	-	12.000	-	-	0.4724	-		
D1	-	10.000	-	-	0.3937	-		
D3	-	7.500	-	-	0.2953	-		
Е	-	12.000	-	-	0.4724	-		
E1	-	10.000	-	-	0.3937	-		
E3	-	7.500	-	-	0.2953	-		

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Device marking for TFBGA64

The following figure gives an example of topside marking and pin 1 position identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

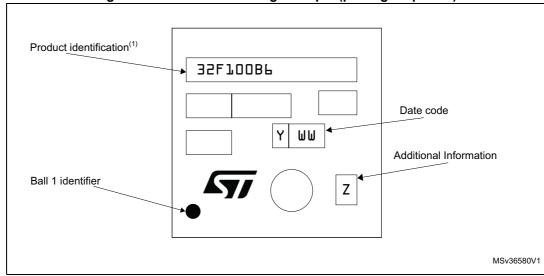


Figure 45. TFBGA64 marking example (package top view)

Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet
qualified and therefore not yet ready to be used in production and any consequences deriving from such
usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering
samples in production. ST Quality has to be contacted prior to any decision to use these Engineering
samples to run qualification activity.



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