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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f100v8t6btr

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F100x4, STM32F100x6, STM32F100x8 and STM32F100xB microcontrollers.

In the rest of the document, the STM32F100x4 and STM32F100x6 are referred to as low-density devices while the STM32F100x8 and STM32F100xB are identified as medium-density devices.

This STM32F100xx datasheet should be read in conjunction with the low- and medium-density STM32F100xx reference manual.
For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F100xx Flash programming manual.*
The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com.*

For information on the Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the www.arm.com website at the following address: http://infocenter.arm.com.

2.2 Overview

2.2.1 ARM® Cortex®-M3 core with embedded Flash and SRAM

The ARM® Cortex®-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex®-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F100xx value line family having an embedded ARM core, is therefore compatible with all ARM tools and software.

2.2.2 Embedded Flash memory

Up to 128 Kbytes of embedded Flash memory is available for storing programs and data.

2.2.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.2.4 Embedded SRAM

Up to 8 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.2.5 Nested vectored interrupt controller (NVIC)

The STM32F100xx value line embeds a nested vectored interrupt controller able to handle up to 41 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 2 V ≤V_{DD} ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

Table 6. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	-25	
$I_{INJ(PIN)}$(2)	Injected current on five volt tolerant pins(3)	-5 / +0	
	Injected current on any other pin(4)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See*Note: on page 70*.
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 5: Voltage characteristics* for the maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 5: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 7. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 8. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	24	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	24	
f_{PCLK2}	Internal APB2 clock frequency	-	0	24	
V_{DD}	Standard operating voltage	-	2	3.6	V
V_{DDA}(1)	Analog operating voltage (ADC not used)	Must be the same potential as V_{DD}	2	3.6	V
	Analog operating voltage (ADC used)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.8	3.6	V

Table 15. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)			Max		Unit
			V_{DD}/ V_{BAT} = 2.0 V	V_{DD}/ V_{BAT} = 2.4 V	V_{DD}/ V_{BAT} = 3.3 V	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in Run mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	23.5	24	190	350	µA
		Regulator in Low-Power mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	13.5	14	170	330	
	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog ON	-	2.6	3.4	-	-	
		Low-speed internal RC oscillator ON, independent watchdog OFF	-	2.4	3.2	-	-	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	-	1.7	2	4	5	
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	0.9	1.1	1.4	1.9	2.2	

1. Typical values are measured at T_A = 25 °C.

Figure 14. Typical current consumption on V_{BAT} with RTC on vs. temperature at different V_{BAT} values

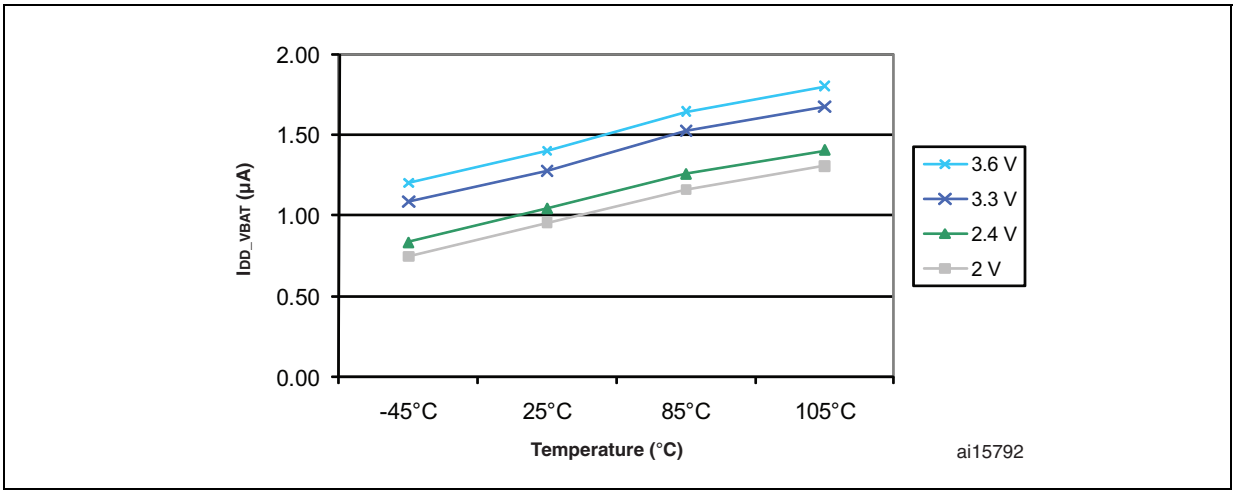
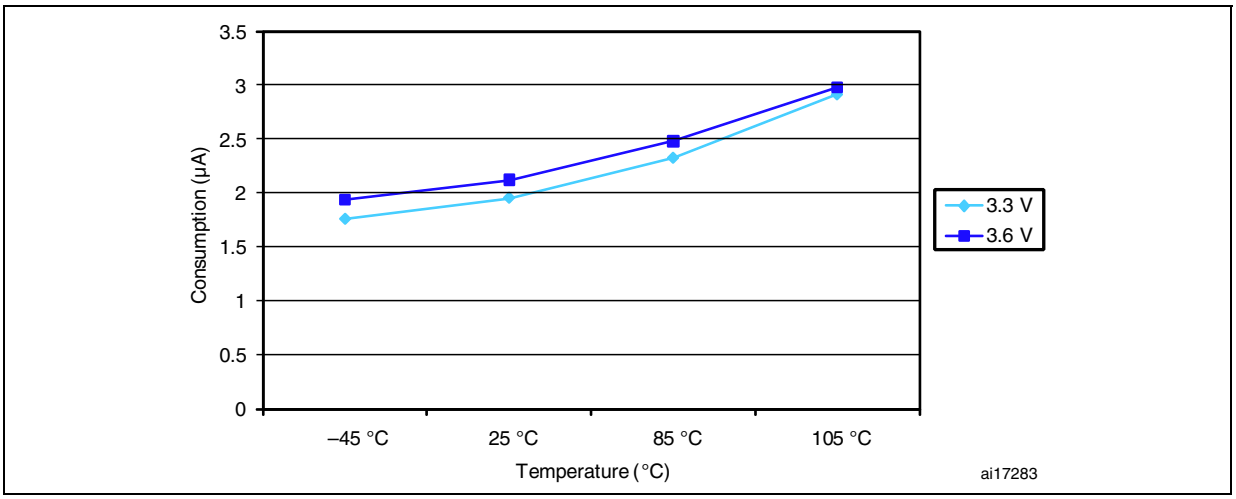


Figure 17. Typical current consumption in Standby mode versus temperature at V_{DD} = 3.3 V and 3.6 V



Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if it is explicitly mentioned
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK2} = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$

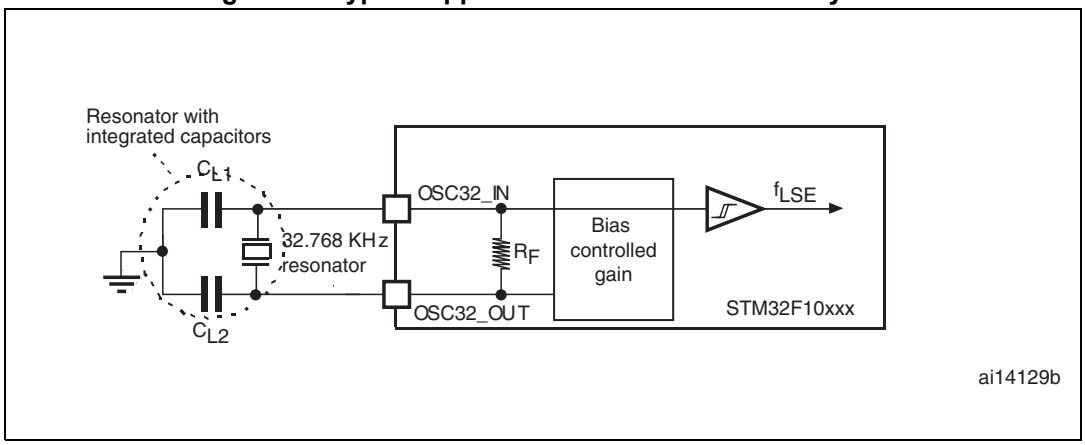
The parameters given in *Table 16* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 18. Peripheral current consumption(1)

Peripheral		Current consumption (µA/MHz)
AHB (up to 24MHz)	DMA1	22.92
	CRC	2,08
	BusMatrix(2)	4,17
APB1 (up to 24MHz)	APB1-Bridge	2,92
	TIM2	18,75
	TIM3	17,92
	TIM4	18,33
	TIM6	5,00
	TIM7	5,42
	SPI2/I2S2	4,17
	USART2	12,08
	USART3	12,92
	I2C1	10,83
	I2C2	10,83
	CEC	5,83
	DAC(3)	8,33
	WWDG	2,50
	PWR	2,50
	BKP	3,33
	IWDG	7,50
APB2 (up to 24MHz)	APB2-Bridge	3.75
	GPIOA	6,67
	GPIOB	6,25
	GPIOC	7,08
	GPIOD	6,67
	GPIOE	6,25
	SPI1	4,17
	USART1	11,67
	TIM1	22,92
	TIM15	14,58
	TIM16	11,67
	TIM17	10.83
	ADC1(4)	15.83

1. f_{HCLK} = 24 MHz, $f_{APB1} = f_{HCLK}$, fAPB2 = f_{HCLK}, default prescaler value for each peripheral.
2. The BusMatrix is automatically active when at least one master is ON.
3. When DAC_OUT1 or DAC_OU2 is enabled a current consumption equal to 0,5 mA must be added
4. Specific conditions for ADC: f_{HCLK} = 24 MHz, $f_{APB1} = f_{HCLK}$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/2$. When ADON bit in the ADC_CR2 register is set to 1, a current consumption equal to 0, 1mA must be added.

Figure 21. Typical application with a 32.768 kHz crystal



5.3.7 Internal clock source characteristics

The parameters given in *Table 23* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

High-speed internal (HSI) RC oscillator

Table 23. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
$DuCy_{(HSI)}$	Duty cycle	-	45	-	55	%
ACC_{HSI}	Accuracy of HSI oscillator	T_A = –40 to 105 °C(2)	-2.4	-	2.5	%
		T_A = –10 to 85 °C(2)	-2.2	-	1.3	%
		T_A = 0 to 70 °C(2)	-1.9	-	1.3	%
		T_A = 25 °C	-1	-	1	%
$t_{su(HSI)}$(3)	HSI oscillator startup time	-	1	-	2	µs
$I_{DD(HSI)}$(3)	HSI oscillator power consumption	-	-	80	100	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C °C unless otherwise specified.
2. Guaranteed by characterization results.
3. Guaranteed by design. Not tested in production

5.3.8 PLL characteristics

The parameters given in *Table 26* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 26. PLL characteristics

Symbol	Parameter	Value			Unit
		Min(1)	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)	1	8.0	24	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	24	MHz
t_{LOCK}	PLL lock time	-	-	200	µs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

1. Guaranteed by characterization results.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (Electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 29*. They are based on the EMS levels and classes defined in application note AN1709.

Table 29. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 24 MHz, LQFP100 package, conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 24 MHz, LQFP100 package, conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second. To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Figure 24. 5 V tolerant I/O input characteristics - CMOS port

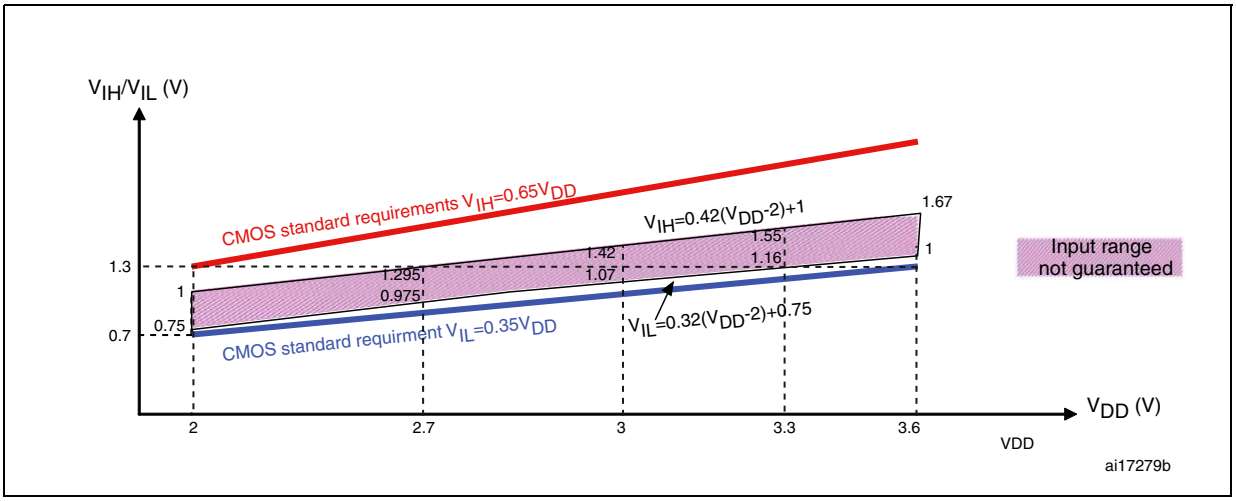
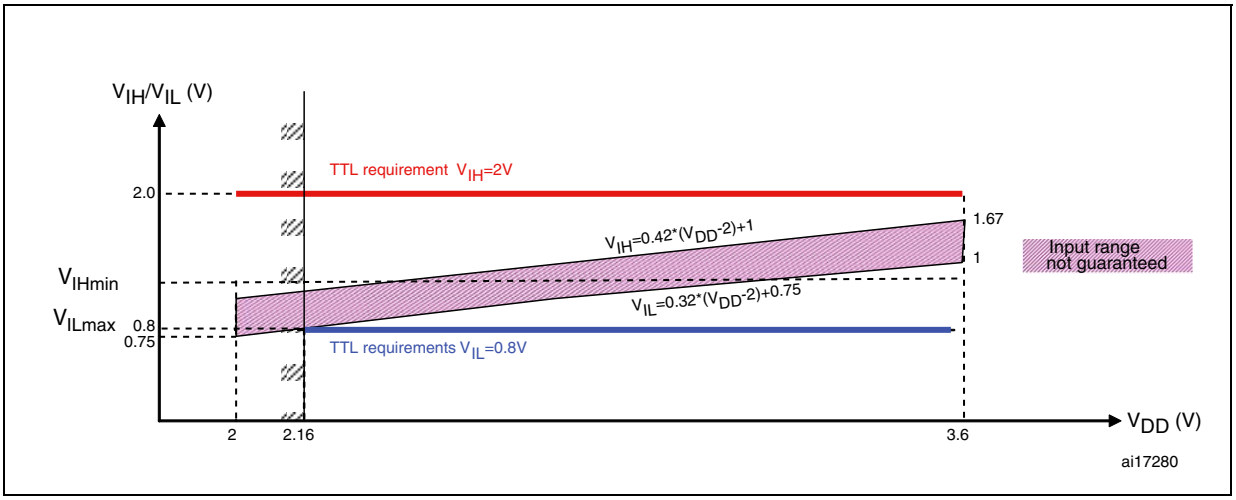


Figure 25. 5 V tolerant I/O input characteristics - TTL port



Output driving current

The GPIOs (general-purpose inputs/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see *Table 6*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 6*).

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 26* and *Table 36*, respectively.

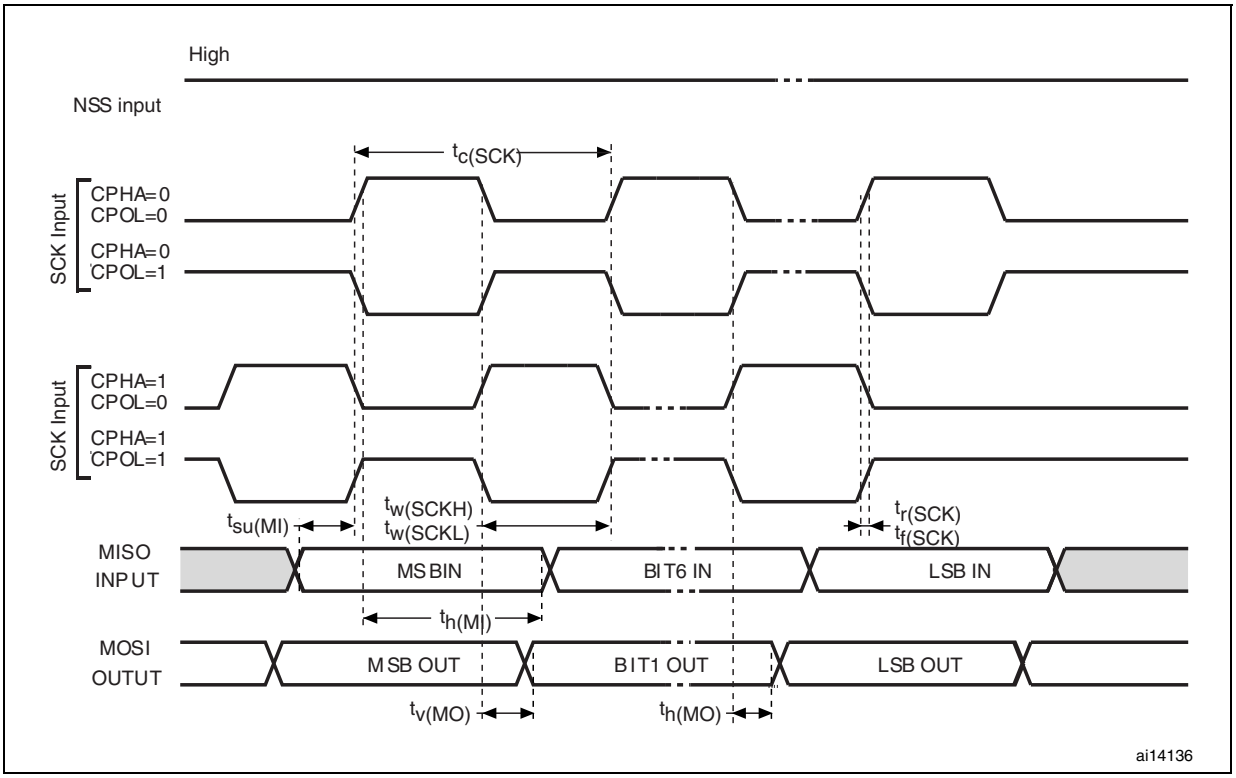
Unless otherwise specified, the parameters given in *Table 36* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 36. I/O AC characteristics(1)

MODEx [1:0] bit value(1)	Symbol	Parameter	Conditions	Max	Unit
10	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	2(3)	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L= 50 pF, V_{DD} = 2 V to 3.6 V	10(3)	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L= 50 pF, V_{DD} = 2 V to 3.6 V	25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		25(3)	
11	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	24	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	12(3)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10(3)	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 26*.
3. Guaranteed by design.

Figure 31. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

HDMI consumer electronics control (CEC)

Refer to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics.

5.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 42* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 8*.

Note: It is recommended to perform a calibration after each power-up.

Table 42. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
I_{VREF}	Current on the V_{REF} input pin	-	-	160(1)	220(1)	µA
f_{ADC}	ADC clock frequency	-	0.6	-	12	MHz
f_S(2)	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 12 MHz	-	-	705	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}(3)	Conversion voltage range	-	0 (V_{SSA} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* and *Table 43* for details	-	-	50	kΩ
R_{ADC}(2)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 12 MHz	6.9			µs
		-	83			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 12 MHz	-	-	0.25	µs
		-	-	-	3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 12 MHz	-	-	0.166	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 12 MHz	0.125	-	20.0	µs
			1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	0	0	1	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 12 MHz	1.17	-	21	µs
		-	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Based on characterization results, not tested in production.
2. Guaranteed by design.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Table 4: Low & medium-density STM32F100xx pin definitions* and *Figure 6* for further details.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 42*.

Equation 1: R_{AIN} max formula:

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above formula (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 48. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Using the values obtained in *Table 53* T_{Jmax} is calculated as follows:

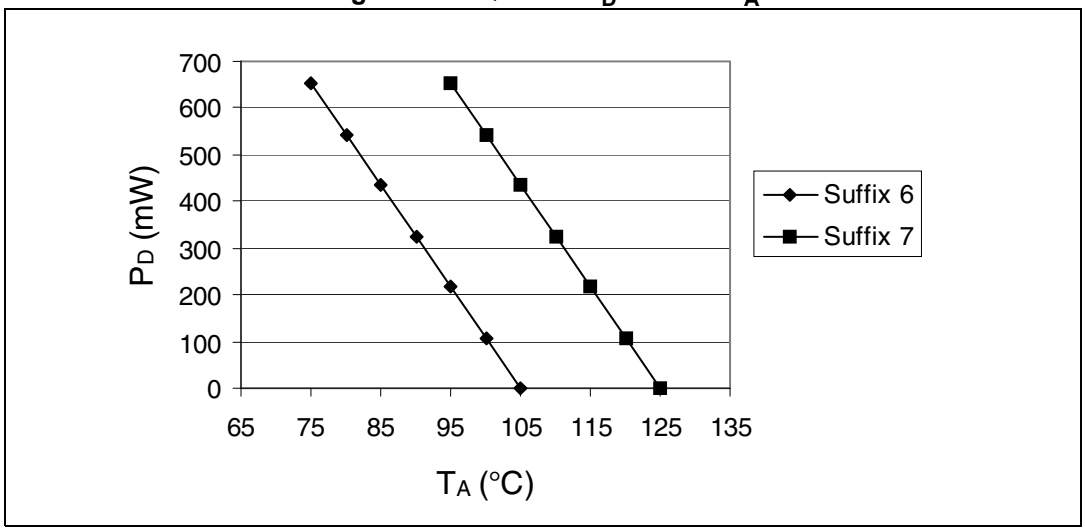
– For LQFP100, 46 °C/W

T_{Jmax} = 115 °C + (46 °C/W × 134 mW) = 115 °C + 6.2 °C = 121.2 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Table 54: Ordering information scheme*).

Figure 49. LQFP100 P_D max vs. T_A



7 Ordering information scheme

Table 54. Ordering information scheme

Example: STM32 F 100 C 6 T 6 B xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Device subfamily

100 = value line

Pin count

C = 48 pins

R = 64 pins

V = 100 pins

Flash memory size

4 = 16 Kbytes of Flash memory

6 = 32 Kbytes of Flash memory

8 = 64 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

Package

T = LQFP

H = BGA

Temperature range

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

Internal code

B

Options

xxx = programmed parts

TR = tape and real

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

8 Revision history

Table 55. Document revision history

Date	Revision	Changes
12-Oct-2009	1	Initial release.
26-Feb-2010	2	TFBGA64 package added (see *Table 50* and *Table 41*). *Note 5* modified in *Table 4: Low & medium-density STM32F100xx pin definitions*. $I_{INJ(PIN)}$ modified in *Table 6: Current characteristics*. Conditions removed from *Table 25: Low-power mode wakeup timings*. Notes modified in *Table 34: I/O static characteristics*. *Figure 27: Recommended NRST pin protection* modified. Note modified in *Table 39: I2C characteristics*. *Figure 28: I2C bus AC waveforms and measurement circuit(1)* modified. *Table 46: DAC characteristics* modified. *Figure 36: 12-bit buffered /non-buffered DAC* added. *TIM2, TIM3, TIM4* and *TIM15, TIM16 and TIM17* updated. HDMI-CEC electrical characteristics added. Values added to: – *Table 12: Maximum current consumption in Run mode, code with data processing running from Flash* – *Table 13: Maximum current consumption in Run mode, code with data processing running from RAM* – *Table 14: Maximum current consumption in Sleep mode, code running from Flash or RAM* – *Table 15: Typical and maximum current consumptions in Stop and Standby modes* – *Table 18: Peripheral current consumption* – *Table 29: EMS characteristics* – *Table 30: EMI characteristics* – *Table 47: TS characteristics* *Section 5.3.12: I/O current injection characteristics* modified. Added figures: – *Figure 12: Maximum current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled* – *Figure 13: Maximum current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled* – *Figure 15: Typical current consumption in Stop mode with regulator in Run mode versus temperature at VDD = 3.3 V and 3.6 V* – *Figure 16: Typical current consumption in Stop mode with regulator in Low-power mode versus temperature at VDD = 3.3 V and 3.6 V* – *Figure 17: Typical current consumption in Standby mode versus temperature at VDD = 3.3 V and 3.6 V*

Table 55. Document revision history (continued)

Date	Revision	Changes
08-Jun-2012	7	Updated *Table 6: Current characteristics on page 34* Updated *Table 39: I2C characteristics on page 64* Corrected note “non-robust “ in *Section 5.3.17: 12-bit ADC characteristics on page 68* Updated *Section 5.3.13: I/O port characteristics on page 57* Updated *Section 2.2.20: GPIOs (general-purpose inputs/outputs) on page 20* Updated *Table 4: Low & medium-density STM32F100xx pin definitions on page 24* Updated *Section 5.3.1: General operating conditions on page 34* Updated *Table 14: Maximum current consumption in Sleep mode, code running from Flash or RAM on page 39*
08-Jun-2015	8	Updated *Table 18: Peripheral current consumption*, *Table 31: ESD absolute maximum ratings*, *Table 48: LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data*, *Table 49: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data*, *Table 50: TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package mechanical data*, *Table 51: TFBGA64 recommended PCB design rules (0.5 mm pitch BGA)* and *Table 52: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data*. Updated *Figure 37: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline*, *Figure 38: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint*, *Figure 40: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline*, *Figure 41: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint*, *Figure 43: TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch thin profile fine pitch ball grid array package outline*, *Figure 44: TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array, recommended footprint*, *Figure 46: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline* and *Figure 47: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint*. Added *Figure 39: LQFP100 marking example (package top view)*, *Figure 42: LQFP64 marking example (package top view) Figure 45: TFBGA64 marking example (package top view)* and *Figure 48: LQFP48 marking example (package top view)*.
21-Nov-2016	9	Updated: – *Figure 7: Memory map* – *Figure 18: High-speed external clock source AC timing diagram* – *Figure 19: Low-speed external clock source AC timing diagram* – *Table 19: High-speed external user clock characteristics* – *Table 20: Low-speed external user clock characteristics* – *Table 42: ADC characteristics*