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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f100vbt6b

Contents

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F100x4, STM32F100x6, STM32F100x8 and STM32F100xB microcontrollers.

In the rest of the document, the STM32F100x4 and STM32F100x6 are referred to as low-density devices while the STM32F100x8 and STM32F100xB are identified as medium-density devices.

This STM32F100xx datasheet should be read in conjunction with the low- and medium-density STM32F100xx reference manual.
For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F100xx Flash programming manual.*
The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com.*

For information on the Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the www.arm.com website at the following address: http://infocenter.arm.com.

2.2.6 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 18 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 80 GPIOs can be connected to the 16 external interrupt lines.

2.2.7 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-24 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the APB domains is 24 MHz.

2.2.8 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1. For further details please refer to AN2606.

2.2.9 Power supply schemes

- V_{DD} = 2.0 to 3.6 V: External power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: External analog power supplies for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC or DAC is used).
  V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8 to 3.6 V: Power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

2.2.10 Power supply supervisor

The device has an integrated power on reset (POR)/power down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, DAC, I^2C, USART, all timers and ADC.

2.2.14 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are ten 16-bit registers used to store 20 bytes of user application data when V_{DD} power is not present.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the high-speed external clock divided by 128. The internal low power RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural crystal deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.2.15 Timers and watchdogs

The STM32F100xx devices include an advanced-control timer, six general-purpose timers, two basic timers and two watchdog timers.

Table 3 compares the features of the advanced-control, general-purpose and basic timers.

Table 3. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
TIM2, TIM3, TIM4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	Yes
TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	Yes
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Table 4. Low & medium-density STM32F100xx pin definitions (continued)

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3)(4)	
LQFP100	LQFP64	TFBGA64	LQFP48					Default	Remap
57	-	-	-	PD10	I/O	FT	PD10	-	USART3_CK
58	-	-	-	PD11	I/O	FT	PD11	-	USART3_CTS
59	-	-	-	PD12	I/O	FT	PD12	-	TIM4_CH1(11) / USART3_RTS
60	-	-	-	PD13	I/O	FT	PD13	-	TIM4_CH2(11)
61	-	-	-	PD14	I/O	FT	PD14	-	TIM4_CH3(11)
62	-	-	-	PD15	I/O	FT	PD15	-	TIM4_CH4(11)
63	37	F6	-	PC6	I/O	FT	PC6	-	TIM3_CH1
64	38	E7	-	PC7	I/O	FT	PC7	-	TIM3_CH2
65	39	E8	-	PC8	I/O	FT	PC8	-	TIM3_CH3
66	40	D8	-	PC9	I/O	FT	PC9	-	TIM3_CH4
67	41	D7	29	PA8	I/O	FT	PA8	USART1_CK / MCO / TIM1_CH1	-
68	42	C7	30	PA9	I/O	FT	PA9	USART1_TX(12) / TIM1_CH2 / TIM15_BKIN	-
69	43	C6	31	PA10	I/O	FT	PA10	USART1_RX(12) / TIM1_CH3 / TIM17_BKIN	-
70	44	C8	32	PA11	I/O	FT	PA11	USART1_CTS / TIM1_CH4	-
71	45	B8	33	PA12	I/O	FT	PA12	USART1_RTS / TIM1_ETR	-
72	46	A8	34	PA13	I/O	FT	JTMS-SWDIO	-	PA13
73	-	-	-	Not connected					-
74	47	D5	35	V_{SS_2}	S	-	V_{SS_2}	-	-
75	48	E5	36	V_{DD_2}	S	-	V_{DD_2}	-	-
76	49	A7	37	PA14	I/O	FT	JTCK/SWCLK	-	PA14
77	50	A6	38	PA15	I/O	FT	JTDI	-	TIM2_CH1_ETR/ PA15/ SPI1_NSS
78	51	B7	-	PC10	I/O	FT	PC10	-	USART3_TX

Table 4. Low & medium-density STM32F100xx pin definitions (continued)

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3)(4)	
LQFP100	LQFP64	TFBGA64	LQFP48					Default	Remap
79	52	B6	-	PC11	I/O	FT	PC11	-	USART3_RX
80	53	C5	-	PC12	I/O	FT	PC12	-	USART3_CK
81	-	C1	-	PD0	I/O	FT	PD0	-	-
82	-	D1	-	PD1	I/O	FT	PD1	-	-
83	54	B5	-	PD2	I/O	FT	PD2	TIM3_ETR	-
84	-	-	-	PD3	I/O	FT	PD3	-	USART2_CTS
85	-	-	-	PD4	I/O	FT	PD4	-	USART2_RTS
86	-	-	-	PD5	I/O	FT	PD5	-	USART2_TX
87	-	-	-	PD6	I/O	FT	PD6	-	USART2_RX
88	-	-	-	PD7	I/O	FT	PD7	-	USART2_CK
89	55	A5	39	PB3	I/O	FT	JTDO		TIM2_CH2 / PB3 TRACESWO SPI1_SCK
90	56	A4	40	PB4	I/O	FT	NJTRST	-	PB4 / TIM3_CH1 SPI1_MISO
91	57	C4	41	PB5	I/O	-	PB5	I2C1_SMBA / TIM16_BKIN	TIM3_CH2 / SPI1_MOSI
92	58	D3	42	PB6	I/O	FT	PB6	I2C1_SCL(12)/ TIM4_CH1(11)(12) TIM16_CH1N	USART1_TX
93	59	C3	43	PB7	I/O	FT	PB7	I2C1_SDA(12)/ TIM17_CH1N TIM4_CH2(11)(12)	USART1_RX
94	60	B4	44	BOOT0	I	-	BOOT0	-	-
95	61	B3	45	PB8	I/O	FT	PB8	TIM4_CH3(11)(12) / TIM16_CH1(12) / CEC(12)	I2C1_SCL
96	62	A3	46	PB9	I/O	FT	PB9	TIM4_CH4(11)(12) / TIM17_CH1(12)	I2C1_SDA
97	-	-	-	PE0	I/O	FT	PE0	TIM4_ETR(11)	-
98	-	-	-	PE1	I/O	FT	PE1	-	-
99	63	D4	47	V_{SS_3}	S	-	V_{SS_3}	-	-
100	64	E4	48	V_{DD_3}	S	-	V_{DD_3}	-	-

Table 10. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	V
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	V
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8(1)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$(2)	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(2)	Reset temporization	-	1.5	2.5	4.5	ms

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design.

Table 18. Peripheral current consumption(1)

Peripheral		Current consumption (µA/MHz)
AHB (up to 24MHz)	DMA1	22.92
	CRC	2,08
	BusMatrix(2)	4,17
APB1 (up to 24MHz)	APB1-Bridge	2,92
	TIM2	18,75
	TIM3	17,92
	TIM4	18,33
	TIM6	5,00
	TIM7	5,42
	SPI2/I2S2	4,17
	USART2	12,08
	USART3	12,92
	I2C1	10,83
	I2C2	10,83
	CEC	5,83
	DAC(3)	8,33
	WWDG	2,50
	PWR	2,50
	BKP	3,33
	IWDG	7,50
APB2 (up to 24MHz)	APB2-Bridge	3.75
	GPIOA	6,67
	GPIOB	6,25
	GPIOC	7,08
	GPIOD	6,67
	GPIOE	6,25
	SPI1	4,17
	USART1	11,67
	TIM1	22,92
	TIM15	14,58
	TIM16	11,67
	TIM17	10.83
	ADC1(4)	15.83

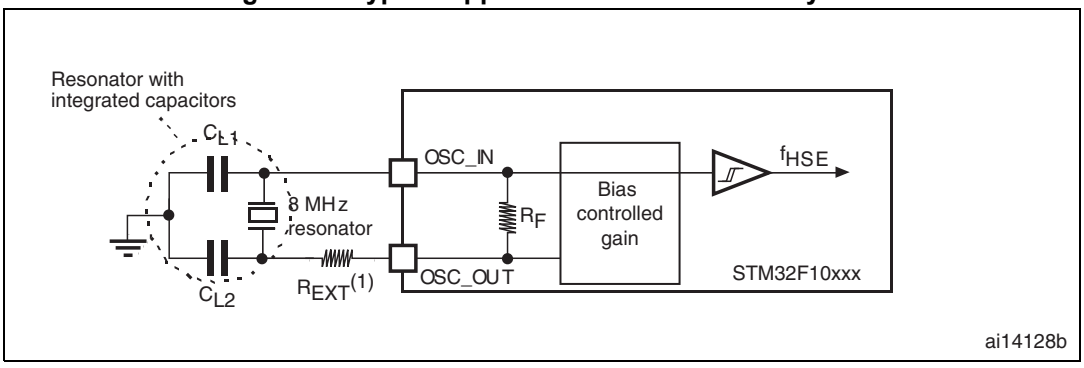
1. f_{HCLK} = 24 MHz, $f_{APB1} = f_{HCLK}$, fAPB2 = f_{HCLK}, default prescaler value for each peripheral.
2. The BusMatrix is automatically active when at least one master is ON.
3. When DAC_OUT1 or DAC_OU2 is enabled a current consumption equal to 0,5 mA must be added
4. Specific conditions for ADC: f_{HCLK} = 24 MHz, $f_{APB1} = f_{HCLK}$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/2$. When ADON bit in the ADC_CR2 register is set to 1, a current consumption equal to 0, 1mA must be added.

Table 21. HSE 4-24 MHz oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	24	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
C_{L1} C_{L2}(3)	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(4)	R_S = 30 Ω	-	30	-	pF
i_2	HSE driving current	V_{DD} = 3.3 V V_{IN} = V_{SS} with 30 pF load	-	-	1	mA
g_m	Oscillator transconductance	Startup	25	-	-	mA/V
$t_{SU(HSE)}$ (5)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results.
3. It is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.
4. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
5. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Figure 20. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

5.3.8 PLL characteristics

The parameters given in *Table 26* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

Table 26. PLL characteristics

Symbol	Parameter	Value			Unit
		Min(1)	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)	1	8.0	24	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	24	MHz
t_{LOCK}	PLL lock time	-	-	200	µs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

1. Guaranteed by characterization results.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 30. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/24 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25°C, LQFP100 package compliant with SAE J1752/3	0.1 MHz to 30 MHz	9	dBµV
			30 MHz to 130 MHz	16	
			130 MHz to 1GHz	19	
			SAE EMI Level	4	-

5.3.11 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 31. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to JESD22-C101	III	500	

1. Based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD78 IC latch-up standard.

Table 32. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78	II level A

5.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

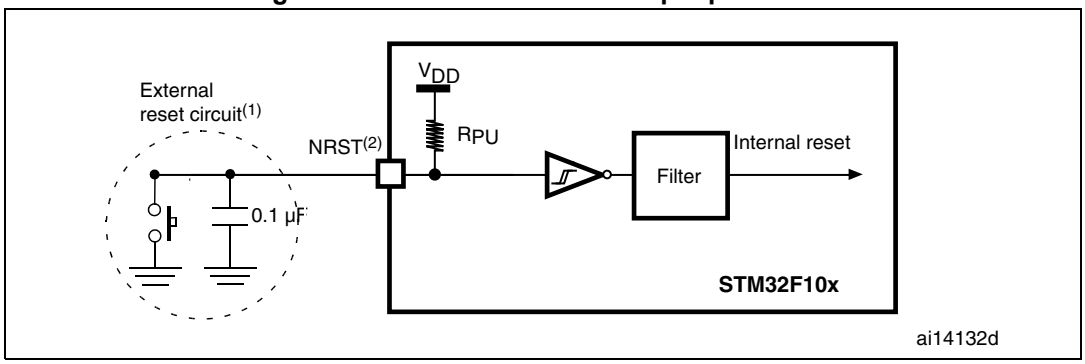
The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 33*

Table 33. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	-0	+0	mA
	Injected current on all FT pins	-5	+0	
	Injected current on any other pin	-5	+5	

Figure 27. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 37*. Otherwise the reset will not be taken into account by the device.

5.3.15 TIMx characteristics

The parameters given in *Table 38* are guaranteed by design.

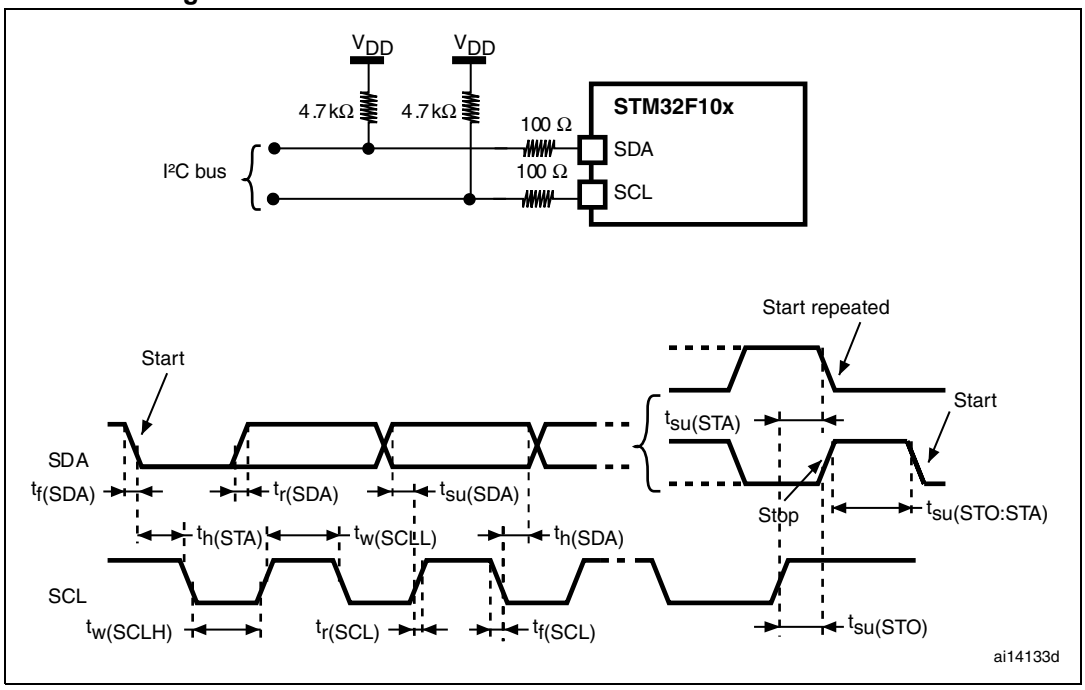
Refer to *Section 5.3.12: I/O current injection characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 38. TIMx characteristics

Symbol	Parameter	Conditions(1)	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 24 MHz	41.7	-	ns
f_{EXT}	Timer external clock frequency on CHx(2)		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 24 MHz	0	12	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock period when the internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 24 MHz	-	2730	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 24 MHz	-	178	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3, TIM4, TIM15, TIM16 and TIM17 timers.
2. CHx is used as a general term to refer to CH1 to CH4 for TIM1, TIM2, TIM3 and TIM4, to the CH1 to CH2 for TIM15, and to CH1 for TIM16 and TIM17.

Figure 28. I²C bus AC waveforms and measurement circuit(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 40. SCL frequency (f_{PCLK1}= 24 MHz, V_{DD} = 3.3 V)(1)(2)

f_{SCL} (kHz)(3)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x8011
300	0x8016
200	0x8021
100	0x0064
50	0x00C8
20	0x01F4

1. R_P = External pull-up resistance, f_{SCL} = I²C speed,
2. For speeds around 400 kHz, the tolerance on the achieved speed is of ±2%. For other speed ranges, the tolerance on the achieved speed ±1%. These variations depend on the accuracy of the external components used to design the application.
3. Guaranteed by design.

Table 43. R_{AIN} max for f_{ADC} = 12 MHz(1)

T_s (cycles)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.125	0.4
7.5	0.625	5.9
13.5	1.125	11.4
28.5	2.375	25.2
41.5	3.45	37.2
55.5	4.625	50
71.5	5.96	NA
239.5	20	NA

1. Guaranteed by design.

Table 44. ADC accuracy - limited test conditions(1)(2)

Symbol	Parameter	Test conditions	Typ	Max	Unit
ET	Total unadjusted error	f_{PCLK2} = 24 MHz, f_{ADC} = 12 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3 V to 3.6 V V_{REF+} = V_{DDA} T_A = 25 °C Measurements made after ADC calibration	±1.3	±2.2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	

1. ADC DC accuracy values are measured after internal calibration.
2. Guaranteed by characterization results.

Table 45. ADC accuracy(1) (2) (3)

Symbol	Parameter	Test conditions	Typ	Max	Unit
ET	Total unadjusted error	f_{PCLK2} = 24 MHz, f_{ADC} = 12 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V T_A = Full operating range Measurements made after ADC calibration	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted V_{DD}, frequency, V_{REF} and temperature ranges.
3. Guaranteed by characterization results.

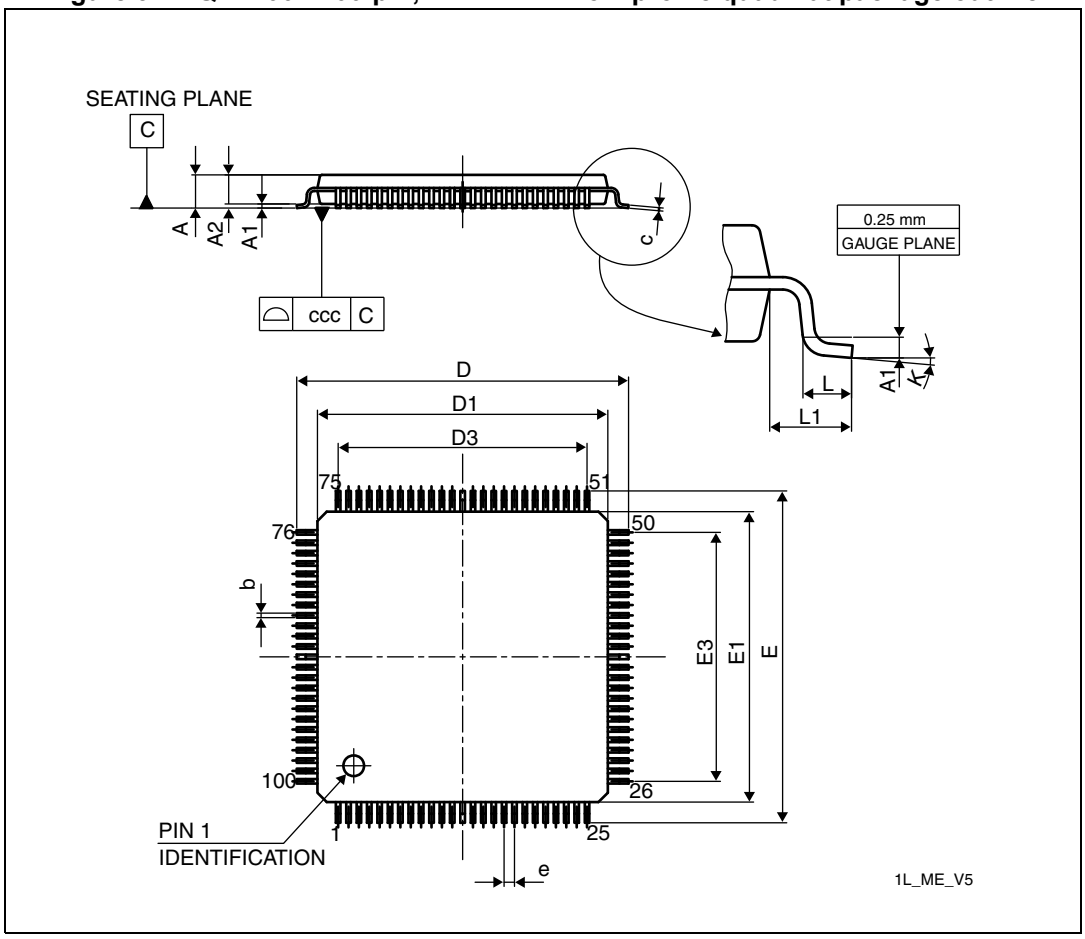
Note: ADC accuracy vs. negative injection current: Injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.12* does not affect the ADC accuracy.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

6.1 LQFP100 package information

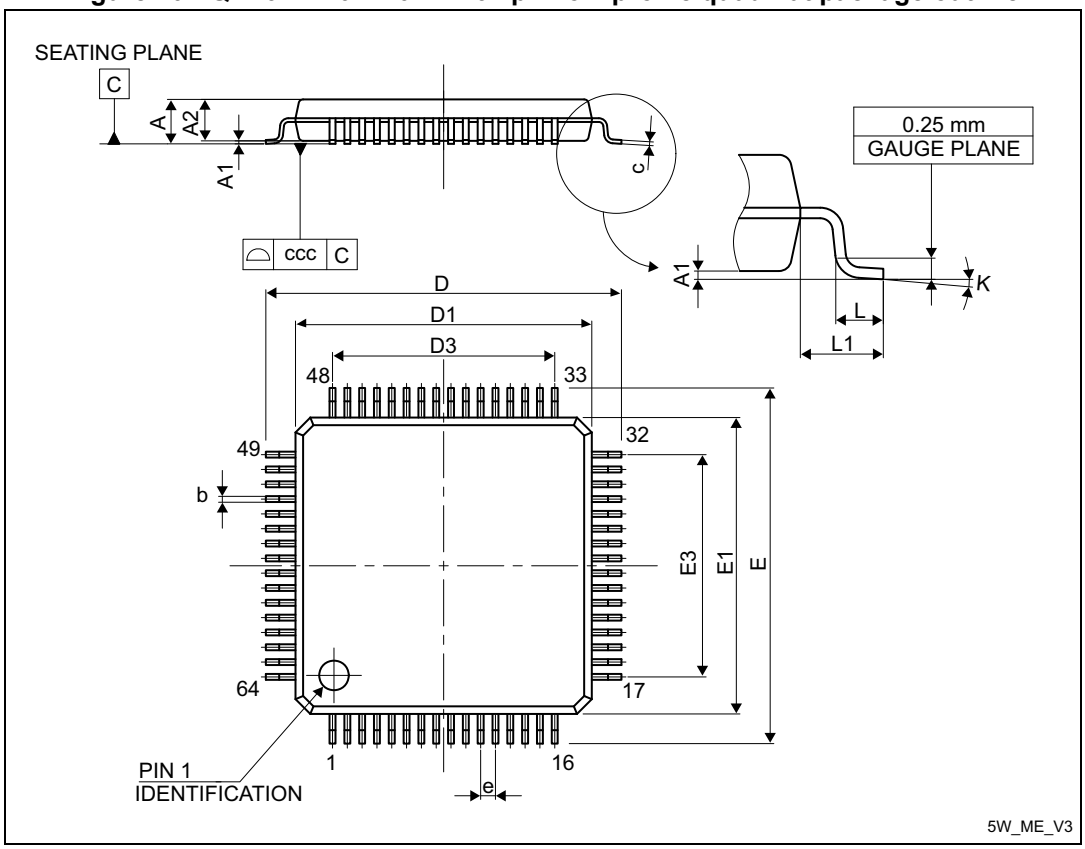
Figure 37. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale. Dimensions are in millimeters.

6.2 LQFP64 package information

Figure 40.LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline



1. Drawing is not in scale.

Table 49. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

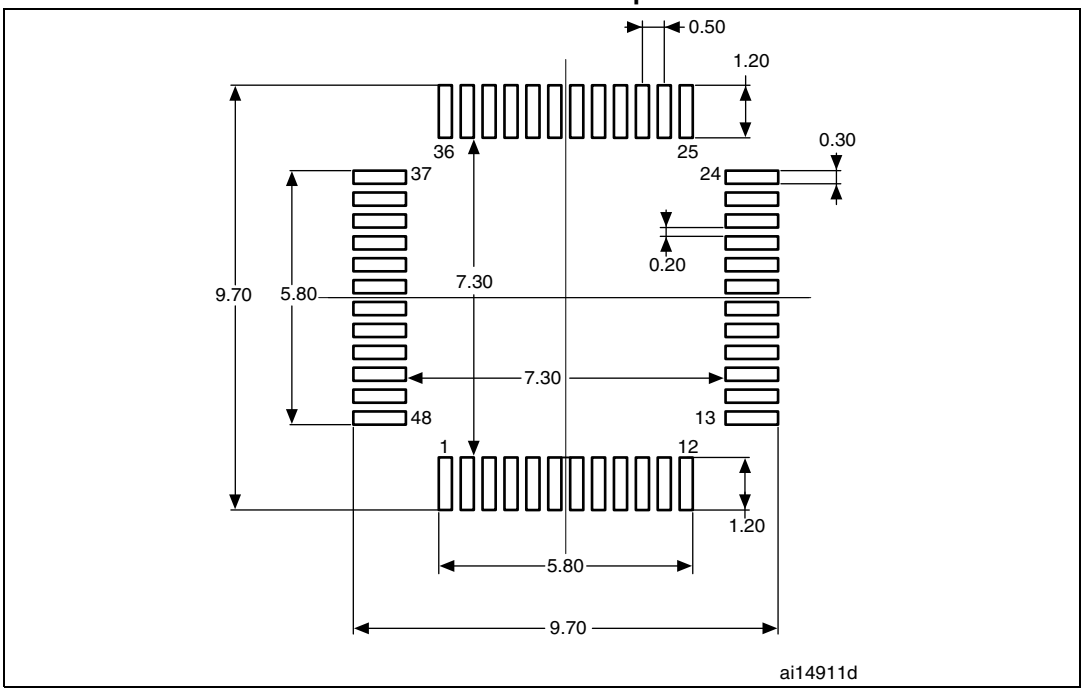
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-

Table 52. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 47. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Using the values obtained in *Table 53* T_{Jmax} is calculated as follows:

– For LQFP100, 46 °C/W

T_{Jmax} = 115 °C + (46 °C/W × 134 mW) = 115 °C + 6.2 °C = 121.2 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Table 54: Ordering information scheme*).

Figure 49. LQFP100 P_D max vs. T_A

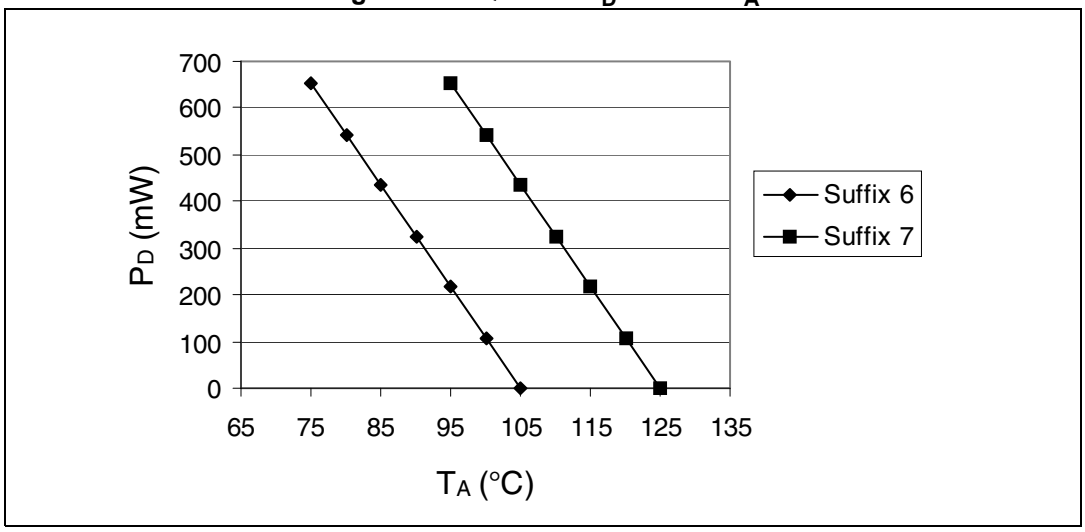


Table 55. Document revision history (continued)

Date	Revision	Changes
08-Jun-2012	7	Updated *Table 6: Current characteristics on page 34* Updated *Table 39: I2C characteristics on page 64* Corrected note “non-robust “ in *Section 5.3.17: 12-bit ADC characteristics on page 68* Updated *Section 5.3.13: I/O port characteristics on page 57* Updated *Section 2.2.20: GPIOs (general-purpose inputs/outputs) on page 20* Updated *Table 4: Low & medium-density STM32F100xx pin definitions on page 24* Updated *Section 5.3.1: General operating conditions on page 34* Updated *Table 14: Maximum current consumption in Sleep mode, code running from Flash or RAM on page 39*
08-Jun-2015	8	Updated *Table 18: Peripheral current consumption*, *Table 31: ESD absolute maximum ratings*, *Table 48: LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data*, *Table 49: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data*, *Table 50: TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package mechanical data*, *Table 51: TFBGA64 recommended PCB design rules (0.5 mm pitch BGA)* and *Table 52: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data*. Updated *Figure 37: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline*, *Figure 38: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint*, *Figure 40: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline*, *Figure 41: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint*, *Figure 43: TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch thin profile fine pitch ball grid array package outline*, *Figure 44: TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array, recommended footprint*, *Figure 46: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline* and *Figure 47: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint*. Added *Figure 39: LQFP100 marking example (package top view)*, *Figure 42: LQFP64 marking example (package top view) Figure 45: TFBGA64 marking example (package top view)* and *Figure 48: LQFP48 marking example (package top view)*.
21-Nov-2016	9	Updated: – *Figure 7: Memory map* – *Figure 18: High-speed external clock source AC timing diagram* – *Figure 19: Low-speed external clock source AC timing diagram* – *Table 19: High-speed external user clock characteristics* – *Table 20: Low-speed external user clock characteristics* – *Table 42: ADC characteristics*