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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f100vbt6btr">https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f100vbt6btr</a>

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# 1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F100x4, STM32F100x6, STM32F100x8 and STM32F100xB microcontrollers.

In the rest of the document, the STM32F100x4 and STM32F100x6 are referred to as low-density devices while the STM32F100x8 and STM32F100xB are identified as medium-density devices.

This STM32F100xx datasheet should be read in conjunction with the low- and medium-density STM32F100xx reference manual.

For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F100xx Flash programming manual*.

The reference and Flash programming manuals are both available from the STMicroelectronics website [www.st.com](http://www.st.com).

For information on the Cortex<sup>®</sup>-M3 core please refer to the Cortex<sup>®</sup>-M3 Technical Reference Manual, available from the [www.arm.com](http://www.arm.com) website at the following address:  
<http://infocenter.arm.com>.



### Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard TIM timers which have the same architecture. The advanced control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

### General-purpose timers (TIM2, TIM3, TIM4, TIM15, TIM16 & TIM17)

There are six synchronizable general-purpose timers embedded in the STM32F100xx devices (see [Table 3](#) for differences). Each general-purpose timers can be used to generate PWM outputs, or as simple time base.

#### TIM2, TIM3, TIM4

STM32F100xx devices feature three synchronizable 4-channels general-purpose timers. These timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2, TIM3, TIM4 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2, TIM3, TIM4 all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

#### TIM15, TIM16 and TIM17

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate with TIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16, and TIM17 have a complementary output with dead-time generation and independent DMA request generation

Their counters can be frozen in debug mode.

### Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

### Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

### Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

### SysTick timer

This timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

## 2.2.16 I<sup>2</sup>C bus

The I<sup>2</sup>C bus interface can operate in multimaster and slave modes. It can support standard and fast modes.

It supports dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

The interface can be served by DMA and it supports SM Bus 2.0/PM Bus.

## 2.2.17 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F100xx value line embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

The available USART interfaces communicate at up to 3 Mbit/s. They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode and have LIN Master/Slave capability.

The USART interfaces can be served by the DMA controller.

### 2.2.18 Serial peripheral interface (SPI)

Up to two SPIs are able to communicate up to 12 Mbit/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits.

Both SPIs can be served by the DMA controller.

### 2.2.19 HDMI (high-definition multimedia interface) consumer electronics control (CEC)

The STM32F100xx value line embeds a HDMI-CEC controller that provides hardware support of consumer electronics control (CEC) (Appendix supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead.

### 2.2.20 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

### 2.2.21 Remap capability

This feature allows the use of a maximum number of peripherals in a given application. Indeed, alternate functions are available not only on the default pins but also on other specific pins onto which they are remappable. This has the advantage of making board design and port usage much more flexible.

For details refer to [Table 4: Low & medium-density STM32F100xx pin definitions](#); it shows the list of remappable alternate functions and the pins onto which they can be remapped. See the STM32F10xxx reference manual for software considerations.

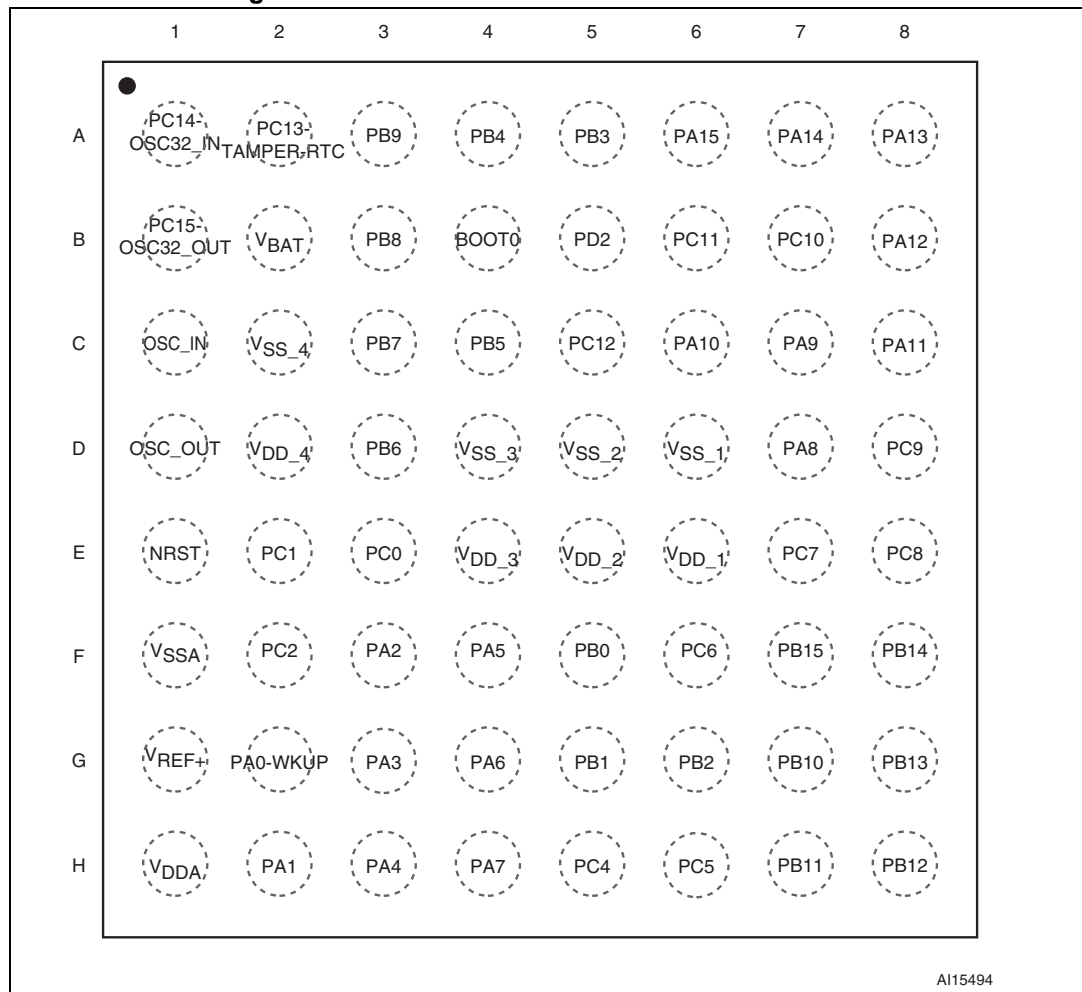
### 2.2.22 ADC (analog-to-digital converter)

The 12-bit analog to digital converter has up to 16 external channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

Figure 6. STM32F100xx value line TFBGA64 ballout



AI15494

Table 4. Low &amp; medium-density STM32F100xx pin definitions

Pins				Pin name	Type <sup>(1)</sup>	I / O level <sup>(2)</sup>	Main function <sup>(3)</sup> (after reset)	Alternate functions <sup>(3)(4)</sup>	
LQFP100	LQFP64	TFBGA64	LQFP48					Default	Remap
1	-	-	-	PE2	I/O	FT	PE2	TRACECLK	-
2	-	-	-	PE3	I/O	FT	PE3	TRACED0	-
3	-	-	-	PE4	I/O	FT	PE4	TRACED1	-
4	-	-	-	PE5	I/O	FT	PE5	TRACED2	-
5	-	-	-	PE6	I/O	FT	PE6	TRACED3	-
6	1	B2	1	V <sub>BAT</sub>	S	-	V <sub>BAT</sub>	-	-
7	2	A2	2	PC13-TAMPER-RTC <sup>(5)</sup>	I/O	-	PC13 <sup>(6)</sup>	TAMPER-RTC	-
8	3	A1	3	PC14-OSC32_IN <sup>(5)</sup>	I/O	-	PC14 <sup>(6)</sup>	OSC32_IN	-

Table 4. Low &amp; medium-density STM32F100xx pin definitions (continued)

Pins				Pin name	Type <sup>(1)</sup>	I / O level <sup>(2)</sup>	Main function <sup>(3)</sup> (after reset)	Alternate functions <sup>(3)(4)</sup>	
LQFP100	LQFP64	TFBGA64	LQFP48					Default	Remap
33	24	H5	-	PC4	I/O	-	PC4	ADC1_IN14	-
34	25	H6	-	PC5	I/O	-	PC5	ADC1_IN15	-
35	26	F5	18	PB0	I/O	-	PB0	ADC1_IN8/TIM3_CH3 <sup>(12)</sup>	TIM1_CH2N
36	27	G5	19	PB1	I/O	-	PB1	ADC1_IN9/TIM3_CH4 <sup>(12)</sup>	TIM1_CH3N
37	28	G6	20	PB2	I/O	FT	PB2/BOOT1	-	-
38	-	-	-	PE7	I/O	FT	PE7	-	TIM1_ETR
39	-	-	-	PE8	I/O	FT	PE8	-	TIM1_CH1N
40	-	-	-	PE9	I/O	FT	PE9	-	TIM1_CH1
41	-	-	-	PE10	I/O	FT	PE10	-	TIM1_CH2N
42	-	-	-	PE11	I/O	FT	PE11	-	TIM1_CH2
43	-	-	-	PE12	I/O	FT	PE12	-	TIM1_CH3N
44	-	-	-	PE13	I/O	FT	PE13	-	TIM1_CH3
45	-	-	-	PE14	I/O	FT	PE14	-	TIM1_CH4
46	-	-	-	PE15	I/O	FT	PE15	-	TIM1_BKIN
47	29	G7	21	PB10	I/O	FT	PB10	I2C2_SCL <sup>(9)</sup> /USART3_TX <sup>(12)</sup>	TIM2_CH3 / HDMI_CEC
48	30	H7	22	PB11	I/O	FT	PB11	I2C2_SDA <sup>(9)</sup> /USART3_RX <sup>(12)</sup>	TIM2_CH4
49	31	D6	23	V <sub>SS_1</sub>	S	-	V <sub>SS_1</sub>	-	-
50	32	E6	24	V <sub>DD_1</sub>	S	-	V <sub>DD_1</sub>	-	-
51	33	H8	25	PB12	I/O	FT	PB12	SPI2_NSS <sup>(10)</sup> / I2C2_SMBA <sup>(9)</sup> / TIM1_BKIN <sup>(12)</sup> /USART3_CK <sup>(12)</sup>	-
52	34	G8	26	PB13	I/O	FT	PB13	SPI2_SCK <sup>(10)</sup> / TIM1_CH1N <sup>(12)</sup> / USART3_CTS <sup>(12)</sup>	-
53	35	F8	27	PB14	I/O	FT	PB14	SPI2_MISO <sup>(10)</sup> / TIM1_CH2N <sup>(12)</sup> / USART3_RTS <sup>(12)</sup>	TIM15_CH1
54	36	F7	28	PB15	I/O	FT	PB15	SPI2_MOSI <sup>(10)</sup> / TIM1_CH3N / TIM15_CH1N <sup>(12)</sup>	TIM15_CH2
55	-	-	-	PD8	I/O	FT	PD8	-	USART3_TX
56	-	-	-	PD9	I/O	FT	PD9	-	USART3_RX



1. I = input, O = output, S = supply, HiZ= high impedance.
2. FT= 5 V tolerant.
3. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripherals that is included. For example, if a device has only one SPI, two USARTs and two timers, they will be called SPI1, USART1 & USART2 and TIM2 & TIM 3, respectively. Refer to [Table 2 on page 11](#).
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch and since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is restricted: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must *not* be used as a current source (e.g. to drive an LED).
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: [www.st.com](http://www.st.com).
7. The pins number 2 and 3 in the VFQFPN36 package, 5 and 6 in the LQFP48 and LQFP64 packages and C1 and C2 in the TFBGA64 package are configured as OSC\_IN/OSC\_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.
8. Unlike in the LQFP64 package, there is no PC3 in the TFBGA64 package. The V<sub>REF+</sub> functionality is provided instead.
9. I2C2 is not present on low-density value line devices.
10. SPI2 is not present on low-density value line devices.
11. TIM4 is not present on low-density value line devices.
12. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: [www.st.com](http://www.st.com).

# 4 Memory mapping

The memory map is shown in [Figure 7](#).

Figure 7. Memory map

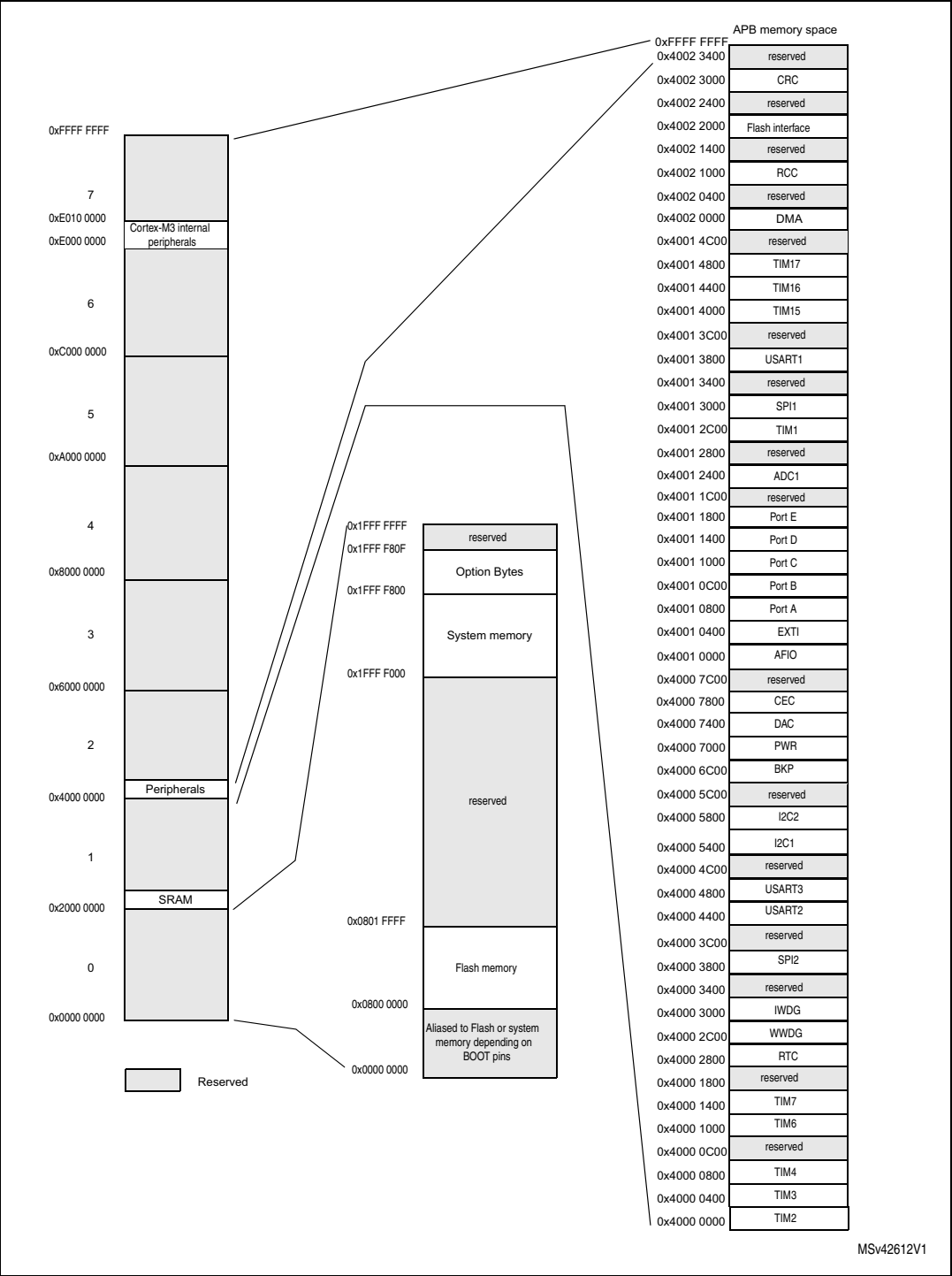


Table 10. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{PVD}$	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	V
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	V
$V_{PVDhyst}^{(2)}$	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8 <sup>(1)</sup>	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}^{(2)}$	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}^{(2)}$	Reset temporization	-	1.5	2.5	4.5	ms

1. The product behavior is guaranteed by design down to the minimum  $V_{POR/PDR}$  value.

2. Guaranteed by design.

**Table 12. Maximum current consumption in Run mode, code with data processing running from Flash**

Symbol	Parameter	Conditions	$f_{HCLK}$	Max <sup>(1)</sup>		Unit
				$T_A = 85\text{ °C}$	$T_A = 105\text{ °C}$	
$I_{DD}$	Supply current in Run mode	External clock <sup>(2)</sup> , all peripherals enabled	24 MHz	15.4	15.7	mA
			16 MHz	11	11.5	
			8 MHz	6.7	6.9	
		External clock <sup>(2)</sup> , all peripherals disabled	24 MHz	10.3	10.5	
			16 MHz	7.8	8.1	
			8 MHz	5.1	5.3	

1. Guaranteed by characterization results.

2. External clock is 8 MHz and PLL is on when  $f_{HCLK} > 8\text{ MHz}$ .

**Table 13. Maximum current consumption in Run mode, code with data processing running from RAM**

Symbol	Parameter	Conditions	$f_{HCLK}$	Max <sup>(1)</sup>		Unit
				$T_A = 85\text{ °C}$	$T_A = 105\text{ °C}$	
$I_{DD}$	Supply current in Run mode	External clock <sup>(2)</sup> , all peripherals enabled	24 MHz	14.5	15	mA
			16 MHz	10	10.5	
			8 MHz	6	6.3	
		External clock <sup>(2)</sup> all peripherals disabled	24MHz	9.3	9.7	
			16 MHz	6.8	7.2	
			8 MHz	4.4	4.7	

1. Guaranteed by characterization, tested in production at  $V_{DD}$  max,  $f_{HCLK}$  max.

2. External clock is 8 MHz and PLL is on when  $f_{HCLK} > 8\text{ MHz}$ .

Table 15. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ <sup>(1)</sup>			Max		Unit
			$V_{DD}/V_{BAT} = 2.0\text{ V}$	$V_{DD}/V_{BAT} = 2.4\text{ V}$	$V_{DD}/V_{BAT} = 3.3\text{ V}$	$T_A = 85\text{ °C}$	$T_A = 105\text{ °C}$	
$I_{DD}$	Supply current in Stop mode	Regulator in Run mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	23.5	24	190	350	$\mu\text{A}$
		Regulator in Low-Power mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	13.5	14	170	330	
	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog ON	-	2.6	3.4	-	-	
		Low-speed internal RC oscillator ON, independent watchdog OFF	-	2.4	3.2	-	-	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	-	1.7	2	4	5	
$I_{DD\_VBAT}$	Backup domain supply current	Low-speed oscillator and RTC ON	0.9	1.1	1.4	1.9	2.2	

1. Typical values are measured at  $T_A = 25\text{ °C}$ .

Figure 14. Typical current consumption on  $V_{BAT}$  with RTC on vs. temperature at different  $V_{BAT}$  values

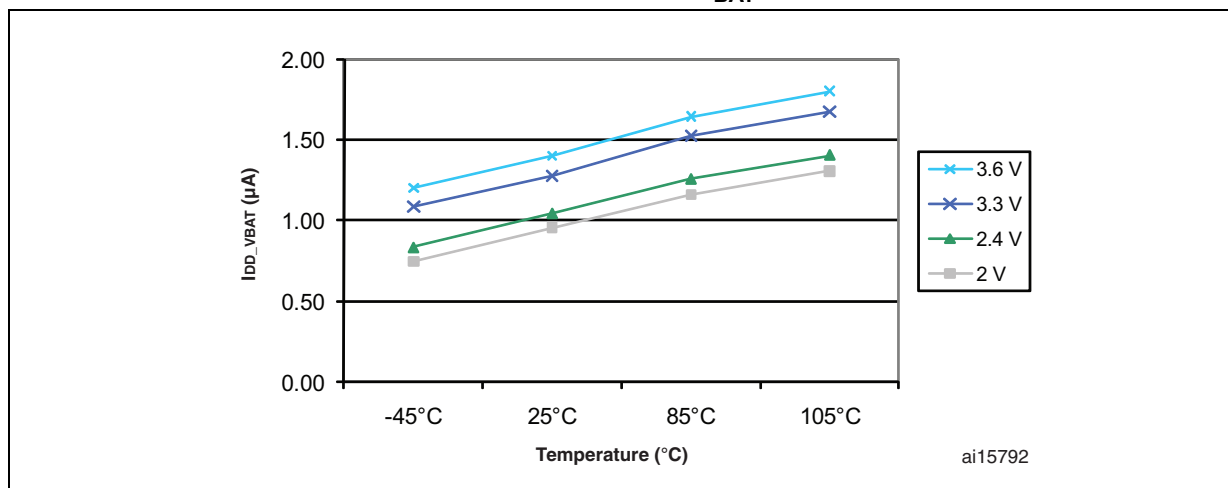


Table 18. Peripheral current consumption<sup>(1)</sup>

Peripheral		Current consumption ( $\mu\text{A}/\text{MHz}$ )
AHB (up to 24MHz)	DMA1	22,92
	CRC	2,08
	BusMatrix <sup>(2)</sup>	4,17
APB1 (up to 24MHz)	APB1-Bridge	2,92
	TIM2	18,75
	TIM3	17,92
	TIM4	18,33
	TIM6	5,00
	TIM7	5,42
	SPI2/I2S2	4,17
	USART2	12,08
	USART3	12,92
	I2C1	10,83
	I2C2	10,83
	CEC	5,83
	DAC <sup>(3)</sup>	8,33
	WWDG	2,50
	PWR	2,50
	BKP	3,33
	IWDG	7,50
APB2 (up to 24MHz)	APB2-Bridge	3,75
	GPIOA	6,67
	GPIOB	6,25
	GPIOC	7,08
	GPIOD	6,67
	GPIOE	6,25
	SPI1	4,17
	USART1	11,67
	TIM1	22,92
	TIM15	14,58
	TIM16	11,67
	TIM17	10,83
	ADC1 <sup>(4)</sup>	15,83

1.  $f_{\text{HCLK}} = 24 \text{ MHz}$ ,  $f_{\text{APB1}} = f_{\text{HCLK}}$ ,  $f_{\text{APB2}} = f_{\text{HCLK}}$ , default prescaler value for each peripheral.

2. The BusMatrix is automatically active when at least one master is ON.

3. When DAC\_OUT1 or DAC\_OUT2 is enabled a current consumption equal to 0,5 mA must be added

4. Specific conditions for ADC:  $f_{\text{HCLK}} = 24 \text{ MHz}$ ,  $f_{\text{APB1}} = f_{\text{HCLK}}$ ,  $f_{\text{APB2}} = f_{\text{HCLK}}$ ,  $f_{\text{ADCCLK}} = f_{\text{APB2}}/2$ . When ADON bit in the ADC\_CR2 register is set to 1, a current consumption equal to 0, 1mA must be added.

### Low-speed external user clock generated from an external source

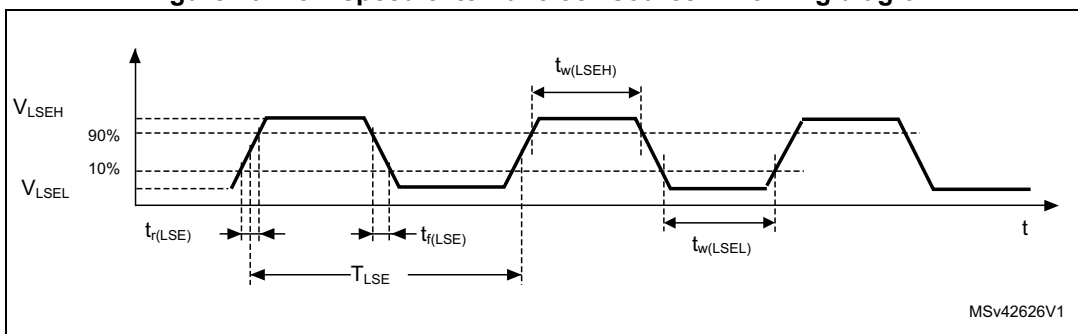
The characteristics given in [Table 20](#) result from tests performed using an low-speed external clock source, and under the ambient temperature and supply voltage conditions summarized in [Table 8](#).

**Table 20. Low-speed external user clock characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{LSE\_ext}$	User external clock source frequency <sup>(1)</sup>	-	-	32.768	1000	kHz
$V_{LSEH}$	OSC32_IN input pin high level voltage <sup>(1)</sup>		$0.7V_{DD}$	-	$V_{DD}$	V
$V_{LSEL}$	OSC32_IN input pin low level voltage <sup>(1)</sup>		$V_{SS}$	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time <sup>(1)</sup>		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time <sup>(1)</sup>		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance <sup>(1)</sup>		-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle <sup>(1)</sup>		30	-	70	%
$I_L$	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	$\pm 1$	$\mu A$

1. Guaranteed by design.

**Figure 19. Low-speed external clock source AC timing diagram**



### High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 21](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

### 5.3.9 Memory characteristics

#### Flash memory

The characteristics are given at  $T_A = -40$  to  $+105$  °C unless otherwise specified.

**Table 27. Flash memory characteristics**

Symbol	Parameter	Conditions	Min <sup>(1)</sup>	Typ	Max <sup>(1)</sup>	Unit
$t_{\text{prog}}$	16-bit programming time	$T_A = -40$ to $+105$ °C	40	52.5	70	µs
$t_{\text{ERASE}}$	Page (1 KB) erase time	$T_A = -40$ to $+105$ °C	20	-	40	ms
$t_{\text{ME}}$	Mass erase time	$T_A = -40$ to $+105$ °C	20	-	40	ms
$I_{\text{DD}}$	Supply current	Read mode $f_{\text{HCLK}} = 24$ MHz, $V_{\text{DD}} = 3.3$ V	-	-	20	mA
		Write / Erase modes $f_{\text{HCLK}} = 24$ MHz, $V_{\text{DD}} = 3.3$ V	-	-	5	mA
		Power-down mode / Halt, $V_{\text{DD}} = 3.0$ to $3.6$ V	-	-	50	µA
$V_{\text{prog}}$	Programming voltage	-	2	-	3.6	V

1. Guaranteed by design.

**Table 28. Flash memory endurance and data retention**

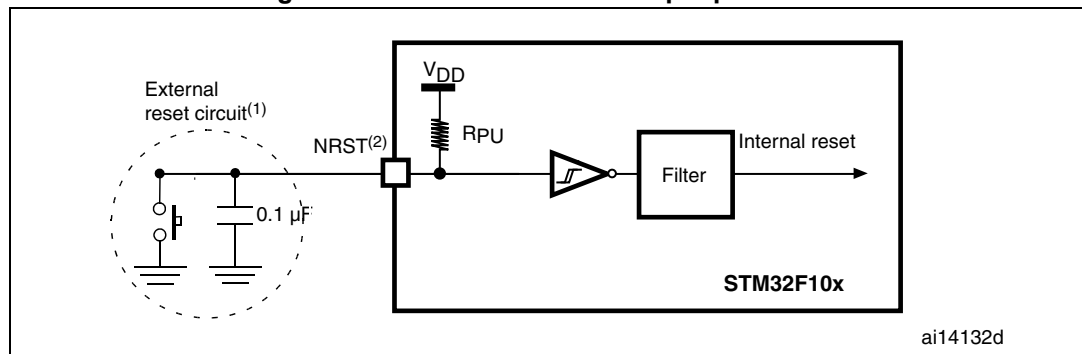
Symbol	Parameter	Conditions	Value			Unit
			Min <sup>(1)</sup>	Typ	Max	
$N_{\text{END}}$	Endurance	$T_A = -40$ to $+85$ °C (6 suffix versions) $T_A = -40$ to $+105$ °C (7 suffix versions)	10	-	-	kcycles
$t_{\text{RET}}$	Data retention	1 kcycle <sup>(2)</sup> at $T_A = 85$ °C	30	-	-	Years
		1 kcycle <sup>(2)</sup> at $T_A = 105$ °C	10	-	-	
		10 kcycles <sup>(2)</sup> at $T_A = 55$ °C	20	-	-	

1. Based on characterization not tested in production.

2. Cycling performed over the whole temperature range.



Figure 27. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the  $V_{IL(NRST)}$  max level specified in [Table 37](#). Otherwise the reset will not be taken into account by the device.

### 5.3.15 TIMx characteristics

The parameters given in [Table 38](#) are guaranteed by design.

Refer to [Section 5.3.12: I/O current injection characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 38. TIMx characteristics

Symbol	Parameter	Conditions <sup>(1)</sup>	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 24 \text{ MHz}$	41.7	-	ns
$f_{EXT}$	Timer external clock frequency on CHx <sup>(2)</sup>	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK} = 24 \text{ MHz}$	0	12	MHz
$Res_{TIM}$	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock period when the internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 24 \text{ MHz}$	-	2730	µs
$t_{MAX\_COUNT}$	Maximum possible count	-	-	$65536 \times 65536$	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 24 \text{ MHz}$	-	178	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3, TIM4, TIM15, TIM16 and TIM17 timers.
2. CHx is used as a general term to refer to CH1 to CH4 for TIM1, TIM2, TIM3 and TIM4, to the CH1 to CH2 for TIM15, and to CH1 for TIM16 and TIM17.

### 5.3.19 Temperature sensor characteristics

Table 47. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	$V_{SENSE}$ linearity with temperature	-	$\pm 1$	$\pm 2$	$^{\circ}\text{C}$
Avg_Slope <sup>(1)</sup>	Average slope	4.0	4.3	4.6	mV/ $^{\circ}\text{C}$
$V_{25}^{(1)}$	Voltage at 25 $^{\circ}\text{C}$	1.32	1.41	1.50	V
$t_{START}^{(2)}$	Startup time	4	-	10	$\mu\text{s}$
$T_{S\_temp}^{(3)(2)}$	ADC sampling time when reading the temperature	-	-	17.1	$\mu\text{s}$

1. Guaranteed by characterization results.

2. Guaranteed by design.

3. Shortest sampling time can be determined in the application by multiple iterations.

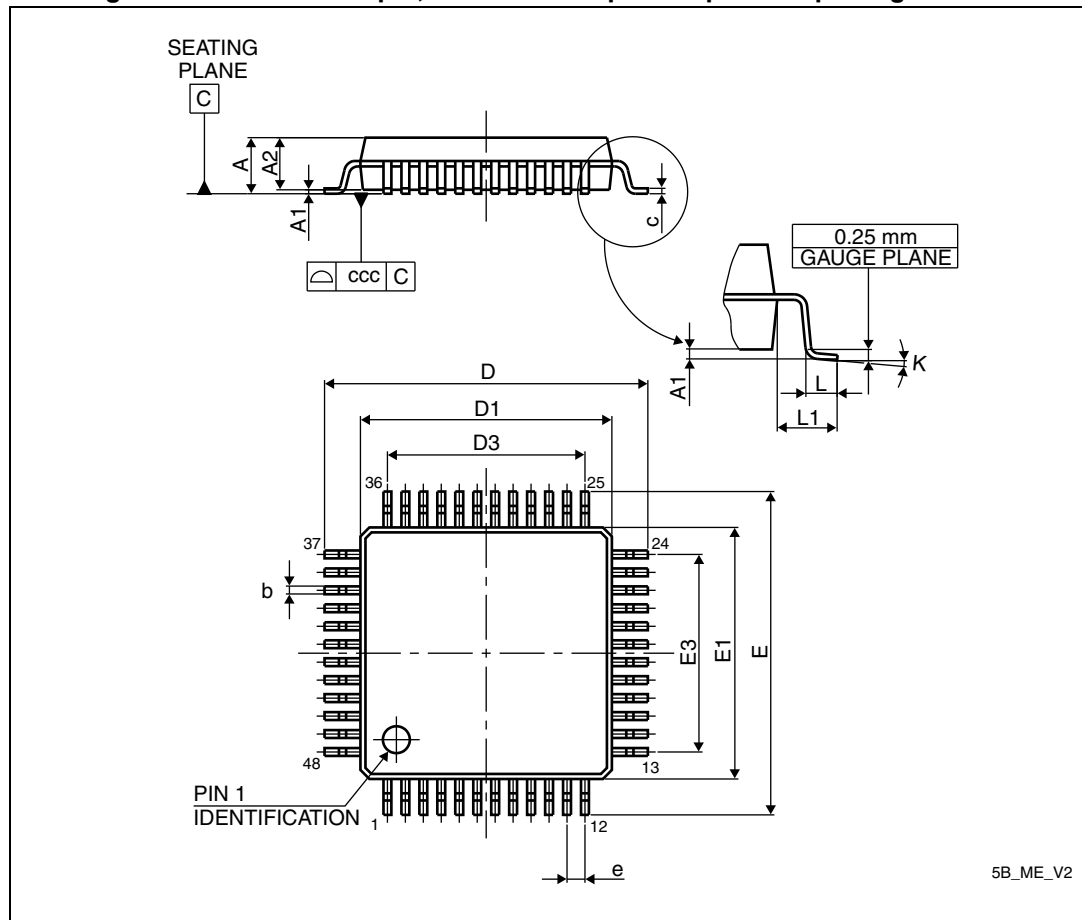
Table 48. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

## 6.4 LQFP48 package information

Figure 46. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 52. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

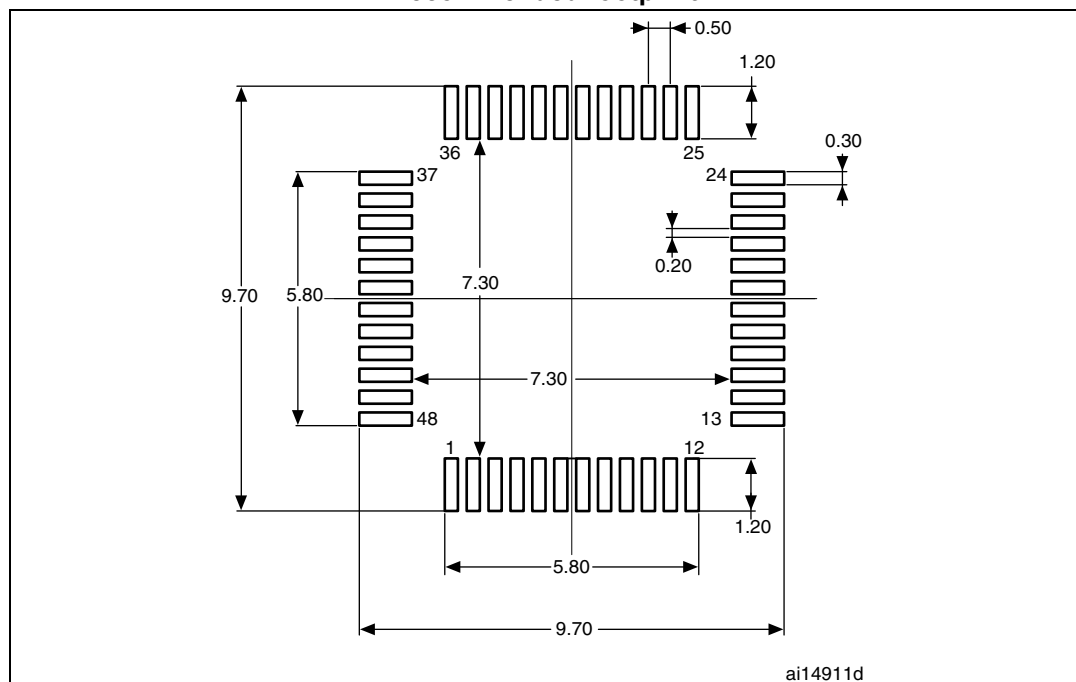
Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622

**Table 52. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data (continued)**

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 47. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint**



1. Dimensions are expressed in millimeters.