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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f100vbt7b

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1 Introduction

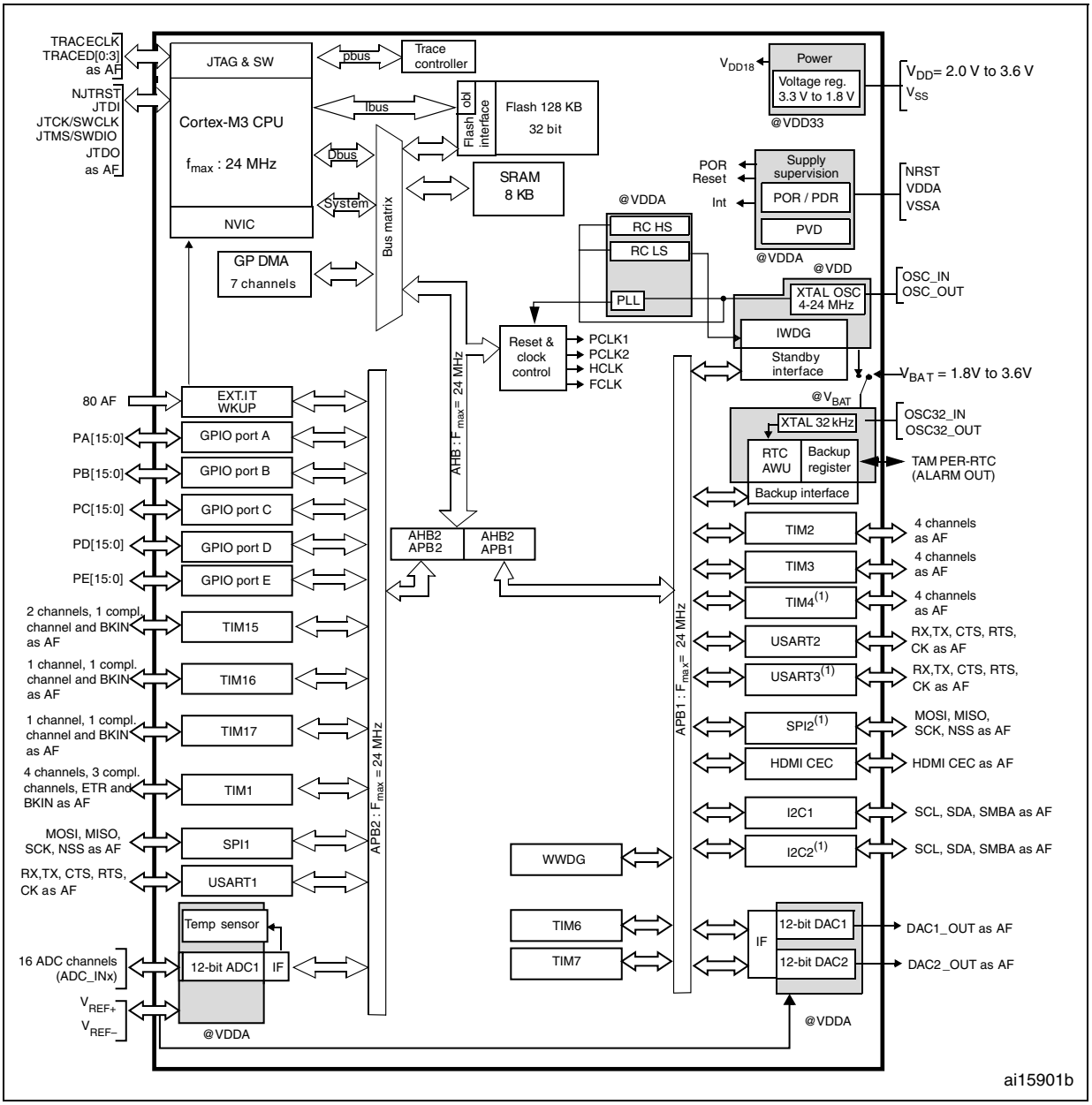
This datasheet provides the ordering information and mechanical device characteristics of the STM32F100x4, STM32F100x6, STM32F100x8 and STM32F100xB microcontrollers.

In the rest of the document, the STM32F100x4 and STM32F100x6 are referred to as low-density devices while the STM32F100x8 and STM32F100xB are identified as medium-density devices.

This STM32F100xx datasheet should be read in conjunction with the low- and medium-density STM32F100xx reference manual.
For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F100xx Flash programming manual.*
The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com.*

For information on the Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the www.arm.com website at the following address: http://infocenter.arm.com.

Figure 1. STM32F100xx value line block diagram



1. Peripherals not present in low-density value line devices.
2. AF = alternate function on I/O port pin.
3. T_A = –40 °C to +85 °C (junction temperature up to 105 °C) or T_A = –40 °C to +105 °C (junction temperature up to 125 °C).

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, DAC, I^2C, USART, all timers and ADC.

2.2.14 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are ten 16-bit registers used to store 20 bytes of user application data when V_{DD} power is not present.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the high-speed external clock divided by 128. The internal low power RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural crystal deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.2.15 Timers and watchdogs

The STM32F100xx devices include an advanced-control timer, six general-purpose timers, two basic timers and two watchdog timers.

Table 3 compares the features of the advanced-control, general-purpose and basic timers.

Table 3. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
TIM2, TIM3, TIM4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	Yes
TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	Yes
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard TIM timers which have the same architecture. The advanced control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIM2, TIM3, TIM4, TIM15, TIM16 & TIM17)

There are six synchronizable general-purpose timers embedded in the STM32F100xx devices (see *Table 3* for differences). Each general-purpose timers can be used to generate PWM outputs, or as simple time base.

TIM2, TIM3, TIM4

STM32F100xx devices feature three synchronizable 4-channels general-purpose timers. These timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2, TIM3, TIM4 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2, TIM3, TIM4 all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

TIM15, TIM16 and TIM17

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate with TIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16, and TIM17 have a complementary output with dead-time generation and independent DMA request generation

Table 4. Low & medium-density STM32F100xx pin definitions (continued)

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3)(4)	
LQFP100	LQFP64	TFBGA64	LQFP48					Default	Remap
9	4	B1	4	PC15-OSC32_OUT(5)	I/O	-	PC15(6)	OSC32_OUT	-
10	-	-	-	V_{SS_5}	S	-	V_{SS_5}	-	-
11	-	-	-	V_{DD_5}	S	-	V_{DD_5}	-	-
12	5	C1	5	OSC_IN	I	-	OSC_IN	-	PD0(7)
13	6	D1	6	OSC_OUT	O	-	OSC_OUT	-	PD1(7)
14	7	E1	7	NRST	I/O	-	NRST	-	-
15	8	E3	-	PC0	I/O	-	PC0	ADC1_IN10	-
16	9	E2	-	PC1	I/O	-	PC1	ADC1_IN11	-
17	10	F2	-	PC2	I/O	-	PC2	ADC1_IN12	-
18	11	-(8)	-	PC3	I/O	-	PC3	ADC1_IN13	-
19	12	F1	8	V_{SSA}	S	-	V_{SSA}	-	-
20	-	-	-	V_{REF-}	S	-	V_{REF-}	-	-
21	-	G1	-	V_{REF+}	S	-	V_{REF+}	-	-
22	13	H1	9	V_{DDA}	S	-	V_{DDA}	-	-
23	14	G2	10	PA0-WKUP	I/O	-	PA0	WKUP / USART2_CTS(12)/ ADC1_IN0 / TIM2_CH1_ETR(12)	-
24	15	H2	11	PA1	I/O	-	PA1	USART2_RTS(12)/ ADC1_IN1 / TIM2_CH2(12)	-
25	16	F3	12	PA2	I/O	-	PA2	USART2_TX(12)/ ADC1_IN2 / TIM2_CH3(12)/ TIM15_CH1(12)	-
26	17	G3	13	PA3	I/O	-	PA3	USART2_RX(12)/ ADC1_IN3 / TIM2_CH4(12) / TIM15_CH2(12)	-
27	18	C2	-	V_{SS_4}	S	-	V_{SS_4}	-	-
28	19	D2	-	V_{DD_4}	S	-	V_{DD_4}	-	-
29	20	H3	14	PA4	I/O	-	PA4	SPI1_NSS(12)/ADC1_IN4 USART2_CK(12) / DAC1_OUT	-
30	21	F4	15	PA5	I/O	-	PA5	SPI1_SCK(12)/ADC1_IN5 / DAC2_OUT	-
31	22	G4	16	PA6	I/O	-	PA6	SPI1_MISO(12)/ADC1_IN6 / TIM3_CH1(12)	TIM1_BKIN / TIM16_CH1
32	23	H4	17	PA7	I/O	-	PA7	SPI1_MOSI(12)/ADC1_IN7 / TIM3_CH2(12)	TIM1_CH1N / TIM17_CH1

Table 4. Low & medium-density STM32F100xx pin definitions (continued)

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(3)(4)	
LQFP100	LQFP64	TFBGA64	LQFP48					Default	Remap
33	24	H5	-	PC4	I/O	-	PC4	ADC1_IN14	-
34	25	H6	-	PC5	I/O	-	PC5	ADC1_IN15	-
35	26	F5	18	PB0	I/O	-	PB0	ADC1_IN8/TIM3_CH3(12)	TIM1_CH2N
36	27	G5	19	PB1	I/O	-	PB1	ADC1_IN9/TIM3_CH4(12)	TIM1_CH3N
37	28	G6	20	PB2	I/O	FT	PB2/BOOT1	-	-
38	-	-	-	PE7	I/O	FT	PE7	-	TIM1_ETR
39	-	-	-	PE8	I/O	FT	PE8	-	TIM1_CH1N
40	-	-	-	PE9	I/O	FT	PE9	-	TIM1_CH1
41	-	-	-	PE10	I/O	FT	PE10	-	TIM1_CH2N
42	-	-	-	PE11	I/O	FT	PE11	-	TIM1_CH2
43	-	-	-	PE12	I/O	FT	PE12	-	TIM1_CH3N
44	-	-	-	PE13	I/O	FT	PE13	-	TIM1_CH3
45	-	-	-	PE14	I/O	FT	PE14	-	TIM1_CH4
46	-	-	-	PE15	I/O	FT	PE15	-	TIM1_BKIN
47	29	G7	21	PB10	I/O	FT	PB10	I2C2_SCL(9)/USART3_TX (12)	TIM2_CH3 / HDMI_CEC
48	30	H7	22	PB11	I/O	FT	PB11	I2C2_SDA(9)/USART3_RX(12)	TIM2_CH4
49	31	D6	23	V_{SS_1}	S	-	V_{SS_1}	-	-
50	32	E6	24	V_{DD_1}	S	-	V_{DD_1}	-	-
51	33	H8	25	PB12	I/O	FT	PB12	SPI2_NSS(10)/ I2C2_SMBA(9)/ TIM1_BKIN(12)/USART3_C K(12)	-
52	34	G8	26	PB13	I/O	FT	PB13	SPI2_SCK(10) /TIM1_CH1N(12) USART3_CTS(12)	-
53	35	F8	27	PB14	I/O	FT	PB14	SPI2_MISO(10)/ TIM1_CH2N(12) / USART3_RTS(12)	TIM15_CH1
54	36	F7	28	PB15	I/O	FT	PB15	SPI2_MOSI(10) / TIM1_CH3N / TIM15_CH1N(12)	TIM15_CH2
55	-	-	-	PD8	I/O	FT	PD8	-	USART3_TX
56	-	-	-	PD9	I/O	FT	PD9	-	USART3_RX

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 2 V ≤V_{DD} ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

Table 17. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typical values(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	Running on high-speed external clock with an 8 MHz crystal(3)	24 MHz	7.3	2.6	mA
			16 MHz	5.2	2	
			8 MHz	2.8	1.3	
			4 MHz	2	1.1	
			2 MHz	1.5	1.1	
			1 MHz	1.25	1	
			500 kHz	1.1	1	
			125 kHz	1.05	0.95	
		Running on high-speed internal RC (HSI)	24 MHz	6.65	1.9	
			16 MHz	4.5	1.4	
			8 MHz	2.2	0.7	
			4 MHz	1.35	0.55	
			2 MHz	0.85	0.45	
			1 MHz	0.6	0.41	
			500 kHz	0.5	0.39	
			125 kHz	0.4	0.37	

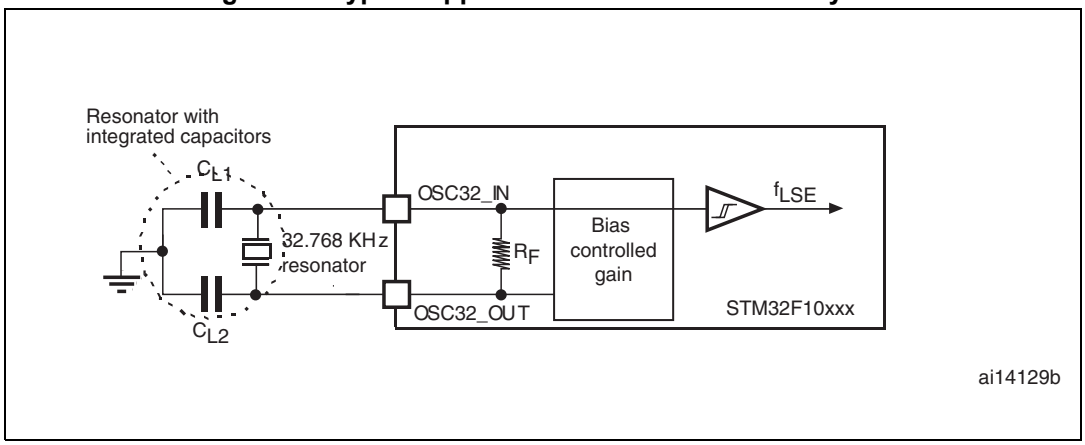
1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA for the ADC and of 0.5 mA for the DAC analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. An 8 MHz crystal is used as the external clock source. The AHB prescaler is used to reduce the frequency when f_{HCLK} > 8 MHz, the PLL is used when f_{HCLK} > 8 MHz.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 18*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions summarized in *Table 5*.

Figure 21. Typical application with a 32.768 kHz crystal



5.3.7 Internal clock source characteristics

The parameters given in *Table 23* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*.

High-speed internal (HSI) RC oscillator

Table 23. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
$DuCy_{(HSI)}$	Duty cycle	-	45	-	55	%
ACC_{HSI}	Accuracy of HSI oscillator	T_A = –40 to 105 °C(2)	-2.4	-	2.5	%
		T_A = –10 to 85 °C(2)	-2.2	-	1.3	%
		T_A = 0 to 70 °C(2)	-1.9	-	1.3	%
		T_A = 25 °C	-1	-	1	%
$t_{su(HSI)}$(3)	HSI oscillator startup time	-	1	-	2	µs
$I_{DD(HSI)}$(3)	HSI oscillator power consumption	-	-	80	100	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C °C unless otherwise specified.
2. Guaranteed by characterization results.
3. Guaranteed by design. Not tested in production

5.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 27. Flash memory characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	52.5	70	µs
t_{ERASE}	Page (1 KB) erase time	T_A = –40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Read mode f_{HCLK} = 24 MHz, V_{DD} = 3.3 V	-	-	20	mA
		Write / Erase modes f_{HCLK} = 24 MHz, V_{DD} = 3.3 V	-	-	5	mA
		Power-down mode / Halt, V_{DD} = 3.0 to 3.6 V	-	-	50	µA
V_{prog}	Programming voltage	-	2	-	3.6	V

1. Guaranteed by design.

Table 28. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value			Unit
			Min(1)	Typ	Max	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	-	-	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	-	-	Years
		1 kcycle(2) at T_A = 105 °C	10	-	-	
		10 kcycles(2) at T_A = 55 °C	20	-	-	

1. Based on characterization not tested in production.
2. Cycling performed over the whole temperature range.

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 30. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/24 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25°C, LQFP100 package compliant with SAE J1752/3	0.1 MHz to 30 MHz	9	dBµV
			30 MHz to 130 MHz	16	
			130 MHz to 1GHz	19	
			SAE EMI Level	4	-

5.3.11 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 31. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to JESD22-C101	III	500	

1. Based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD78 IC latch-up standard.

Table 32. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78	II level A

5.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 34* are derived from tests performed under the conditions summarized in *Table 8*. All I/Os are CMOS and TTL compliant.

Table 34. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard I/O input low level voltage	-	–0.3	-	0.28*(V_{DD}–2 V)+0.8 V	V
	I/O FT(1) input low level voltage		–0.3	-	0.32*(V_{DD}–2 V)+0.75 V	
V_{IH}	Standard I/O input high level voltage		0.41*(V_{DD}–2 V) +1.3 V	-	V_{DD}+0.3	
	I/O FT(1) input high level voltage	V_{DD} > 2 V	0.42*(V_{DD}–2)+1 V	-	5.5	
		V_{DD} ≤2 V			5.2	
V_{hys}	Standard I/O Schmitt trigger voltage hysteresis(2)	-	200	-	-	mV
	I/O FT Schmitt trigger voltage hysteresis(2)		5% V_{DD}(3)	-	-	mV
I_{lkg}	Input leakage current(4)	V_{SS} ≤V_{IN} ≤V_{DD} Standard I/Os	-	-	±1	µA
		V_{IN} = 5 V I/O FT	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(5)	V_{IN} = V_{SS}	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	V_{IN} = V_{DD}	30	40	50	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. FT = 5V tolerant. To sustain a voltage higher than V_{DD}+0.3 the internal pull-up/pull-down resistors must be disabled.
2. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by design.
3. With a minimum of 100 mV.
4. Leakage could be higher than max. if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 22* and *Figure 23* for standard I/Os, and in *Figure 24* and *Figure 25* for 5 V tolerant I/Os.

Output voltage levels

Unless otherwise specified, the parameters given in *Table 35* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 8*. All I/Os are CMOS and TTL compliant.

Table 35. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output Low level voltage for an I/O pin when 8 pins are sunk at the same time	CMOS port(2) I_{IO} = +8 mA, 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output High level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	TTL port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		2.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +20 mA(4) 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH} (3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–1.3	-	
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at the same time	I_{IO} = +6 mA(4) 2 V < V_{DD} < 2.7 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at the same time		V_{DD}–0.4	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 6* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 6* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Based on characterization data, not tested in production.

5.3.16 Communications interfaces

I²C interface characteristics

Unless otherwise specified, the parameters given in *Table 39* are derived from tests performed under the ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage conditions summarized in *Table 8*.

The STM32F100xx value line I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I²C characteristics are described in *Table 39*. Refer also to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 39. I²C characteristics

Symbol	Parameter	Standard mode I²C(1)		Fast mode I²C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	-	0	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

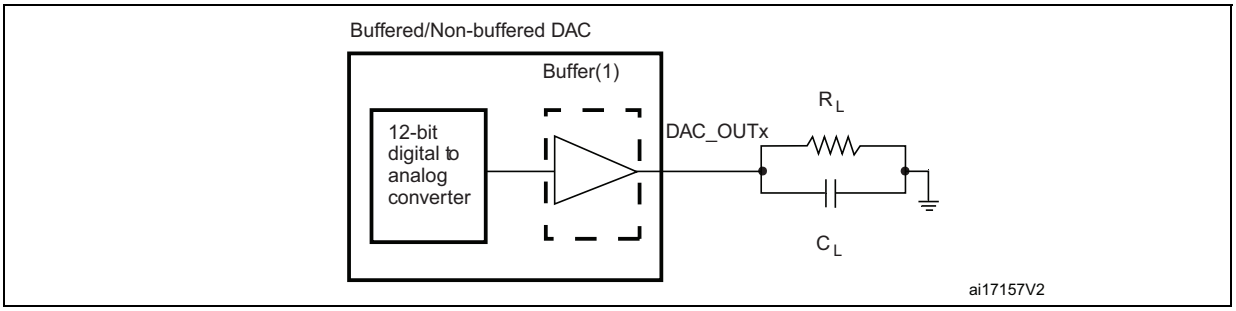
1. Guaranteed by design.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I²C frequencies. It must be at least 4 MHz to achieve fast mode I²C frequencies. It must be a multiple of 10 MHz to reach the 400 kHz maximum I2C fast mode clock.
3. The maximum Data hold time has only to be met if the interface does not stretch the low period of SCL signal.

Table 46. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max(1)	Unit	Comments
Offset(1)	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{REF+}/2)	-	-	±10	mV	Given for the DAC in 12-bit configuration
		-	-	±3	LSB	Given for the DAC in 10-bit at V_{REF+} = 3.6 V
		-	-	±12	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V
Gain error(1)	Gain error	-	-	±0.5	%	Given for the DAC in 12bit configuration
$t_{SETTLING}$(1)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	-	3	4	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
Update rate(1)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
t_{WAKEUP}(1)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+ (1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement	-	–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. Guaranteed by characterization results.
2. Guaranteed by design.

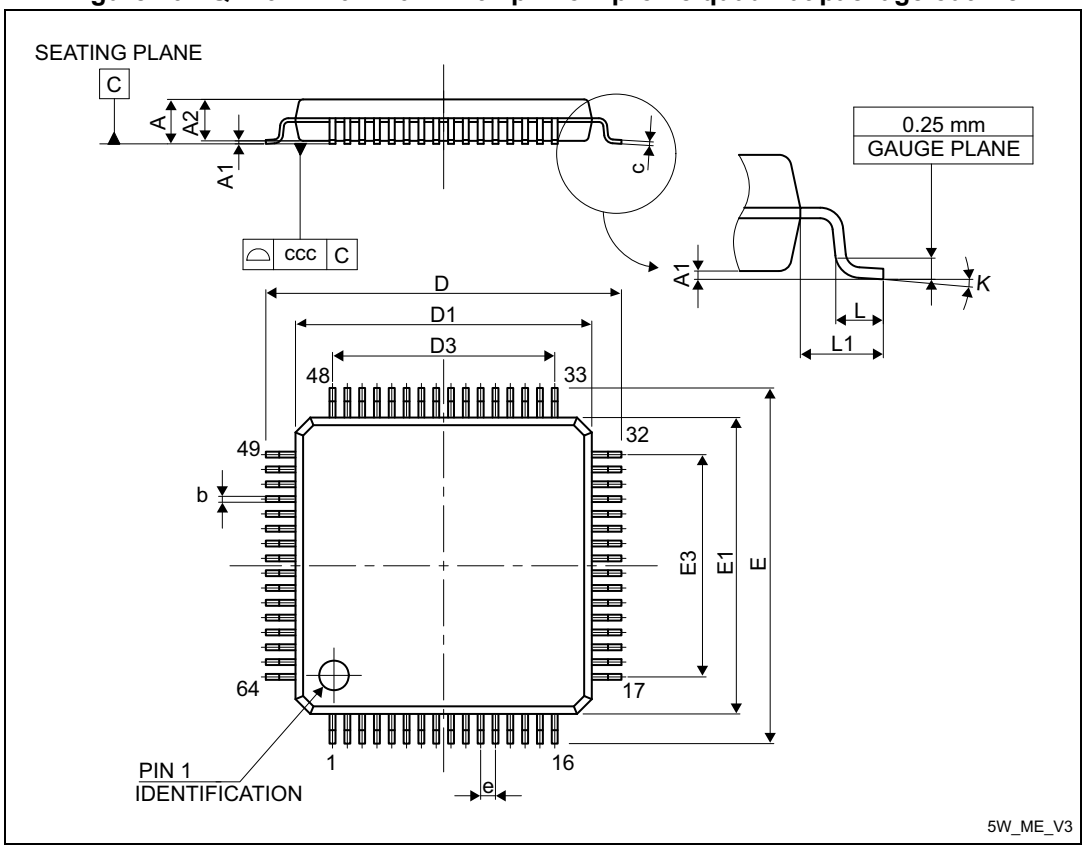
Figure 36. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.2 LQFP64 package information

Figure 40.LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline



1. Drawing is not in scale.

Table 49. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

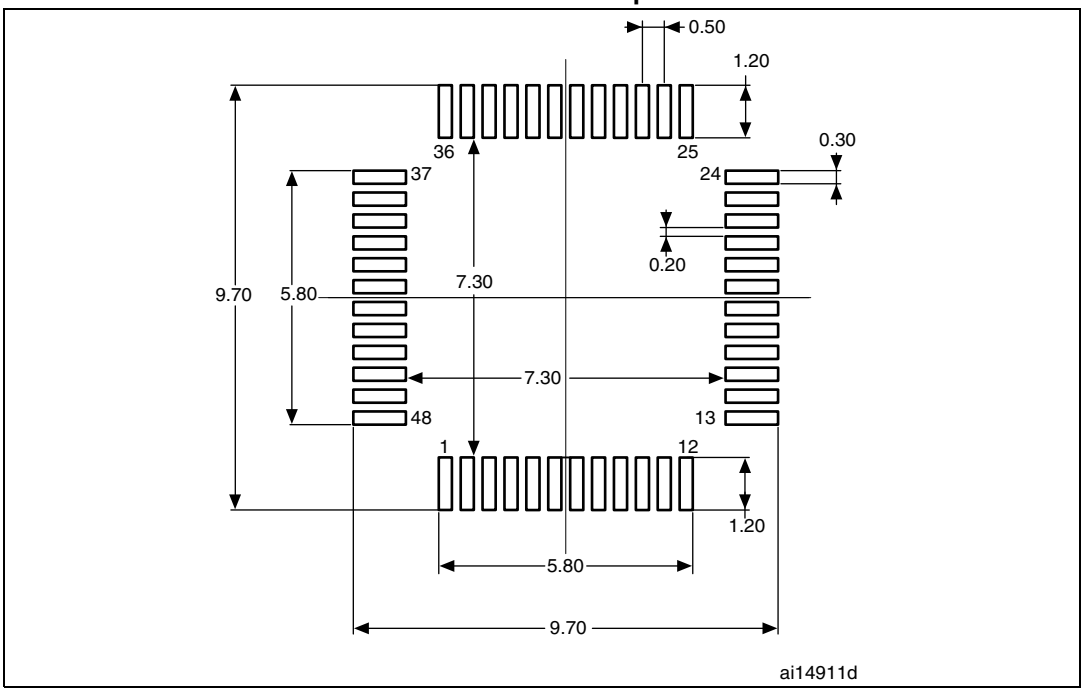
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-

Table 52. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 47. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

7 Ordering information scheme

Table 54. Ordering information scheme

Example: STM32 F 100 C 6 T 6 B xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Device subfamily

100 = value line

Pin count

C = 48 pins

R = 64 pins

V = 100 pins

Flash memory size

4 = 16 Kbytes of Flash memory

6 = 32 Kbytes of Flash memory

8 = 64 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

Package

T = LQFP

H = BGA

Temperature range

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

Internal code

B

Options

xxx = programmed parts

TR = tape and real

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 55. Document revision history (continued)

Date	Revision	Changes
08-Jun-2012	7	Updated *Table 6: Current characteristics on page 34* Updated *Table 39: I2C characteristics on page 64* Corrected note “non-robust “ in *Section 5.3.17: 12-bit ADC characteristics on page 68* Updated *Section 5.3.13: I/O port characteristics on page 57* Updated *Section 2.2.20: GPIOs (general-purpose inputs/outputs) on page 20* Updated *Table 4: Low & medium-density STM32F100xx pin definitions on page 24* Updated *Section 5.3.1: General operating conditions on page 34* Updated *Table 14: Maximum current consumption in Sleep mode, code running from Flash or RAM on page 39*
08-Jun-2015	8	Updated *Table 18: Peripheral current consumption*, *Table 31: ESD absolute maximum ratings*, *Table 48: LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data*, *Table 49: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data*, *Table 50: TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package mechanical data*, *Table 51: TFBGA64 recommended PCB design rules (0.5 mm pitch BGA)* and *Table 52: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data*. Updated *Figure 37: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline*, *Figure 38: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint*, *Figure 40: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline*, *Figure 41: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint*, *Figure 43: TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch thin profile fine pitch ball grid array package outline*, *Figure 44: TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array, recommended footprint*, *Figure 46: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline* and *Figure 47: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint*. Added *Figure 39: LQFP100 marking example (package top view)*, *Figure 42: LQFP64 marking example (package top view) Figure 45: TFBGA64 marking example (package top view)* and *Figure 48: LQFP48 marking example (package top view)*.
21-Nov-2016	9	Updated: – *Figure 7: Memory map* – *Figure 18: High-speed external clock source AC timing diagram* – *Figure 19: Low-speed external clock source AC timing diagram* – *Table 19: High-speed external user clock characteristics* – *Table 20: Low-speed external user clock characteristics* – *Table 42: ADC characteristics*