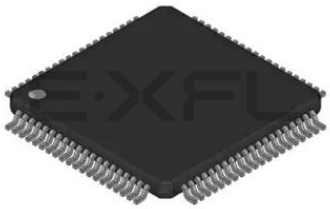
Infineon Technologies - XC2289I136F128LAAKXUMA1 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	128MHz
Connectivity	CANbus, EBI/EMI, FlexRay, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	118
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	90K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 28x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-13
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2289i136f128laakxuma1

2 General Device Information

The XC228xI series (16/32-Bit Single-Chip Microcontroller with 32-Bit Performance) is a part of the Infineon XC2000 Family of full-feature single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 128 million instructions per second) with extended peripheral functionality and enhanced IO capabilities. Optimized peripherals can be adapted flexibly to meet the application requirements. These derivatives utilize clock generation via PLL and internal or external clock sources. On-chip memory modules include program Flash, program RAM, and data RAM.

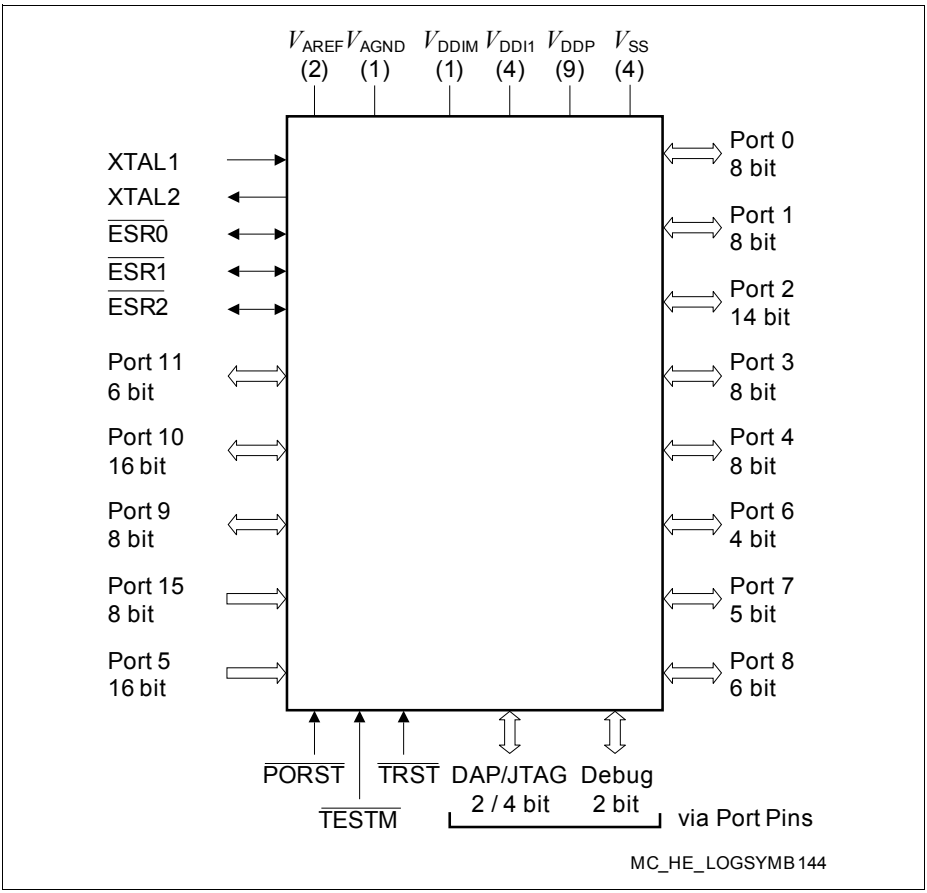

Figure 1 Logic Symbol

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
55	P2.0	O0 / I	St/B	**Bit 0 of Port 2, General Purpose Input/Output**
	TxDC5	O1	St/B	**CAN Node 5 Transmit Data Output**
	CCU63_CC60	O2	St/B	**CCU63 Channel 0 Output**
	AD13	OH / IH	St/B	**External Bus Interface Address/Data Line 13**
	RxDC0C	I	St/B	**CAN Node 0 Receive Data Input**
	CCU63_CC60INB	I	St/B	**CCU63 Channel 0 Input**
	T5INB	I	St/B	**GPT12E Timer T5 Count/Gate Input**
56	P2.1	O0 / I	St/B	**Bit 1 of Port 2, General Purpose Input/Output**
	TxDC0	O1	St/B	**CAN Node 0 Transmit Data Output**
	CCU63_CC61	O2	St/B	**CCU63 Channel 1 Output**
	AD14	OH / IH	St/B	**External Bus Interface Address/Data Line 14**
	RxDC5C	I	St/B	**CAN Node 5 Receive Data Input**
	CCU63_CC61INB	I	St/B	**CCU63 Channel 1 Input**
	T5EUDB	I	St/B	**GPT12E Timer T5 External Up/Down Control Input**
	ESR1_5	I	St/B	**ESR1 Trigger Input 5**
	ERU_0A0	I	St/B	**External Request Unit Channel 0 Input A0**
57	P11.4	O0 / I	St/B	**Bit 4 of Port 11, General Purpose Input/Output**
	CCU61_CC62	O1	St/B	**CCU61 Channel 2 Output**
	U3C1_DOUT	O2	St/B	**USIC3 Channel 1 Shift Data Output**
	RxDC5B	I	St/B	**CAN Node 5 Receive Data Input**
	CCU61_CC62INB	I	St/B	**CCU61 Channel 2 Input**
	U3C1_DX0B	I	St/B	**USIC3 Channel 1 Shift Data Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
78	P2.7	O0 / I	St/B	**Bit 7 of Port 2, General Purpose Input/Output**
	U0C1_SELO 0	O1	St/B	**USIC0 Channel 1 Select/Control 0 Output**
	U0C0_SELO 1	O2	St/B	**USIC0 Channel 0 Select/Control 1 Output**
	CC2_CC20	O3 / I	St/B	**CAPCOM2 CC20IO Capture Inp./ Compare Out.**
	A20	OH	St/B	**External Bus Interface Address Line 20**
	U0C1_DX2C	I	St/B	**USIC0 Channel 1 Shift Control Input**
	RxDC1C	I	St/B	**CAN Node 1 Receive Data Input**
	ESR2_7	I	St/B	**ESR2 Trigger Input 7**
	U4C0_DX0D	I	St/B	**USIC4 Channel 0 Shift Data Input**
79	P0.1	O0 / I	St/B	**Bit 1 of Port 0, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CCU61_CC6 1	O3	St/B	**CCU61 Channel 1 Output**
	A1	OH	St/B	**External Bus Interface Address Line 1**
	U1C0_DX0B	I	St/B	**USIC1 Channel 0 Shift Data Input**
	CCU61_CC6 1INA	I	St/B	**CCU61 Channel 1 Input**
	U1C0_DX1A	I	St/B	**USIC1 Channel 0 Shift Clock Input**
80	P2.8	O0 / I	DP/B	**Bit 8 of Port 2, General Purpose Input/Output**
	U0C1_SCLK OUT	O1	DP/B	**USIC0 Channel 1 Shift Clock Output**
	EXTCLK	O2	DP/B	**Programmable Clock Signal Output** 1)
	CC2_CC21	O3 / I	DP/B	**CAPCOM2 CC21IO Capture Inp./ Compare Out.**
	A21	OH	DP/B	**External Bus Interface Address Line 21**
	U0C1_DX1D	I	DP/B	**USIC0 Channel 1 Shift Clock Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
84	P10.0	O0 / I	St/B	**Bit 0 of Port 10, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CCU60_CC60	O2	St/B	**CCU60 Channel 0 Output**
	AD0	OH / IH	St/B	**External Bus Interface Address/Data Line 0**
	CCU60_CC60INA	I	St/B	**CCU60 Channel 0 Input**
	ESR1_2	I	St/B	**ESR1 Trigger Input 2**
	U0C0_DX0A	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX0A	I	St/B	**USIC0 Channel 1 Shift Data Input**
85	P3.0	O0 / I	St/B	**Bit 0 of Port 3, General Purpose Input/Output**
	U2C0_DOUT	O1	St/B	**USIC2 Channel 0 Shift Data Output**
	ESR1_1	I	St/B	**ESR1 Trigger Input 1**
	U2C0_DX0A	I	St/B	**USIC2 Channel 0 Shift Data Input**
	RxDC3B	I	St/B	**CAN Node 3 Receive Data Input**
	U2C0_DX1A	I	St/B	**USIC2 Channel 0 Shift Clock Input**
86	P10.1	O0 / I	St/B	**Bit 1 of Port 10, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU60_CC61	O2	St/B	**CCU60 Channel 1 Output**
	AD1	OH / IH	St/B	**External Bus Interface Address/Data Line 1**
	CCU60_CC61INA	I	St/B	**CCU60 Channel 1 Input**
	U0C0_DX1A	I	St/B	**USIC0 Channel 0 Shift Clock Input**
	U0C0_DX0B	I	St/B	**USIC0 Channel 0 Shift Data Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
95	P10.3	O0 / I	St/B	**Bit 3 of Port 10, General Purpose Input/Output**
	CCU60_COUT60	O2	St/B	**CCU60 Channel 0 Output**
	AD3	OH / IH	St/B	**External Bus Interface Address/Data Line 3**
	U0C0_DX2A	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2A	I	St/B	**USIC0 Channel 1 Shift Control Input**
	U3C0_DX0A	I	St/B	**USIC3 Channel 0 Shift Data Input**
96	P0.5	O0 / I	St/B	**Bit 5 of Port 0, General Purpose Input/Output**
	U1C1_SCLKOUT	O1	St/B	**USIC1 Channel 1 Shift Clock Output**
	U1C0_SELO2	O2	St/B	**USIC1 Channel 0 Select/Control 2 Output**
	CCU61_COUT62	O3	St/B	**CCU61 Channel 2 Output**
	A5	OH	St/B	**External Bus Interface Address Line 5**
	U1C1_DX1A	I	St/B	**USIC1 Channel 1 Shift Clock Input**
	U1C0_DX1C	I	St/B	**USIC1 Channel 0 Shift Clock Input**
	RXDC3E	I	St/B	**CAN Node 3 Receive Data Input**
97	P3.3	O0 / I	St/B	**Bit 3 of Port 3, General Purpose Input/Output**
	U2C0_SELO0	O1	St/B	**USIC2 Channel 0 Select/Control 0 Output**
	U2C1_SELO1	O2	St/B	**USIC2 Channel 1 Select/Control 1 Output**
	U4C0_SELO0	O3	St/B	**USIC4 Channel 0 Select/Control 0 Output**
	U2C0_DX2A	I	St/B	**USIC2 Channel 0 Shift Control Input**
	RxDC3A	I	St/B	**CAN Node 3 Receive Data Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
107	P3.7	O0 / I	St/B	**Bit 7 of Port 3, General Purpose Input/Output**
	U2C1_DOUT	O1	St/B	**USIC2 Channel 1 Shift Data Output**
	U2C0_SELO 3	O2	St/B	**USIC2 Channel 0 Select/Control 3 Output**
	U0C0_SELO 7	O3	St/B	**USIC0 Channel 0 Select/Control 7 Output**
	U2C1_DX0B	I	St/B	**USIC2 Channel 1 Shift Data Input**
111	P1.0	O0 / I	St/B	**Bit 0 of Port 1, General Purpose Input/Output**
	U1C0_MCLK OUT	O1	St/B	**USIC1 Channel 0 Master Clock Output**
	U1C0_SELO 4	O2	St/B	**USIC1 Channel 0 Select/Control 4 Output**
	A8	OH	St/B	**External Bus Interface Address Line 8**
	ESR1_3	I	St/B	**ESR1 Trigger Input 3**
	ERU_0B0	I	St/B	**External Request Unit Channel 0 Input B0**
	CCU62_CTR APB	I	St/B	**CCU62 Emergency Trap Input**
	T6INB	I	St/B	**GPT12E Timer T6 Count/Gate Input**
112	P9.0	O0 / I	St/B	**Bit 0 of Port 9, General Purpose Input/Output**
	CCU63_CC6 0	O1	St/B	**CCU63 Channel 0 Output**
	CCU63_CC6 0INA	I	St/B	**CCU63 Channel 0 Input**
	T6EUDB	I	St/B	**GPT12E Timer T6 External Up/Down Control Input**

Memory Content Protection

The contents of on-chip memories can be protected against soft errors (induced e.g. by radiation) by activating the parity mechanism or the Error Correction Code (ECC).
The parity mechanism can detect a single-bit error and prevent the software from using incorrect data or executing incorrect instructions.
The ECC mechanism can detect and automatically correct single-bit errors. This supports the stable operation of the system.

It is strongly recommended to activate the ECC mechanism wherever possible because this dramatically increases the robustness of an application against such soft errors.

3.3 Central Processing Unit (CPU)

The core of the CPU consists of a 5-stage execution pipeline with a 2-stage instruction-fetch pipeline, a 16-bit arithmetic and logic unit (ALU), a 32-bit/40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated SFRs. The ALU features a multiply-and-divide unit, a bit-mask generator, and a barrel shifter.

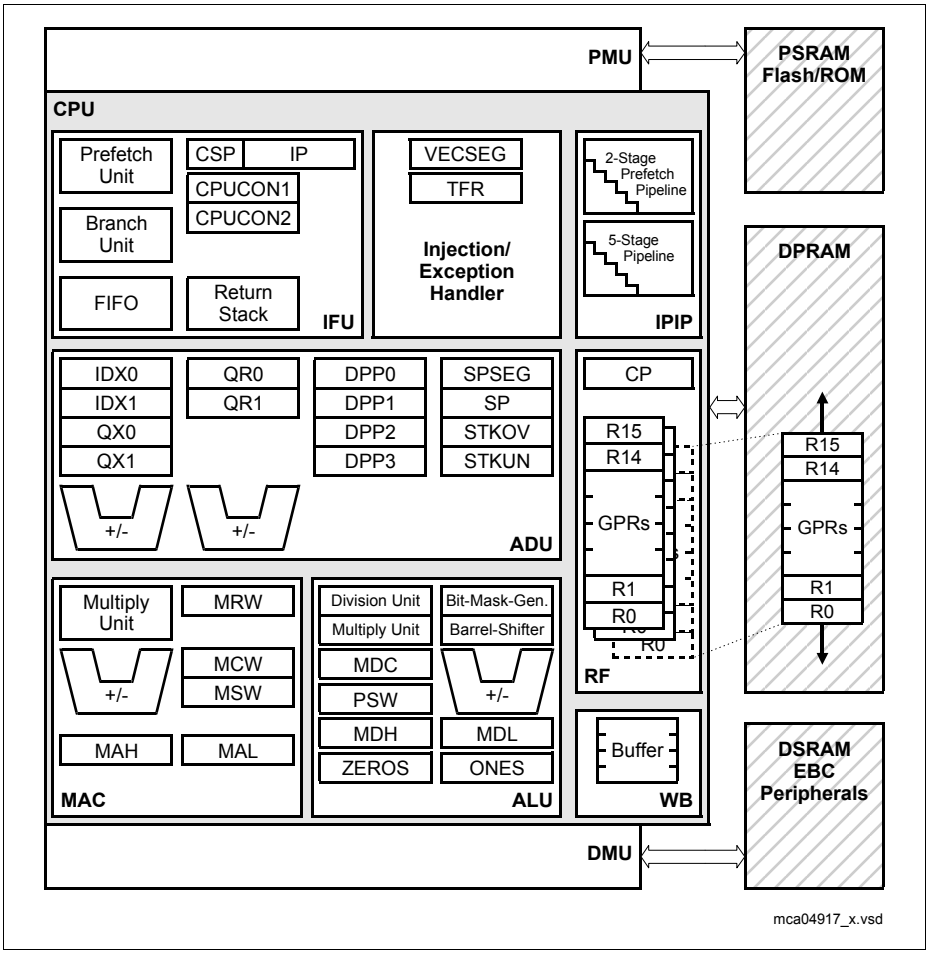

Figure 3 CPU Block Diagram

With this hardware most XC228xI instructions are executed in a single machine cycle of ns @ -MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle, no matter how many bits are shifted. Also, multiplication and most MAC instructions execute in one cycle. All multiple-cycle instructions have been optimized so that they can be executed very fast; for example, a 32-/16-bit division is started within 4 cycles while the remaining cycles are executed in the background. Another pipeline optimization, the branch target prediction, eliminates the execution time of branch instructions if the prediction was correct.

The CPU has a register context consisting of up to three register banks with 16 word-wide GPRs each at its disposal. One of these register banks is physically allocated within the on-chip DPRAM area. A Context Pointer (CP) register determines the base address of the active register bank accessed by the CPU at any time. The number of these register bank copies is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 32 Kwords is provided for storage of temporary data. The system stack can be allocated to any location within the address space (preferably in the on-chip RAM area); it is accessed by the CPU with the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared with the stack pointer value during each stack access to detect stack overflow or underflow.

The high performance of the CPU hardware implementation can be best utilized by the programmer with the highly efficient XC228xI instruction set. This includes the following instruction classes:

- Standard Arithmetic Instructions
- DSP-Oriented Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

3.17 Clock Generation

The Clock Generation Unit can generate the system clock signal f_{SYS} for the XC228xI from a number of external or internal clock sources:

- External clock signals with pad voltage or core voltage levels
- External crystal or resonator using the on-chip oscillator
- On-chip clock source for operation without crystal/resonator
- Wake-up clock (ultra-low-power) to further reduce power consumption

The programmable on-chip PLL with multiple prescalers generates a clock signal for maximum system performance from standard crystals, a clock input signal, or from the on-chip clock source. See also **Section 4.7.2**.

The Oscillator Watchdog (OWD) generates an interrupt if the crystal oscillator frequency falls below a certain limit or stops completely. In this case, the system can be supplied with an emergency clock to enable operation even after an external clock failure.

All available clock signals can be output on one of two selectable pins.

4.1.3 Voltage Range Definition

The XC228xI timing depends on the supply voltage. If such a dependency exists the timing values are given for 2 voltage areas commonly used. The voltage areas are defined in the following tables.

Table 14 Upper Voltage Range Definition

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage for IO pads and voltage regulators	V_{DDP} SR	4.5	5	5.5	V	$f_{SYS} \leq 100$ MHz
		4.75	5	5.25	V	$f_{SYS} \leq 128$ MHz

Table 15 Lower Voltage Range Definition

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage for IO pads and voltage regulators	V_{DDP} SR	3.0	3.3	4.5	V	

4.1.4 Pad Timing Definition

If not otherwise noted, all timing parameters are tested and are valid for the corresponding output pins operating in strong driver, fast edge mode.
See also **“Pad Properties” on Page 118**.

4.1.5 Parameter Interpretation

The parameters listed in the following include both the characteristics of the XC228xI and its demands on the system. To aid in correctly interpreting the parameters when evaluating them for a design, they are marked accordingly in the column “Symbol”:

CC (**C**ontroller **C**haracteristics):
The logic of the XC228xI provides signals with the specified characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the specified characteristics to the XC228xI.

Table 19 Leakage Power Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Leakage supply current (DMP_1 off)[1]	I_{LK0} CC	–	20	35	µA	T_J= 25 °C[2]
		–	115	330	µA	T_J= 85 °C[2]
		–	270	880	µA	T_J= 125 °C[2]
		–	420	1 450	µA	T_J= 150 °C[2]
Leakage supply current (DMP_1 powered)[1]	I_{LK1} CC	–	0.03	0.05	mA	T_J= 25 °C[2]
		–	0.7	1.7	mA	T_J= 85 °C[2]
		–	3.0	8.3	mA	T_J= 125 °C[2]
		–	6.4	18.5	mA	T_J= 150 °C[2]

1) The supply current caused by leakage depends mainly on the junction temperature and the supply voltage. The temperature difference between the junction temperature T_J and the ambient temperature T_A must be taken into account. As this fraction of the supply current does not depend on device activity, it must be added to other power consumption values.

2) All inputs (including pins configured as inputs) are set at 0 V to 0.1 V or at V_{DDP} - 0.1 V to V_{DDP} and all outputs (including pins configured as outputs) are disconnected.

Note: A fraction of the leakage current flows through domain DMP_A (pin V_{DDPA}). This current can be calculated as 7 000 $\times e^{-\alpha}$, with α = 5 000 / (273 + 1.3$\times T_J$).
For T_J = 150°C, this results in a current of 160 μA.

The leakage power consumption can be calculated according to the following formula:

I_{LK0} = 500 000 + $e^{-\alpha}$, with α = 3 000 / (273 + B$\times T_J$) must be tagged “PWR_Management”

Parameter B must be replaced by

- 1.0 for typical values
- 1.6 for maximum values

I_{LK1} = 580 000 + $e^{-\alpha}$, with α = 5 000 / (273 + B$\times T_J$)

Parameter B must be replaced by

- 1.1 for typical values
- 1.4 for maximum values

2) This parameter includes the sample time (also the additional sample time specified by STC), the time to determine the digital result and the time to load the result register with the conversion result. Values for the basic clock t_{ADCI} depend on programming.

3) The broken wire detection delay against V_{AGND} is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 500 µs. Result below 10% (66_H).

4) The broken wire detection delay against V_{AREF} is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 10 µs. This function is influenced by leakage current, in particular at high temperature. Result above 80% (332_H).

5) V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

Table 21 ADC Parameters for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input resistance of the selected analog channel	R_{AIN} CC	–	0.9	1.5	kΩ	not subject to production test 1)
Input resistance of the reference input	R_{AREF} CC	–	0.5	1	kΩ	not subject to production test 1)
Differential Non-Linearity Error 2)3)4)5)	$\|EA_{DNL}\|$ CC	–	1.5	3.0	LSB	not subject to production test
Gain Error 2)3)4)5)	$\|EA_{GAIN}\|$ CC	–	0.5	3.5	LSB	not subject to production test
Integral Non-Linearity 2)3)4)5)	$\|EA_{INL}\|$ CC	–	1.5	3.0	LSB	not subject to production test
Offset Error 2)3)4)5)	$\|EA_{OFF}\|$ CC	–	1.0	4.0	LSB	not subject to production test
Total Unadjusted Error 3)4)	|TUE| CC	–	2.5	4	LSB	6)
Analog clock frequency	f_{ADCI} SR	2	–	20	MHz	Std. reference input (V_{AREF})
		2	–	17.5	MHz	Alt. reference input (CH0)
Wakeup time from analog powerdown, fast mode	t_{WAF} CC	–	–	7	µs	
Wakeup time from analog powerdown, slow mode	t_{WAS} CC	–	–	11.5	µs	

1) The short-term frequency deviation refers to a timeframe of a few hours and is measured relative to the current frequency at the beginning of the respective timeframe. This parameter is useful to determine a time span for re-triggering a LIN synchronization.
2) This parameter is tested for the fastest and the slowest selection. The medium selections are not subject to production test - verified by design/characterization
3) f_{WU} in MHz
4) This value includes a hysteresis of approximately 50 mV for rising voltage.
5) V_{LV} = selected PVC/SWD voltage level
6) The limit V_{LV} - 0.10 V is valid for the OK1 level. The limit for the OK2 level is V_{LV} - 0.15 V.

Conditions for t_{SPO} Timing Measurement

The time required for the transition from **Power-On** to **Base** mode is called t_{SPO}. It is measured under the following conditions:

Precondition: The pad supply is valid, i.e. V_{DDPB} is above 3.0 V and remains above 3.0 V even though the XC228xI is starting up. See also V_{DDPB} requirements in **Table 13**.

Start condition: Power-on reset is removed ($\overline{\text{PORST}}$ = 1).

End condition: External pin toggle caused by first user instruction executed from FLASH after startup.

Conditions for t_{SSB} Timing Measurement

The time required for the transition from **Standby** to **Base** mode is called t_{SSB}. It is measured under the following conditions:

Precondition: The **Standby** mode has been entered using the procedure defined in the Programmer's Guide.

Start condition: Pin toggle on $\overline{\text{ESR}}$ pin triggering the startup sequence.

End condition: External pin toggle caused by first user instruction executed from FLASH after startup.

Conditions for t_{SSO} Timing Measurement

The time required for the transition from **Stopover** to **Stopover Waked-Up** mode is called t_{SSO}. It is measured under the following conditions:

Precondition: The **Stopover** mode has been entered using the procedure defined in the Programmer's Guide.

Start condition: Pin toggle on $\overline{\text{ESR}}$ pin triggering the startup sequence.

End condition: External pin toggle caused by first user instruction executed from PSRAM after startup.

4.5 Flash Memory Parameters

The XC228xI is delivered with all Flash sectors erased and with no protection installed.

The data retention time of the XC228xI's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 27 Flash Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Parallel Flash module program/erase limit depending on Flash read activity	N_{PP} SR	–	–	5[1)]		$N_{FL\_RD} \leq 1$
		–	–	1[2)]		$N_{FL\_RD} > 1$
Flash erase endurance for security pages	N_{SEC} SR	10	–	–	cycles	$t_{RET} \geq 20$ years
Flash wait states[3)]	$N_{WSFLASH}$ SR	1	–	–		$f_{SYS} \leq 8$ MHz
		2	–	–		$f_{SYS} \leq 13$ MHz
		3	–	–		$f_{SYS} \leq 17$ MHz
		4	–	–		$f_{SYS} > 17$ MHz
Flash wait state extension[4)]	N_{WSFLE} SR	0	–	–		$f_{SYS} \leq 80$ MHz
		1	–	–		$f_{SYS} > 80$ MHz; $f_{SYS} \leq 128$ MHz
Erase time per sector/page	t_{ER} CC	–	7[5)]	8.0	ms	
Programming time per page	t_{PR} CC	–	3[5)]	3.5	ms	
Data retention time	t_{RET} CC	20	–	–	years	$N_{Er} \leq 1\,000$ cycles
Drain disturb limit	N_{DD} SR	32	–	–	cycles	

4.6.4 Pad Properties

The output pad drivers of the XC228xI can operate in several user-selectable modes. Strong driver mode allows controlling external components requiring higher currents such as power bridges or LEDs. Reducing the driving power of an output pad reduces electromagnetic emissions (EME). In strong driver mode, selecting a slower edge reduces EME.

The dynamic behavior, i.e. the rise time and fall time, depends on the applied external capacitance that must be charged and discharged. Timing values are given for a capacitance of 20 pF, unless otherwise noted.

In general, the performance of a pad driver depends on the available supply voltage V_{DDP}. Therefore the following tables list the pad parameters for the upper voltage range and the lower voltage range, respectively.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 35 EBC External Bus Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output valid delay for $\overline{RD}$, $\overline{WR}$(L/$\overline{H}$)	t_{10} CC	–	7	13	ns	
Output valid delay for $\overline{BHE}$, ALE	t_{11} CC	–	7	14	ns	
Address output valid delay for A23 ... A0	t_{12} CC	–	8	14	ns	
Address output valid delay for AD15 ... AD0 (MUX mode)	t_{13} CC	–	8	15	ns	
Output valid delay for $\overline{CS}$	t_{14} CC	–	7	13	ns	
Data output valid delay for AD15 ... AD0 (write data, MUX mode)	t_{15} CC	–	8	15	ns	
Data output valid delay for D15 ... D0 (write data, DEMUX mode)	t_{16} CC	–	8	15	ns	
Output hold time for $\overline{RD}$, $\overline{WR}$(L/$\overline{H}$)	t_{20} CC	-2	6	8	ns	
Output hold time for $\overline{BHE}$, ALE	t_{21} CC	-2	6	10	ns	
Address output hold time for AD15 ... AD0	t_{23} CC	-3	6	8	ns	
Output hold time for $\overline{CS}$	t_{24} CC	-3	6	11	ns	
Data output hold time for D15 ... D0 and AD15 ... AD0	t_{25} CC	-3	6	8	ns	
Input setup time for READY, D15 ... D0, AD15 ... AD0	t_{30} SR	25	15	–	ns	
Input hold time READY, D15 ... D0, AD15 ... AD0[1)]	t_{31} SR	0	-7	–	ns	

1) Read data are latched with the same internal clock edge that triggers the address change and the rising edge of RD. Address changes before the end of RD have no impact on (demultiplexed) read cycles. Read data can change after the rising edge of RD.

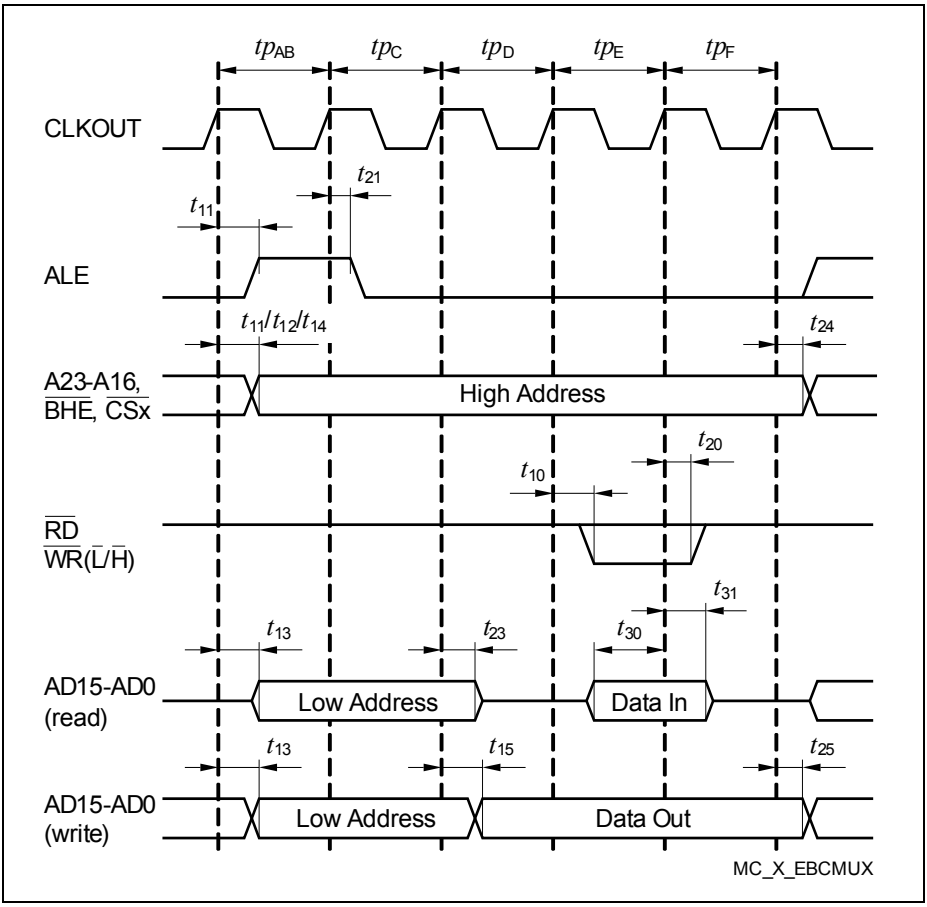

Figure 20 Multiplexed Bus Cycle

Table 45 Interface Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	50[1]	–	–	ns	
TCK high time	t_2 SR	16	–	–	ns	
TCK low time	t_3 SR	16	–	–	ns	
TCK clock rise time	t_4 SR	–	–	8	ns	
TCK clock fall time	t_5 SR	–	–	8	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6	–	–	ns	
TDI/TMS hold after TCK rising edge	t_7 SR	6	–	–	ns	
TDO valid from TCK falling edge (propagation delay)[2]	t_8 CC	–	32	36	ns	
TDO high impedance to valid output from TCK falling edge[3][2]	t_9 CC	–	32	36	ns	
TDO valid output to high impedance from TCK falling edge[2]	t_{10} CC	–	32	36	ns	
TDO hold after TCK falling edge[2]	t_{18} CC	5	–	–	ns	

1) The debug interface cannot operate faster than the overall system, therefore $t_1 \geq t_{SYS}$.

2) The falling edge on TCK is used to generate the TDO timing.

3) The setup time for TDO is given implicitly by the TCK cycle time.

w w w . i n f i n e o n . c o m

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