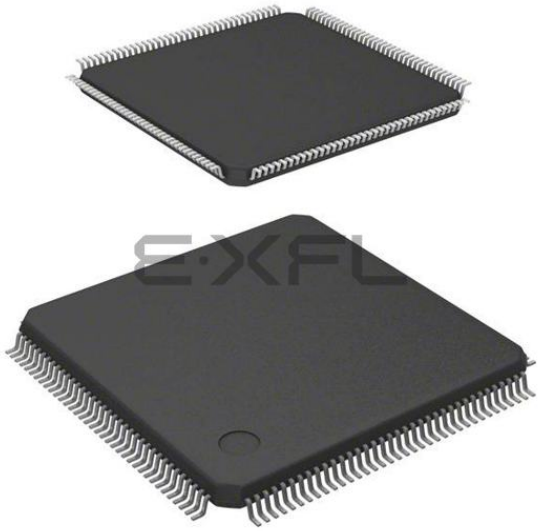

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ST10
Core Size	16-Bit
Speed	40MHz
Connectivity	ASC, CANbus, EBI/EMI, I²C, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st10f272m-4t3

2 Pin data

Figure 2. Pin configuration (top view)

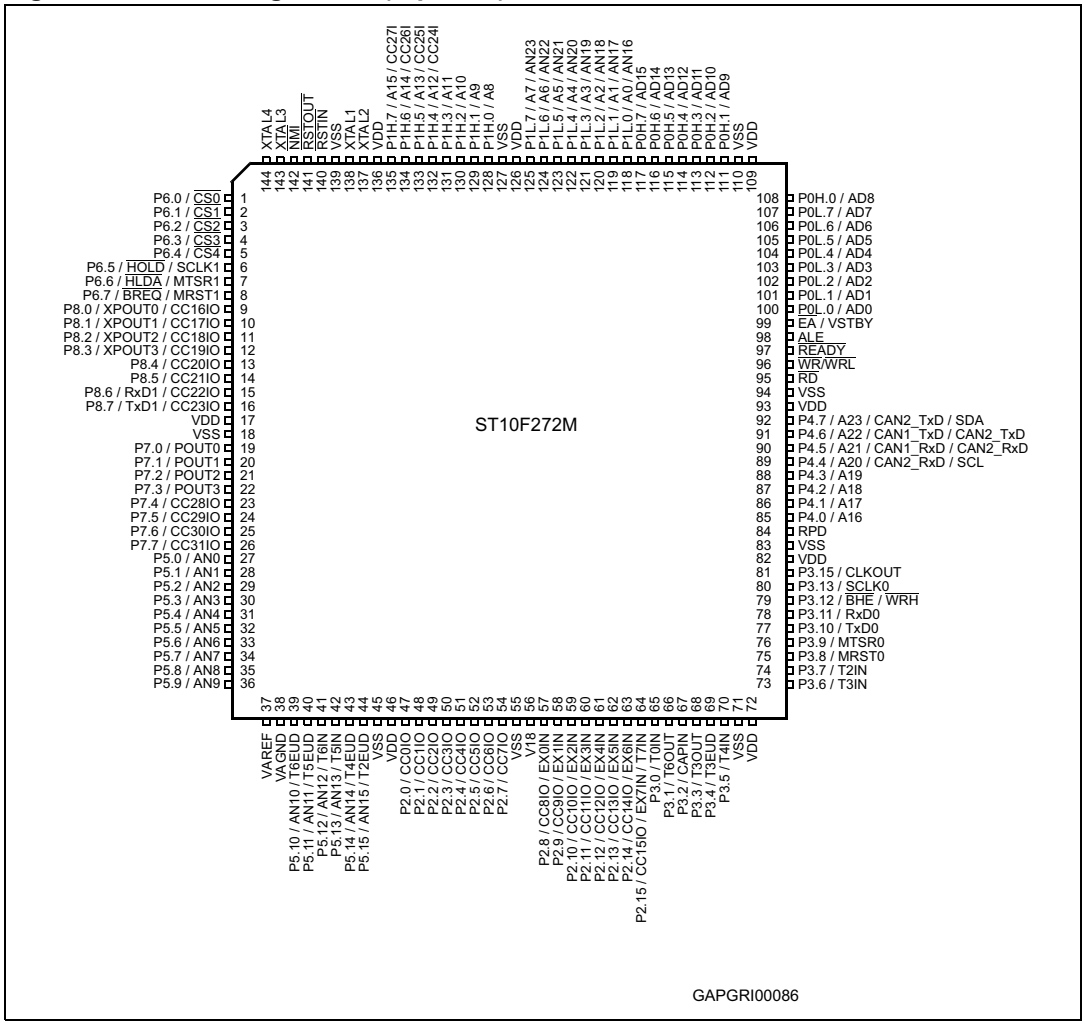
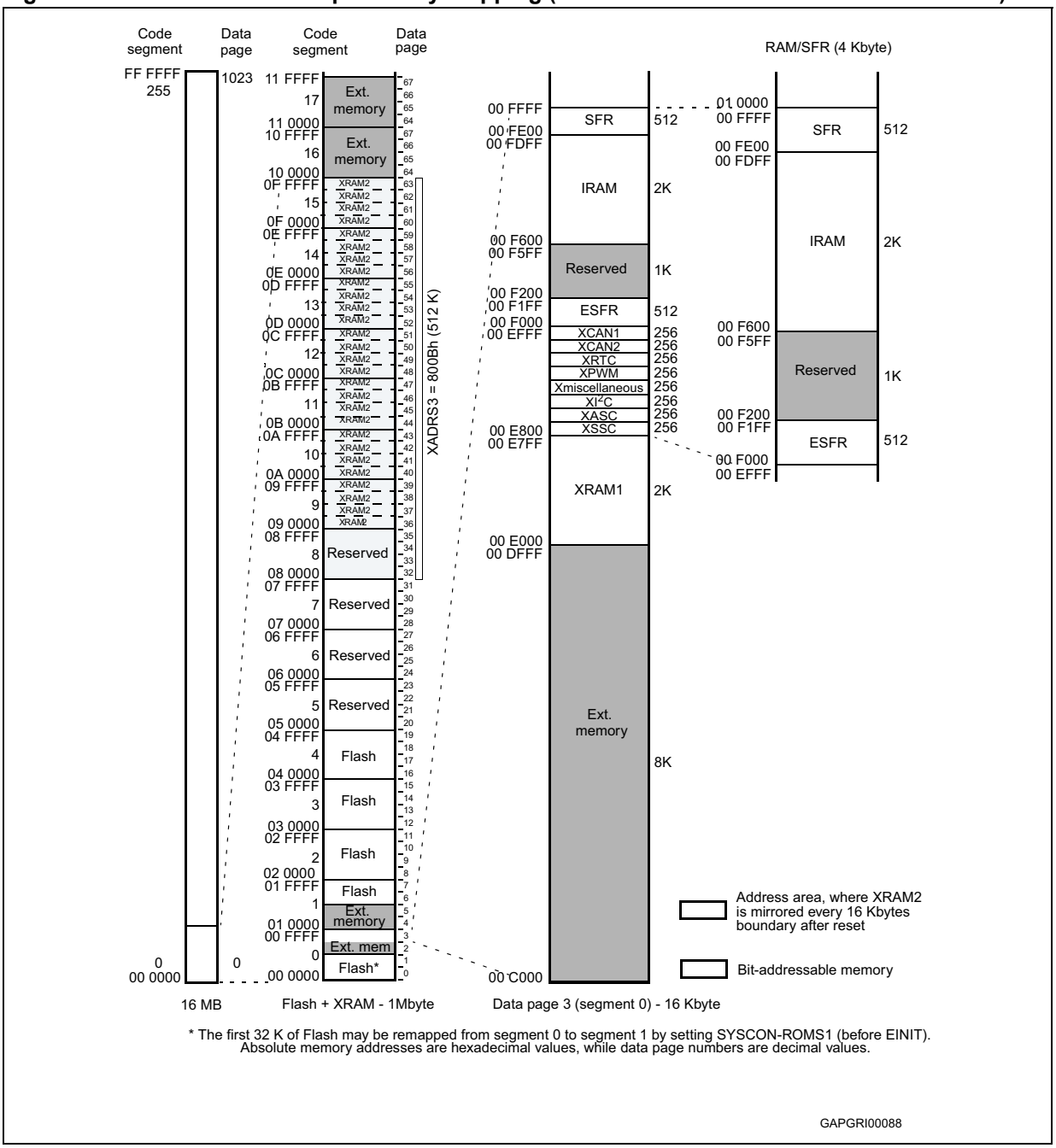


Figure 4. ST10F272M on-chip memory mapping (ROMEN = 1/XADRS = 800Bh - reset value)



* The first 32 K of Flash may be remapped from segment 0 to segment 1 by setting SYSCON-ROMS1 (before EINIT).
Absolute memory addresses are hexadecimal values, while data page numbers are decimal values.

Table 11. Banks (BxS) and sectors (BxFy) status bits meaning

ERR	SUSP	B0S = 1 meaning	B0Fy = 1 meaning
1	-	Erase error in bank0	Erase error in sector y of bank0
0	1	Erase suspended in bank0	Erase suspended in sector y of bank0
0	0	Don't care	Don't care

5.4.5 Flash data register 0 low (FDR0L)

During program operations, the Flash address registers (FARH/L) are used to store the Flash address in which to program and the Flash data registers (FDR1H/L-FDR0H/L) are used to store the Flash data to program.

FDR0L (0x08 0008) FCR Reset value: FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIN15	DIN14	DIN13	DIN12	DIN11	DIN10	DIN9	DIN8	DIN7	DIN6	DIN5	DIN4	DIN3	DIN2	DIN1	DIN0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 12. Flash data register 0 low

Bit	Name	Function
15:0	DIN[15:0]	Data Input 15:0 These bits must be written with the data to program the Flash with the following operations: Word program (32-bit), double word program (64-bit) and set protection.

5.4.6 Flash data register 0 high (FDR0H)

FDR0H (0x08 000A) FCR Reset value: FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIN31	DIN30	DIN29	DIN28	DIN27	DIN26	DIN25	DIN24	DIN23	DIN22	DIN21	DIN20	DIN19	DIN18	DIN17	DIN16
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 13. Flash data register 0 high

Bit	Name	Function
15:0	DIN[31:16]	Data input 31:16 These bits must be written with the data to program the Flash with the following operations: Word program (32-bit), double word program (64-bit) and set protection.

Example of indirect addressing mode

```
MOV  RWm, #ADDRESS;        /*Load Add in RWm*/
MOV  RWn, #DATA;           /*Load Data in RWn*/
MOV  [RWm], RWn;           /*Indirect addressing*/
```

Word program

Example: 32-bit word program of data 0xAAAAAAAA at address 0x025554

```
FCR0H|= 0x2000;            /*Set WPG in FCR0H*/
FARL  = 0x5554;            /*Load Add in FARL*/
FARH  = 0x0002;            /*Load Add in FARH*/
FDR0L = 0xAAAA;            /*Load Data in FDR0L*/
FDR0H = 0xAAAA;            /*Load Data in FDR0H*/
FCR0H|= 0x8000;            /*Operation start*/
```

Double word program

Example: Double word program (64-bit) of data 0x55AA55AA at address 0x035558 and data 0xAA55AA55 at address 0x03555C in IFlash module.

```
FCR0H   |= 0x1000;         /*Set DWPG/
FARL    = 0x5558;          /*Load Add in FARL*/
FARH    = 0x0003;          /*Load Add in FARH*/
FDR0L   = 0x55AA;          /*Load Data in FDR0L*/
FDR0H   = 0x55AA;          /*Load Data in FDR0H*/
FDR1L   = 0xAA55;          /*Load Data in FDR1L*/
FDR1H   = 0xAA55;          /*Load Data in FDR1H*/
FCR0H  |= 0x8000;          /*Operation start*/
```

Double word program is always performed on the double word aligned on an even word: bit ADD2 of FARL is ignored.

Sector erase

Example: Sector erase of sectors B0F1 and B0F0 of Bank 0 in IFlash module.

```
FCR0H  |= 0x0800;          /*Set SER in FCR0H*/
FCR1L  |= 0x0003;          /*Set B0F1, B0F0*/
FCR0H  |= 0x8000;          /*Operation start*/
```

Suspend and resume

Word program, double word program, and sector erase operations can be suspended in the following way:

```
FCR0H  |= 0x4000;          /*Set SUSP in FCR0H*/
```

Then the operation can be resumed in the following way:

```
FCR0H  |= 0x0800;          /*Set SER in FCR0H*/
FCR0H  |= 0x8000;          /*Operation resume*/
```

Before resuming a suspended erase, FCR1H/FCR1L must be read to check if the erase is already completed (FCR1H = FCR1L = 0x0000 if erase is complete). Original setup of select operation bits in FCR0H/L must be restored before the operation resume, otherwise the operation is aborted and bit RESER of FER is set.

6 Bootstrap loader

The ST10F272M implements boot capabilities in order to:

- Support bootstrap via UART or bootstrap via CAN for the standard bootstrap
- Support a selective bootstrap loader, to manage the bootstrap sequence in a different way

6.1 Selection among user-code, standard or selective bootstrap

The boot modes are triggered with a special combination set on port0l[5...4]. Those signals, as other configuration signals, are latched on the rising edge of RSTIN pin.

- Decoding of reset configuration (P0L.5 = 1, P0L.4 = 1) selects the normal mode (also called User mode) and selects the user Flash to be mapped from address 00’0000h.
- Decoding of reset configuration (P0L.5 = 1, P0L.4 = 0) selects ST10 standard bootstrap mode (test-Flash is active and overlaps user Flash for code fetches from address 00'0000h; user Flash is active and available for read accesses).
- Decoding of reset configuration (P0L.5 = 0, P0L.4 = 1) activates new verifications to select which bootstrap software to execute:
  - if the user mode signature in the user Flash is programmed correctly, then a software reset sequence is selected and the user code is executed;
  - if the User mode signature is not programmed correctly in the user Flash, then the user key location is read again. Its value determines which communication channel will be enabled for bootstrapping.

Table 26. ST10F272M boot mode selection

P0.5	P0.4	ST10 decoding
1	1	User mode: User Flash mapped at 00’0000h
1	0	Standard bootstrap loader: User Flash mapped from 00’0000h, code fetches redirected to test-Flash at 00’0000h
0	1	Selective boot mode: User Flash mapped from 00’0000h, code fetches redirected to test-Flash at 00’0000h (different sequence execution compared to standard bootstrap loader)
0	0	Reserved

6.2 Standard bootstrap loader

After entering the standard BSL mode and the respective initialization, the ST10F272M scans the RxD0 line and the CAN1_RxD line to receive either a valid dominant bit from the CAN interface or a start condition from the UART line.

Start condition on UART RxD: ST10F272M starts standard bootstrap loader. This bootstrap loader is identical to that of other ST10 devices (example: ST10F269, ST10F168).

Valid dominant bit on CAN1 RxD: ST10F272M start bootstrapping via CAN1.

Caution: As both UART_RxD and CAN1_RxD lines are polled to detect a start of communication, ensure a stable level on the unused channel by adding a pull-up resistor.

Table 27. Standard instruction set summary (continued)

Mnemonic	Description	Bytes
J(N)B	Jump relative if direct bit is (not) set	4
JBC	Jump relative and clear bit if direct bit is set	4
JNBS	Jump relative and set bit if direct bit is not set	4
CALLA, CALLI, CALLR	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH, POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET	Return from intra-segment subroutine	2
RETS	Return from inter-segment subroutine	2
RETP	Return from intra-segment subroutine and pop direct word register from system stack	2
RETI	Return from interrupt service subroutine	2
SRST	Software reset	4
IDLE	Enter idle mode	4
PWRDN	Enter power-down mode (supposes $\overline{\text{NMI}}$-pin being low)	4
SRVWDT	Service watchdog timer	4
DISWDT	Disable watchdog timer	4
EINIT	Signify end-of-initialization on RSTOUT-pin	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended register sequence	2
EXTP(R)	Begin EXTended page (and register) sequence	2/4
EXTS(R)	Begin EXTended segment (and register) sequence	2/4
NOP	Null operation	2

8 External bus controller

All of the external memory accesses are performed by the on-chip external bus controller.

The EBC can be programmed to single chip mode when no external memory is required, or to one of four different external memory access modes:

- 16-/18-/20-/24-bit addresses and 16-bit data, demultiplexed
- 16-/18-/20-/24-bit addresses and 16-bit data, multiplexed
- 16-/18-/20-/24-bit addresses and 8-bit data, multiplexed
- 16-/18-/20-/24-bit addresses and 8-bit data, demultiplexed

In demultiplexed bus modes addresses are output on PORT1 and data is input/output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output.

Timing characteristics of the external bus interface (memory cycle time, memory tri-state time, length of ALE and read/write delay) are programmable giving the choice of a wide range of memories and external peripherals.

Up to four independent address windows may be defined (using register pairs ADDRSELx/BUSCONx) to access different resources and bus characteristics.

These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1.

All accesses to locations not covered by these four address windows are controlled by BUSCON0. Up to five external $\overline{CS}$ signals (four windows plus default) can be generated in order to save external glue logic. Access to very slow memories is supported by a ‘ready’ function.

A $\overline{HOLD}$/$\overline{HLDA}$ protocol is available for bus arbitration which shares external resources with other bus masters.

The bus arbitration is enabled by setting bit HLDEN in register PSW. After setting HLDEN once, pins P6.7...P6.5 ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) are automatically controlled by the EBC. In master mode (default after reset) the $\overline{HLDA}$ pin is an output. By setting bit DP6.7 to’1’ the slave mode is selected where pin $\overline{HLDA}$ is switched to input. This directly connects the slave controller to another master controller without glue logic.

For applications which require less external memory space, the address space can be restricted to 1 Mbyte, 256 Kbytes or to 64 Kbytes. Port 4 outputs all eight address lines if an address space of 16 Mbytes is used, otherwise four, two or no address lines.

Chip select timing can be made programmable. By default (after reset), the $\overline{CSx}$ lines change half a CPU clock cycle after the rising edge of ALE. With the CSCFG bit set in the SYSCON register the $\overline{CSx}$ lines change with the rising edge of ALE.

The active level of the $\overline{READY}$ pin can be set by bit RDYPOL in the BUSCONx registers. When the READY function is enabled for a specific address window, each bus cycle within the window must be terminated with the active level defined by bit RDYPOL in the associated BUSCON register.

Table 32. Compare modes

Compare modes	Function
Mode 0	Interrupt-only compare mode; several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; only one compare interrupt per timer period is generated
Mode 3	Pin set ‘1’ on match; pin reset ‘0’ on compare time overflow; only one compare event per timer period is generated
Double register mode	Two registers operate on one pin; pin toggles on each compare match; several compare events per timer period are possible.

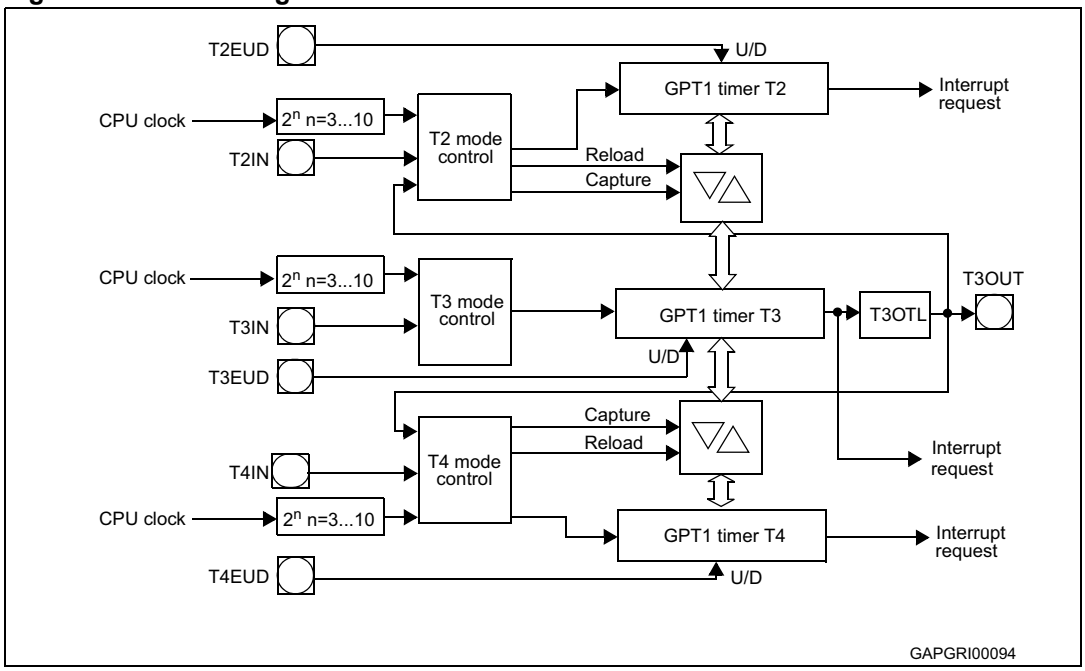
Table 33. CAPCOM timer input frequencies, resolutions and periods at 40 MHz

f_{CPU} = 40 MHz	Timer input selection TxI							
	000b	001b	010b	011b	100b	101b	110b	111b
Prescaler for f_{CPU}	8	16	32	64	128	256	512	1024
Input frequency	5 MHz	2.5 MHz	1.25 MHz	625 kHz	312.5 kHz	156.25 kHz	78.125 kHz	39.1 kHz
Resolution	200 ns	400 ns	0.8 µs	1.6 µs	3.2 µs	6.4 µs	12.8 µs	25.6 µs
Period	13.1 ms	26.2 ms	52.4 ms	104.8 ms	209.7 ms	419.4 ms	838.9 ms	1.678 s

Table 34. GPT1 timer input frequencies, resolutions and periods at 40 MHz

f_{CPU} = 40 MHz	Timer input selection T2I / T3I / T4I							
	000b	001b	010b	011b	100b	101b	110b	111b
Prescaler factor	8	16	32	64	128	256	512	1024
Input frequency	5 MHz	2.5 MHz	1.25 MHz	625 kHz	312.5 kHz	156.25 kHz	78.125 kHz	39.1 kHz
Resolution	200 ns	400 ns	0.8 µs	1.6 µs	3.2 µs	6.4 µs	12.8 µs	25.6 µs
Period maximum	13.1 ms	26.2 ms	52.4 ms	104.8 ms	209.7 ms	419.4 ms	838.9 ms	1.678 s

Figure 10. Block diagram of GPT1



13 Parallel ports

13.1 Introduction

The ST10F272M MCU provides up to 111 I/O lines with programmable features. These capabilities permit this MCU to be adapted to a wide range of applications.

ST10F272M has nine groups of I/O lines gathered as follows:

- Port 0 is a two time 8-bit port named P0L (low as less significant byte) and P0H (high as most significant byte)
- Port 1 is a two time 8-bit port named P1L and P1H
- Port 2 is a 16-bit port
- Port 3 is a 15-bit port (P3.14 line is not implemented)
- Port 4 is an 8-bit port
- Port 5 is a 16-bit port input only
- Port 6, Port 7 and Port 8 are 8-bit ports

These ports may be used as general purpose bidirectional input or output, software controlled with dedicated registers.

For example, the output drivers of six of the ports (2, 3, 4, 6, 7, 8) can be configured (bitwise) for push-pull or open drain operation using ODPx registers.

The input threshold levels are programmable (TTL/CMOS) for all the ports. The logic level of a pin is clocked into the input latch once per state time, regardless whether the port is configured for input or output. The threshold is selected with PICON and XPICON registers control bits.

A write operation to a port pin configured as an input causes the value to be written into the port output latch, while a read operation returns the latched state of the pin itself. A read-modify-write operation reads the value of the pin, modifies it, and writes it back to the output latch.

Writing to a pin configured as an output (DPx.y = ‘1’) causes the output latch and the pin to have the written value, since the output buffer is enabled. Reading this pin returns the value of the output latch. A read-modify-write operation reads the value of the output latch, modifies it, and writes it back to the output latch, thus also modifying the level at the pin.

I/O lines support an alternate function which is detailed in the following description of each port.

13.2 I/O’s special features

13.2.1 Open drain mode

Some of the I/O ports of ST10F272M support the open drain capability. This programmable feature may be used with an external pull-up resistor, in order to provide an AND wired logical function.

This feature is implemented for ports P2, P3, P4, P6, P7 and P8 (see respective sections), and is controlled through the respective open drain control registers ODPx.

This is done by setting or clearing the direction control bit DPx.y of the pin before enabling the alternate function.

There are port lines, however, where the direction of the port line is switched automatically.

For instance, in the multiplexed external bus modes of port0, the direction must be switched several times for an instruction fetch in order to output the addresses and to input the data.

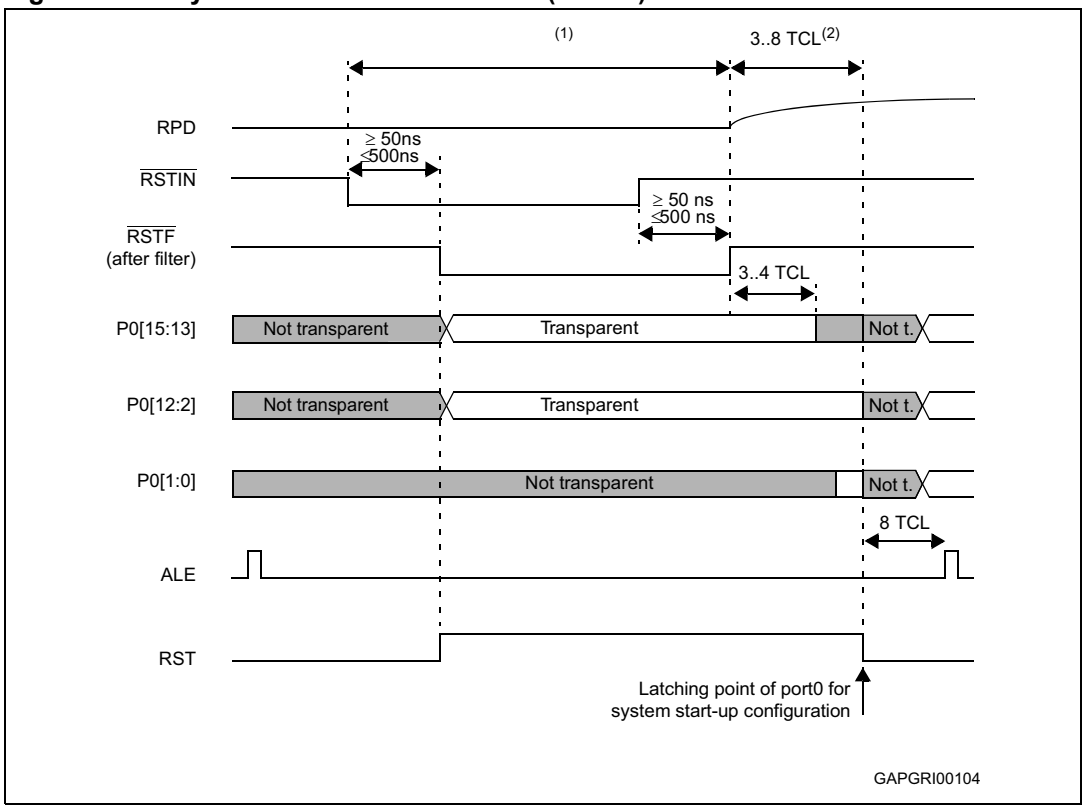
Obviously, this cannot be done through instructions. In these cases, the direction of the port line is switched automatically by hardware if the alternate function of such a pin is enabled.

To determine the appropriate level of the port output latches, check how the alternate data output is combined with the respective port latch output.

There is one basic structure for all port lines with only an alternate input function. Port lines with only an alternate output function, however, have different structures due to the way the direction of the pin is switched and depending on whether the pin is accessible by the user software or not in the alternate function mode.

All port lines that are not used for these alternate functions may be used as general purpose I/O lines.

Figure 20. Asynchronous hardware reset ($\overline{EA}$ = 0)



1. Longer than port0 settling time + PLL synchronization (if needed, that is P0(15:13) changed). Longer than 500 ns to take account input filter on RSTIN pin.
2. 3 to 8 TCL depending on clock source selection.

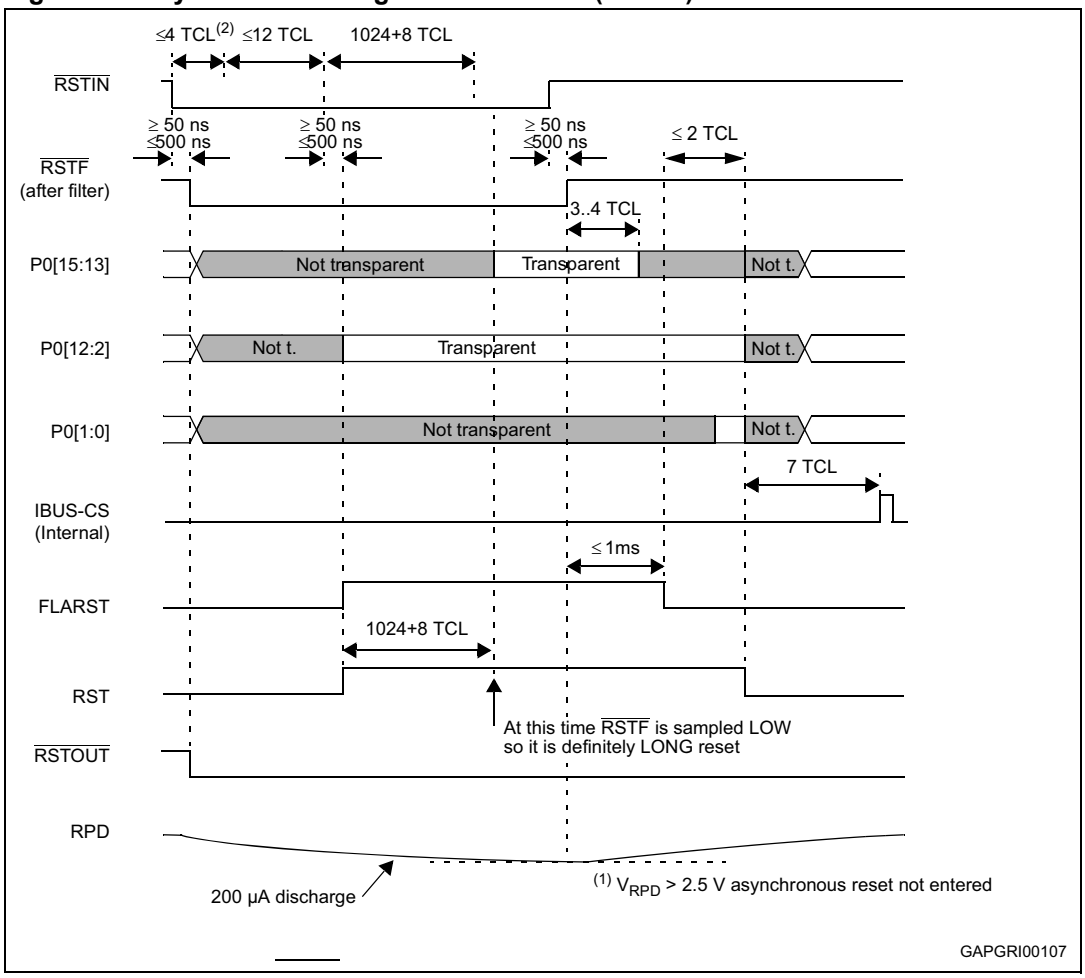
Exit from asynchronous reset state

When the $\overline{RSTIN}$ pin is pulled high, the device restarts: As already mentioned, if internal Flash is used, the restarting occurs after the embedded Flash initialization routine is completed. The system configuration is latched from Port0: ALE, $\overline{RD}$ and $\overline{WR}$/$\overline{WRL}$ pins are driven to their inactive level. The ST10F272M starts program execution from memory location 00'0000h in code segment 0. This starting location will typically point to the general initialization routine. The timings of asynchronous hardware reset sequence are summarized in *Figure 19* and *Figure 20*.

20.3 Synchronous reset (warm reset)

A synchronous reset is triggered when $\overline{RSTIN}$ pin is pulled low while RPD pin is at high level. In order to properly activate the internal reset logic of the device, the $\overline{RSTIN}$ pin must be held low, at least, during 4 TCL (two periods of CPU clock): Refer also to *Section 20.1* for details on minimum reset pulse duration. The I/O pins are set to high impedance and $\overline{RSTOUT}$ pin is driven low. After $\overline{RSTIN}$ level is detected, a short duration of a maximum of 12 TCL (six periods of CPU clock) elapses, during which pending internal hold states are cancelled and the current internal access cycle if any is completed. External bus cycle is aborted. The internal pull-down of $\overline{RSTIN}$ pin is activated if bit BDRSTEN of SYSCON register was previously set by software. Note that this bit is always cleared on power-on or after a reset sequence.

Figure 23. Synchronous long hardware reset ($\overline{EA}$ = 1)



1. If during the reset condition ($\overline{RSTIN}$ low), RPD voltage drops below the threshold voltage (about 2.5 V for 5V operation), the asynchronous reset is then immediately entered. Even if RPD returns above the threshold,the reset is defnitively taken as asynchronous.
2. Minimum $\overline{RSTIN}$ low pulse duration shall also be longer than 500 ns to guarantee the pulse is not masked by theinternal filter (refer to *Section 21.1*).

Figure 28. SW/WDT bidirectional reset ($\overline{EA}$ = 0)

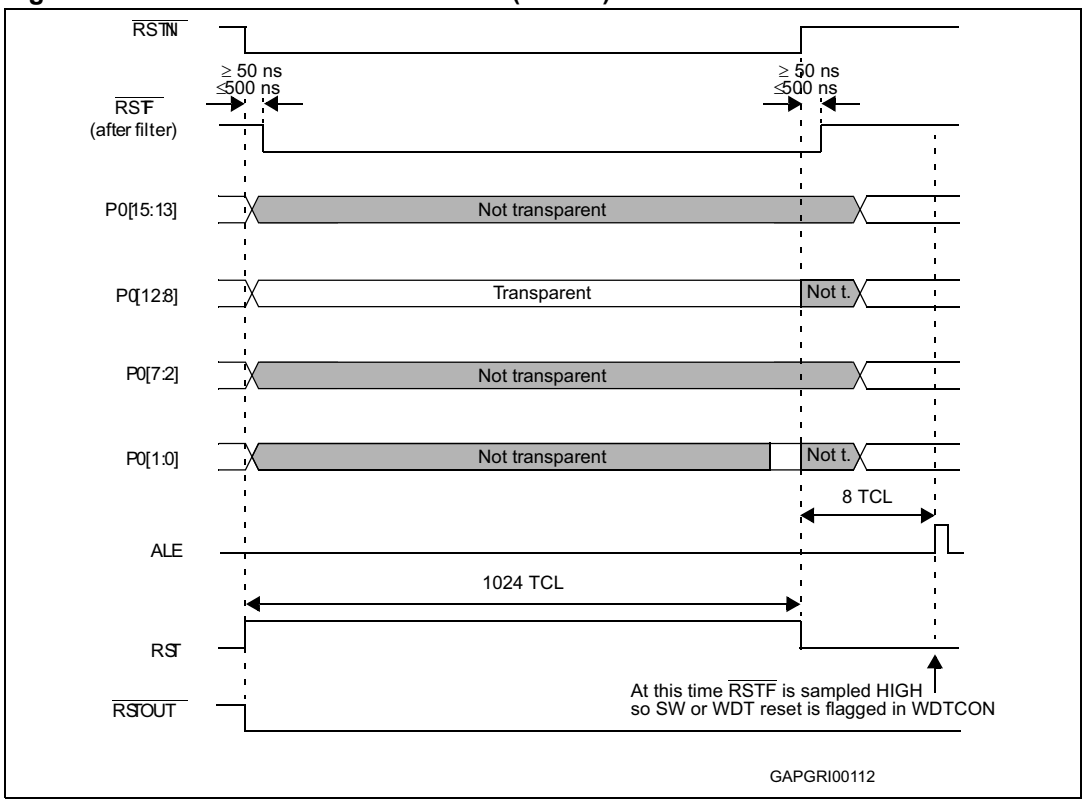
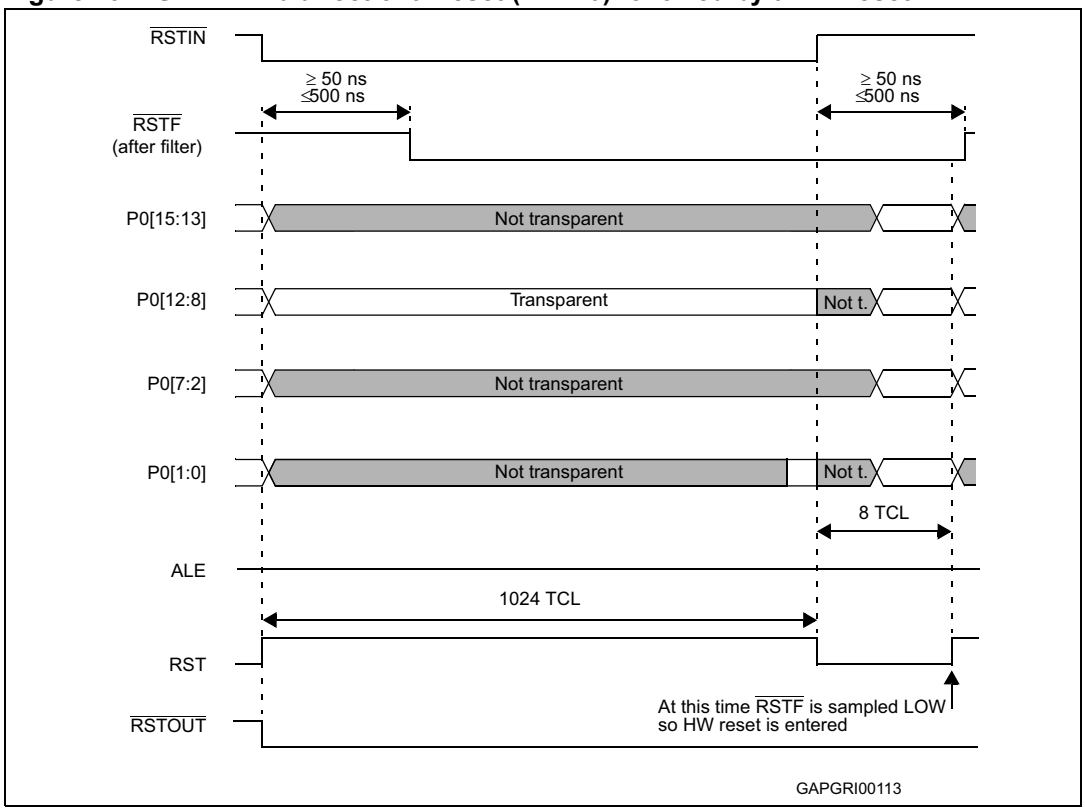


Figure 29. SW/WDT bidirectional reset ($\overline{EA}$ = 0) followed by a HW reset



20.8 Reset application examples

The next two timing diagrams (*Figure 33* and *Figure 34*) provide additional examples of bidirectional internal reset events (software and watchdog) including in particular the external capacitances charge and discharge transients (refer also to *Figure 31* for the external circuit scheme).

Figure 33. Example of software or watchdog bidirectional reset ($\overline{EA}$ = 1)

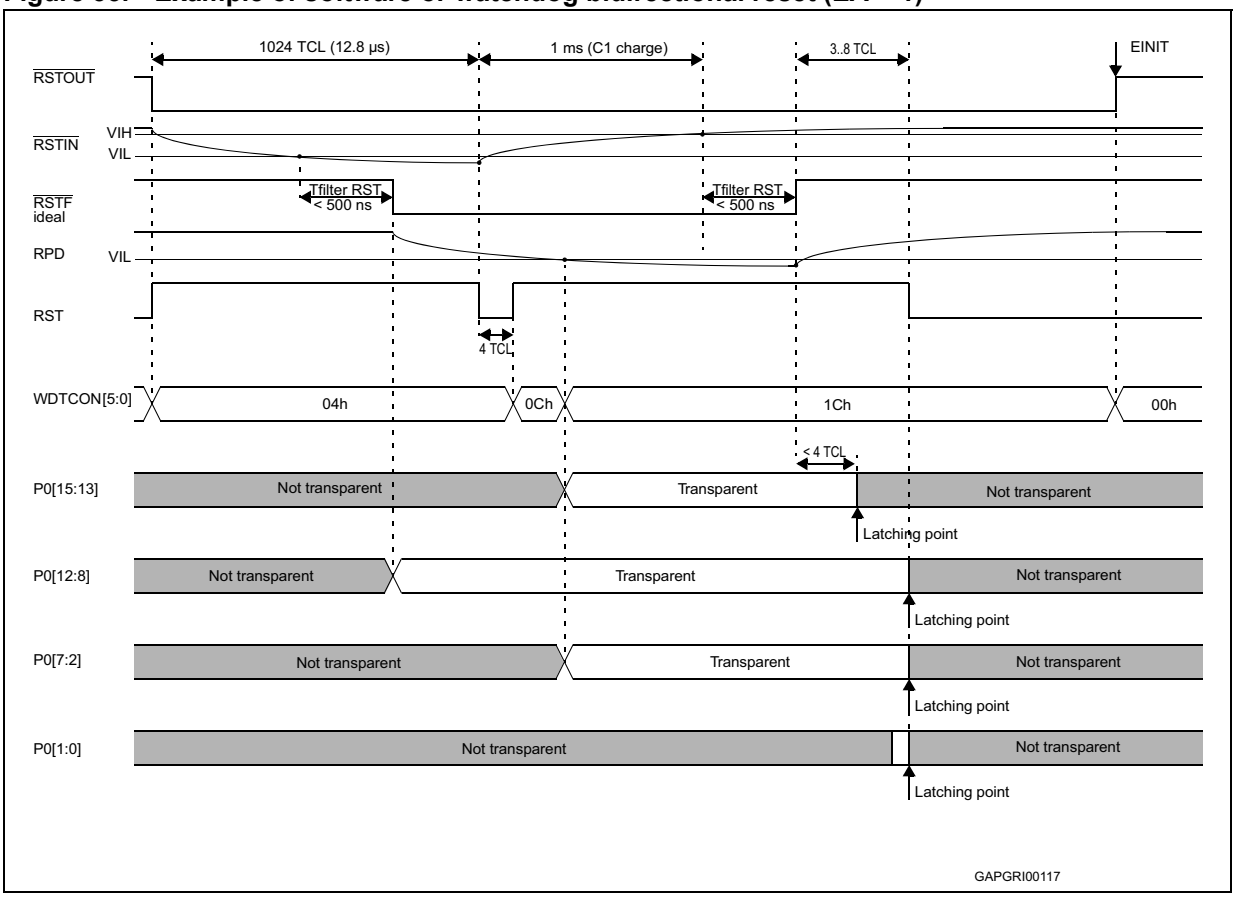


Table 42. Reset event (continued)

Event	RPD	$\overline{EA}$	Bidir	Synch. asynch.	RSTIN		WDTCON flags				
					Min	Max	PONR	LHWR	SHWR	SWR	WDTR
Software reset (2)	x	0	N	Synch.	Not activated		0	0	0	1	0
	x	0	N	Synch.	Not activated		0	0	0	1	0
	0	1	Y	Synch.	Not activated		0	0	0	1	0
	1	1	Y	Synch.	Activated by internal logic for 1024 TCL		0	0	0	1	0
Watchdog reset (2)	x	0	N	Synch.	Not activated		0	0	0	1	1
	x	0	N	Synch.	Not activated		0	0	0	1	1
	0	1	Y	Synch.	Not activated		0	0	0	1	1
	1	1	Y	Synch.	Activated by internal logic for 1024 TCL		0	0	0	1	1

1. It can degenerate into a long hardware reset and consequently differently flagged (see *Section 20.3* for details).
2. When bidirectional is active (and with RPD = 0), it can be followed by a short hardware reset and consequently differently flagged (see *Section 20.6* for details).

The start-up configurations and some system features are selected on reset sequences as described in *Table 43* and *Figure 35*.

Table 43 describes the system configuration latched on port0 in the six different reset modes. *Figure 35* summarizes the state of bits of PORT0 latched in RP0H, SYSCON, BUSCON0 registers.

Table 43. PORT0 latched configuration for the different reset events

X: Pin is sampled -: Pin is not sampled	Port0															
	Clock options			Segment address lines		Chip selects		WR configuration	Bus type		Reserved	BSL	Reserved	Reserved	Adapt mode	Emu mode
Sample event	P0H.7	P0H.6	P0H.5	P0H.4	P0H.3	P0H.2	P0H.1	P0H.0	P0L.7	P0L.6	P0L.5	P0L.4	P0L.3	P0L.2	P0L.1	P0L.0
Software reset	-	-	-	X	X	X	X	X	X	X	-	-	-	-	-	-
Watchdog reset	-	-	-	X	X	X	X	X	X	X	-	-	-	-	-	-
Synchronous short hardware reset	-	-	-	X	X	X	X	X	X	X	X	X	X	X	X	X
Synchronous long hardware reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Asynchronous hardware reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Asynchronous power-on reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 45. List of special function registers (continued)

Name	Physical address	8-bit address	Description	Reset value
DP1L**b**	F104h**E**	82h	P1L direction control register	- - 00h
DP1H**b**	F106h**E**	83h	P1h direction control register	- - 00h
DP2 **b**	FFC2h	E1h	Port 2 direction control register	0000h
DP3 **b**	FFC6h	E3h	Port 3 direction control register	0000h
DP4 **b**	FFCAh	E5h	Port 4 direction control register	- - 00h
DP6 **b**	FFCEh	E7h	Port 6 direction control register	- - 00h
DP7 **b**	FFD2h	E9h	Port 7 direction control register	- - 00h
DP8 **b**	FFD6h	EBh	Port 8 direction control register	- - 00h
DPP0	FE00h	00h	CPU data page pointer 0 register (10-bit)	0000h
DPP1	FE02h	01h	CPU data page pointer 1 register (10-bit)	0001h
DPP2	FE04h	02h	CPU data page pointer 2 register (10-bit)	0002h
DPP3	FE06h	03h	CPU data page pointer 3 register (10-bit)	0003h
EMUCON	FE0Ah	05h	Emulation control register	- - XXh
EXICON**b**	F1C0h**E**	E0h	External interrupt control register	0000h
EXISEL**b**	F1DAh**E**	EDh	External interrupt source selection register	0000h
IDCHIP	F07Ch**E**	3Eh	Device identifier register (n is the device revision)	110nh
IDMANUF	F07Eh**E**	3Fh	Manufacturer identifier register	0403h
IDMEM	F07Ah**E**	3Dh	On-chip memory identifier register	2040h
IDPROG	F078h**E**	3Ch	Programming voltage identifier register	0040h
IDX0**b**	FF08h	84h	MAC unit address pointer 0	0000h
IDX1**b**	FF0Ah	85h	MAC unit address pointer 1	0000h
MAH	FE5Eh	2Fh	MAC unit accumulator - high word	0000h
MAL	FE5Ch	2Eh	MAC unit accumulator - low word	0000h
MCW**b**	FFDCh	EEh	MAC unit control word	0000h
MDC**b**	FF0Eh	87h	CPU multiply divide control register	0000h
MDH	FE0Ch	06h	CPU multiply divide register – high word	0000h
MDL	FE0Eh	07h	CPU multiply divide register – low word	0000h
MRW**b**	FFDAh	EDh	MAC unit repeat word	0000h
MSW**b**	FFDEh	EFh	MAC unit status word	0200h
ODP2**b**	F1C2h**E**	E1h	Port 2 open drain control register	0000h
ODP3**b**	F1C6h**E**	E3h	Port 3 open drain control register	0000h
ODP4**b**	F1CAh**E**	E5h	Port 4 open drain control register	- - 00h
ODP6**b**	F1CEh**E**	E7h	Port 6 open drain control register	- - 00h
ODP7**b**	F1D2h**E**	E9h	Port 7 open drain control register	- - 00h

Table 59. A/D converter characteristics (continued)

Parameter	Symbol		Limit values		Unit	Test condition
			Min	Max		
Analog switch resistance(3)(8)	R_{SW}	CC	– –	600 1600	W	Port5 Port1
	R_{AD}	CC	–	1300	W	

1. V_{AREF} can be tied to ground when A/D converter is not in use. There is increased consumption (approximately 200 µA) on main V_{DD} due to internal analog circuitry not being completely turned off. Therefore, it is suggested to maintain the V_{AREF} at V_{DD} level even when not in use, and to eventually switch off the A/D converter circuitry setting bit ADOFF in ADCON register.
2. V_{AIN} may exceed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $0x000_H$ or $0x3FF_H$, respectively
3. Not 100% tested, guaranteed by design characterization
4. During the sample time the input capacitance C_{AIN} can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming and can be taken from *Table 60: A/D converter programming*.
5. This parameter includes the sample time t_S, the time for determining the digital result and the time to load the result register with the conversion result. Values for the conversion clock t_{CC} depend on programming and can be taken from the next *Table 60*.
6. DNL, INL, OFS and TUE are tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V, V_{DD} = 5.0 V. It is guaranteed by design characterization for all other voltages within the defined voltage range. 'LSB' has a value of V_{AREF}/1024. For port5 channels, the specified TUE (± 2 LSB) is guaranteed also with an overload condition (see I_{OV} specification) occurring on maximum 2 not selected analog input pins of port5 and the absolute sum of input overload currents on all Port5 analog input pins does not exceed 10 mA. For port1 channels, the specified TUE is guaranteed when no overload condition is applied to port1 pins: when an overload condition occurs on maximum 2 not selected analog input pins of port1 and the input positive overload current on all analog input pins does not exceed 10 mA (either dynamic or static injection), the specified TUE is degraded (± 7 LSB). To obtain the same accuracy, the negative injection current on port1 pins must not exceed -1mA in case of both dynamic and static injection.
7. The coupling factor is measured on a channel while an overload condition occurs on the adjacent not selected channels with the overload current within the different specified ranges (for both positive and negative injection current).
8. Refer to scheme shown in *Figure 40*.

24.7.1 Conversion timing control

When a conversion is started, first the capacitances of the converter are loaded via the respective analog input pin to the current analog input voltage. The time to load the capacitances is referred to as sample time. Next the sampled voltage is converted to a digital value several successive steps, which correspond to the 10-bit resolution of the ADC. During these steps the internal capacitances are repeatedly charged and discharged via the V_{AREF} pin.

The current that has to be drawn from the sources for sampling and changing charges depends on the time that each respective step takes, because the capacitors must reach their final voltage level within the given time, at least with a certain approximation. The maximum current, however, that a source can deliver, depends on its internal resistance.

The time that the two different actions during conversion take (sampling, and converting) can be programmed within a certain range in the ST10F272M relative to the CPU clock. The absolute time that is consumed by the different conversion steps therefore is independent from the general speed of the controller. This allows adjustment of the ST10F272M A/D converter to the system's properties:

Fast conversion can be achieved by programming the respective times to their absolute possible minimum. This is preferable for scanning high frequency signals. The internal resistance of analog source and analog supply must be sufficiently low, however.

High internal resistance can be achieved by programming the respective times to a higher value, or the possible maximum. This is preferable when using analog sources and supply with a high internal resistance in order to keep the current as low as possible. The conversion rate in this case may be considerably lower, however.

The conversion times are programmed via the upper four bits of register ADCON. Bit fields ADCTC and ADSTC are used to define the basic conversion time and in particular the partition between sample phase and comparison phases. The table below lists the possible combinations. The timings refer to the unit TCL, where f_{CPU} = 1/2 TCL. A complete conversion time includes the conversion itself, the sample time and the time required to transfer the digital value to the result register.

Table 60. A/D converter programming

ADCTC	ADSTC	Sample	Comparison	Extra	Total conversion
00	00	TCL * 120	TCL * 240	TCL * 28	TCL * 388
00	01	TCL * 140	TCL * 280	TCL * 16	TCL * 436
00	10	TCL * 200	TCL * 280	TCL * 52	TCL * 532
00	11	TCL * 400	TCL * 280	TCL * 44	TCL * 724
11	00	TCL * 240	TCL * 480	TCL * 52	TCL * 772
11	01	TCL * 280	TCL * 560	TCL * 28	TCL * 868
11	10	TCL * 400	TCL * 560	TCL * 100	TCL * 1060
11	11	TCL * 800	TCL * 560	TCL * 52	TCL * 1444
10	00	TCL * 480	TCL * 960	TCL * 100	TCL * 1540
10	01	TCL * 560	TCL * 1120	TCL * 52	TCL * 1732
10	10	TCL * 800	TCL * 1120	TCL * 196	TCL * 2116
10	11	TCL * 1600	TCL * 1120	TCL * 164	TCL * 2884

Note: The total conversion time is compatible with the formula valid for ST10F269, while the meaning of the bit fields ADCTC and ADSTC is no longer compatible: the minimum conversion time is 388 TCL, which at 40 MHz CPU frequency corresponds to 4.85 µs (see ST10F269).

24.7.2 A/D conversion accuracy

The A/D converter compares the analog voltage sampled on the selected analog input channel to its analog reference voltage (V_{AREF}) and converts it into 10-bit digital data. The absolute accuracy of the A/D conversion is the deviation between the input analog value and the output digital value. It includes the following errors:

- Offset error (OFS)
- Gain error (GE)
- Quantization error
- Nonlinearity error (differential and integral)

Table 71. Demultiplexed bus timings (continued)

Symbol		Parameter	f_{CPU} = 40 MHz TCL = 12.5 ns		Variable CPU clock 1/2 TCL = 1 to 40 MHz		Unit
			Min	Max	Min	Max	
t_{41}	CC	Latched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	2 + t_F	–	TCL - 10.5 + t_F	–	ns
t_{82}	CC	Address setup to $\overline{RdCS}$, $\overline{WrCS}$ (with RW-delay)	14 + 2t_A	–	2TCL - 11 + 2t_A	–	ns
t_{83}	CC	Address setup to $\overline{RdCS}$, $\overline{WrCS}$ (no RW-delay)	2 + 2t_A	–	TCL - 10.5 + 2 t_A	–	ns
t_{46}	SR	$\overline{RdCS}$ to valid data in (with RW-delay)	–	4 + t_C	–	2TCL - 21 + t_C	ns
t_{47}	SR	$\overline{RdCS}$ to valid data in (no RW-delay)	–	16.5 + t_C	–	3TCL - 21 + t_C	ns
t_{48}	CC	$\overline{RdCS}$, $\overline{WrCS}$ low time (with RW-delay)	15.5 + t_C	–	2TCL - 9.5 + t_C	–	ns
t_{49}	CC	$\overline{RdCS}$, $\overline{WrCS}$ low time (no RW-delay)	28 + t_C	–	3TCL - 9.5 + t_C	–	ns
t_{50}	CC	Data valid to $\overline{WrCS}$	10 + t_C	–	2TCL - 15 + t_C	–	ns
t_{51}	SR	Data hold after $\overline{RdCS}$	0	–	0	–	ns
t_{53}	SR	Data float after $\overline{RdCS}$ (with RW-delay)(3)	–	16.5 + t_F	–	2TCL - 8.5 + t_F	ns
t_{68}	SR	Data float after $\overline{RdCS}$ (no RW-delay)(3)	–	4 + t_F	–	TCL - 8.5 + t_F	ns
t_{55}	CC	Address hold after $\overline{RdCS}$, $\overline{WrCS}$	-8.5 + t_F	–	-8.5 + t_F	–	ns
t_{57}	CC	Data hold after $\overline{WrCS}$	2 + t_F	–	TCL - 10.5 + t_F	–	ns

1. RW-delay and t_A refer to the next following bus cycle.
2. Read data is latched with the same clock edge that triggers the address change and the rising $\overline{RD}$ edge. Therefore address changes before the end of $\overline{RD}$ have no impact on read cycles.
3. Partially tested, guaranteed by design characterization.