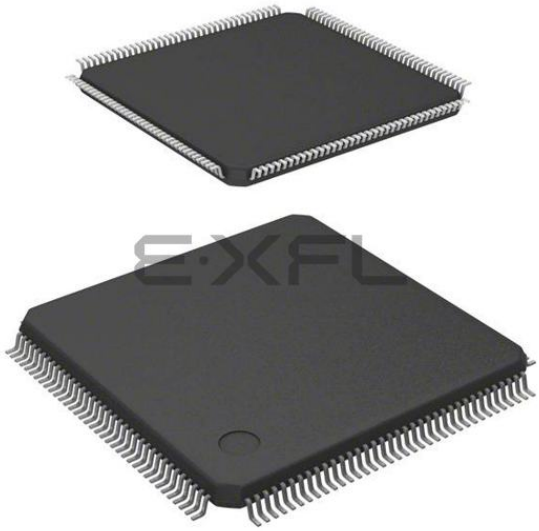

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST10
Core Size	16-Bit
Speed	40MHz
Connectivity	ASC, CANbus, EBI/EMI, I²C, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st10f272m-4tr3

Table 5 above refers to the configuration when bit ROMS1 of SYSCON register is set. Refer to the device user manual for more details on the memory mapping during bootstrap mode. In particular, when bootstrap mode is entered:

- Test-Flash is seen and available for code fetches (address 00'0000h)
- User IFlash is only available for read and write accesses
- Write accesses must be made with addresses starting in segment 1 from 01'0000h, whatever ROMS1 bit in SYSCON value
- Read accesses are made in segment 0 or in segment 1 depending of ROMS1 value.

In bootstrap mode, by default ROMS1 = 0, so the first 32 Kbytes of IFlash are mapped in segment 0.

Example:
In default configuration, to program address 0, the user must put the value 01'0000h in the FARL and FARH registers but to verify the content of the address 0, a read to 00'0000h must be performed.

The next *Table 6* shows the control register interface composition: This set of registers can be addressed by the CPU.

Table 6. Control register interface

Name	Description	Addresses	Size
FCR1-0	Flash control registers 1-0	0x0008 0000 - 0x0008 0007	8 bytes
FDR1-0	Flash data registers 1-0	0x0008 0008 - 0x0008 000F	8 bytes
FAR	Flash address registers	0x0008 0010 - 0x0008 0013	4 bytes
FER	Flash error register	0x0008 0014 - 0x0008 0015	2 bytes
FNVWPIR	Flash non-volatile protection i register	0x0008 DFB0 - 0x0008 DFB1	2 bytes
FNVPIR-Mirror	Mirror of Flash non-volatile protection i register	0x0008 DFB4 - 0x0008 DFB5	2 bytes
FNVAPR0	Flash non-volatile access protection register 0	0x0008 DFB8 - 0x0008 DFB9	2 bytes
FNVAPR1	Flash non-volatile access protection register 1	0x0008 DFBC - 0x0008 DFBF	4 bytes
XFVTAUR0	X-bus Flash volatile temporary access unprotection register 0	0x0000 EB50 - 0x0000 EB51	2 bytes

5.2.3 Low power mode

The Flash module is automatically switched off executing PWRDN instruction. The consumption is drastically reduced, but exiting this state can require a long time (t_{PD}).

Recovery time from power-down mode for the Flash modules is anyway shorter than the main oscillator start-up time. To avoid any problem in restarting to fetch code from the Flash, it is important to size properly the external circuit on RPD pin.

Note: PWRDN instruction must not be executed while a Flash program/erase operation is in progress.

Table 29. Interrupt sources (continued)

Source of interrupt or PEC service request	Request flag	Enable flag	Interrupt vector	Vector location	Trap number
GPT2 timer 6	T6IR	T6IE	T6INT	00'0098h	26h
GPT2 CAPREL register	CRIR	CRIE	CRINT	00'009Ch	27h
A/D conversion complete	ADCIR	ADCIE	ADCINT	00'00A0h	28h
A/D overrun error	ADEIR	ADEIE	ADEINT	00'00A4h	29h
ASC0 transmit	S0TIR	S0TIE	S0TINT	00'00A8h	2Ah
ASC0 transmit buffer	S0TBIR	S0TBIE	S0TBINT	00'011Ch	47h
ASC0 receive	S0RIR	S0RIE	S0RINT	00'00ACh	2Bh
ASC0 error	S0EIR	S0EIE	S0EINT	00'00B0h	2Ch
SSC transmit	SCTIR	SCTIE	SCTINT	00'00B4h	2Dh
SSC receive	SCRIR	SCRIE	SCRINT	00'00B8h	2Eh
SSC error	SCEIR	SCEIE	SCEINT	00'00BCh	2Fh
PWM channel 0...3	PWMIR	PWMIE	PWMINT	00'00FCh	3Fh
See *Section 9.1*	XP0IR	XP0IE	XP0INT	00'0100h	40h
See *Section 9.1*	XP1IR	XP1IE	XP1INT	00'0104h	41h
See *Section 9.1*	XP2IR	XP2IE	XP2INT	00'0108h	42h
See *Section 9.1*	XP3IR	XP3IE	XP3INT	00'010Ch	43h

Hardware traps are exceptions or error conditions that arise during run-time. They cause immediate non-maskable system reaction similar to a standard interrupt service (branching to a dedicated vector table location).

The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). A hardware trap will interrupt any other program execution except when another higher prioritized trap service is in progress. Hardware trap services cannot not be interrupted by a standard interrupt or by PEC interrupts.

9.1 X-peripheral interrupt

The limited number of X-bus interrupt lines of the present ST10 architecture, imposes some constraints on the implementation of the new functionality. In particular, the additional X-peripherals SSC1, ASC1, I^2C, PWM1 and RTC need some resources to implement interrupt and PEC transfer capabilities. For this reason, a multiplexed structure for the interrupt management is proposed. In *Figure 9*, the principle is explained through a simple diagram, which shows the basic structure replicated for each of the four X-interrupt available vectors (XP0INT, XP1INT, XP2INT and XP3INT).

It is based on a set of 16-bit registers XIRxSEL (x = 0,1,2,3), divided in two portions each:

- Byte high XIRxSEL[15:8] Interrupt enable bits
- Byte low XIRxSEL[7:0] Interrupt flag bits

When different sources submit an interrupt request, the enable bits (byte high of XIRxSEL register) define a mask which controls which sources will be associated with the unique available vector. If more than one source is enabled to issue the request, the service routine will have to take care to identify the real event to be serviced. This can easily be done by checking the flag bits (byte low of XIRxSEL register). Note that the flag bits can also provide information about events which are not currently serviced by the interrupt controller (since they are masked through the enable bits), allowing an effective software management even if the related interrupt request cannot be served: A periodic polling of the flag bits may be implemented inside the user application.

Figure 9. X-interrupt basic structure

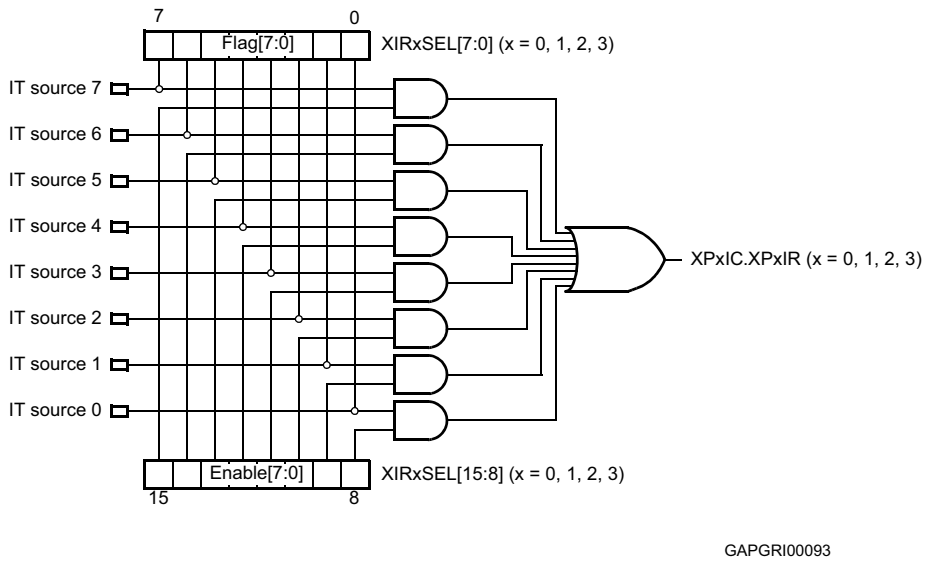
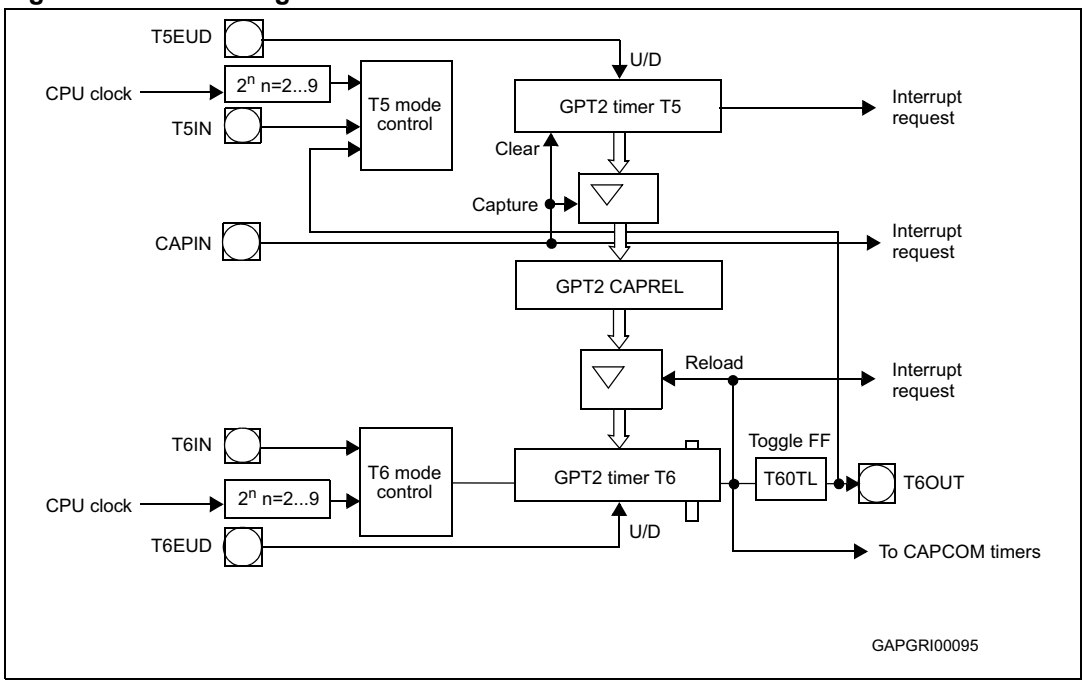


Table 30 summarizes the mapping of the different interrupt sources which shares the four X-interrupt vectors.

Table 30. X-interrupt detailed mapping

Interrupt source	XP0INT	XP1INT	XP2INT	XP3INT
CAN1 interrupt	x			x
CAN2 interrupt		x		x
I^2C receive	x	x	x	
I^2C transmit	x	x	x	
I^2C error				x
SSC1 receive	x	x	x	
SSC1 transmit	x	x	x	
SSC1 error				x
ASC1 receive	x	x	x	
ASC1 transmit	x	x	x	

Figure 11. Block diagram of GPT2



13 Parallel ports

13.1 Introduction

The ST10F272M MCU provides up to 111 I/O lines with programmable features. These capabilities permit this MCU to be adapted to a wide range of applications.

ST10F272M has nine groups of I/O lines gathered as follows:

- Port 0 is a two time 8-bit port named P0L (low as less significant byte) and P0H (high as most significant byte)
- Port 1 is a two time 8-bit port named P1L and P1H
- Port 2 is a 16-bit port
- Port 3 is a 15-bit port (P3.14 line is not implemented)
- Port 4 is an 8-bit port
- Port 5 is a 16-bit port input only
- Port 6, Port 7 and Port 8 are 8-bit ports

These ports may be used as general purpose bidirectional input or output, software controlled with dedicated registers.

For example, the output drivers of six of the ports (2, 3, 4, 6, 7, 8) can be configured (bitwise) for push-pull or open drain operation using ODPx registers.

The input threshold levels are programmable (TTL/CMOS) for all the ports. The logic level of a pin is clocked into the input latch once per state time, regardless whether the port is configured for input or output. The threshold is selected with PICON and XPICON registers control bits.

A write operation to a port pin configured as an input causes the value to be written into the port output latch, while a read operation returns the latched state of the pin itself. A read-modify-write operation reads the value of the pin, modifies it, and writes it back to the output latch.

Writing to a pin configured as an output (DPx.y = ‘1’) causes the output latch and the pin to have the written value, since the output buffer is enabled. Reading this pin returns the value of the output latch. A read-modify-write operation reads the value of the output latch, modifies it, and writes it back to the output latch, thus also modifying the level at the pin.

I/O lines support an alternate function which is detailed in the following description of each port.

13.2 I/O’s special features

13.2.1 Open drain mode

Some of the I/O ports of ST10F272M support the open drain capability. This programmable feature may be used with an external pull-up resistor, in order to provide an AND wired logical function.

This feature is implemented for ports P2, P3, P4, P6, P7 and P8 (see respective sections), and is controlled through the respective open drain control registers ODPx.

Table 39. Synchronous baudrate and reload values (f_{CPU} = 40 MHz)

Baudrate	Bit time	Reload value
Reserved	-	0000h
Can be used only with f_{CPU} = 32 MHz (or lower)	-	0001h
6.6 Mbaud	150 ns	0002h
5 Mbaud	200 ns	0003h
2.5 Mbaud	400 ns	0007h
1 Mbaud	1 µs	0013h
100 Kbaud	10 µs	00C7h
10 Kbaud	100 µs	07CFh
1 Kbaud	1 ms	4E1Fh
306 baud	3.26 ms	FF4Eh

Warning: **It is recommended to provide the external hardware with a current limitation circuitry. This is necessary to avoid permanent damage of the device during the power-on transient, when the capacitance on V_{18} pin is charged. For the on-chip voltage regulator functionality 10nF is sufficient: In any case, a maximum of 100 nF on V_{18} pin should not generate problems of over-current (higher value is allowed if current is limited by the external hardware). External current limitation is nevertheless also recommended to avoid risks of damage in case of a temporary short between V_{18} and ground: The internal 1.8 V drivers are sized to drive currents of several tens of Amps, so the current must be limited by the external hardware. The limit of current is imposed by power dissipation considerations (refer to *Section 24: Electrical characteristics*).**

In figures *17* and *18* below, asynchronous power-on timing diagrams are shown, with boot from internal or external memory respectively, highlighting the reset phase extension introduced by the embedded Flash module when selected.

Caution: Never power the device without keeping the RSTIN pin grounded: The device could enter into unpredictable states, risking also permanent damage.

or watchdog reset become a short hardware reset. On the contrary, if $\overline{RSTF}$ remains low for less than 4 TCL, the device simply exits reset state.

The bidirectional reset is not effective in case RPD is held low, when a software or watchdog reset event occurs. On the contrary, if a software or watchdog bidirectional reset event is active and RPD becomes low, the $\overline{RSTIN}$ pin is immediately released, while the internal reset sequence is completed regardless of RPD status change (1024 TCL).

Note: The bidirectional reset function is disabled by any reset sequence (bit BDRSTEN of SYSCON is cleared). To be activated again it must be enabled during the initialization routine.

WDTCON flags

Similar to what is highlighted in the previous section, when discussing short reset and the degeneration into long reset, comparable situations may occur when bidirectional reset is enabled. The presence of the internal filter on $\overline{RSTIN}$ pin introduces a delay: When $\overline{RSTIN}$ is released, the internal signal after the filter (see $\overline{RSTF}$ in the drawings) is delayed, so it remains still active (low) for a while. It means that depending on the internal clock speed, a short reset may be recognized as a long reset: The WDTCON flags are set accordingly.

Moreover, when either software or watchdog bidirectional reset events occur, when the $\overline{RSTIN}$ pin is released (at the end of the internal reset sequence), the $\overline{RSTF}$ internal signal (after the filter) remains low for a while, and depending on the clock frequency it is recognized high or low: 8TCL after the completion of the internal sequence, the level of $\overline{RSTF}$ signal is sampled, and if recognized still low a hardware reset sequence starts, and WDTCON will flag this last event, masking the previous one (software or watchdog reset). Typically, a short hardware reset is recognized, unless the $\overline{RSTIN}$ pin (and consequently internal signal $\overline{RSTF}$) is sufficiently held low by the external hardware to inject a long hardware reset. After this occurrence, the initialization routine is not able to recognize a software or watchdog bidirectional reset event, since a different source is flagged inside WDTCON register. This phenomenon does not occur when internal Flash is selected during reset ($\overline{EA}$ = 1), since the initialization of the Flash itself extend the internal reset duration well beyond the filter delay.

Figures *Figure 27*, *Figure 28* and *Figure 29* summarize the timing for software and watchdog timer bidirectional reset events: In particular *Figure 29* shows the degeneration into hardware reset.

Table 42. Reset event (continued)

Event	RPD	$\overline{EA}$	Bidir	Synch. asynch.	RSTIN		WDTCON flags				
					Min	Max	PONR	LHWR	SHWR	SWR	WDTR
Software reset (2)	x	0	N	Synch.	Not activated		0	0	0	1	0
	x	0	N	Synch.	Not activated		0	0	0	1	0
	0	1	Y	Synch.	Not activated		0	0	0	1	0
	1	1	Y	Synch.	Activated by internal logic for 1024 TCL		0	0	0	1	0
Watchdog reset (2)	x	0	N	Synch.	Not activated		0	0	0	1	1
	x	0	N	Synch.	Not activated		0	0	0	1	1
	0	1	Y	Synch.	Not activated		0	0	0	1	1
	1	1	Y	Synch.	Activated by internal logic for 1024 TCL		0	0	0	1	1

1. It can degenerate into a long hardware reset and consequently differently flagged (see *Section 20.3* for details).
2. When bidirectional is active (and with RPD = 0), it can be followed by a short hardware reset and consequently differently flagged (see *Section 20.6* for details).

The start-up configurations and some system features are selected on reset sequences as described in *Table 43* and *Figure 35*.

Table 43 describes the system configuration latched on port0 in the six different reset modes. *Figure 35* summarizes the state of bits of PORT0 latched in RP0H, SYSCON, BUSCON0 registers.

Table 43. PORT0 latched configuration for the different reset events

X: Pin is sampled -: Pin is not sampled	Port0															
	Clock options			Segment address lines		Chip selects		WR configuration	Bus type		Reserved	BSL	Reserved	Reserved	Adapt mode	Emu mode
Sample event	P0H.7	P0H.6	P0H.5	P0H.4	P0H.3	P0H.2	P0H.1	P0H.0	P0L.7	P0L.6	P0L.5	P0L.4	P0L.3	P0L.2	P0L.1	P0L.0
Software reset	-	-	-	X	X	X	X	X	X	X	-	-	-	-	-	-
Watchdog reset	-	-	-	X	X	X	X	X	X	X	-	-	-	-	-	-
Synchronous short hardware reset	-	-	-	X	X	X	X	X	X	X	X	X	X	X	X	X
Synchronous long hardware reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Asynchronous hardware reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Asynchronous power-on reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 45. List of special function registers (continued)

Name	Physical address	8-bit address	Description	Reset value
CC4IC**b**	FF80h	C0h	CAPCOM register 4 interrupt control register	- - 00h
CC5	FE8Ah	45h	CAPCOM register 5	0000h
CC5IC**b**	FF82h	C1h	CAPCOM register 5 interrupt control register	- - 00h
CC6	FE8Ch	46h	CAPCOM register 6	0000h
CC6IC**b**	FF84h	C2h	CAPCOM register 6 interrupt control register	- - 00h
CC7	FE8Eh	47h	CAPCOM register 7	0000h
CC7IC**b**	FF86h	C3h	CAPCOM register 7 interrupt control register	- - 00h
CC8	FE90h	48h	CAPCOM register 8	0000h
CC8IC**b**	FF88h	C4h	CAPCOM register 8 interrupt control register	- - 00h
CC9	FE92h	49h	CAPCOM register 9	0000h
CC9IC**b**	FF8Ah	C5h	CAPCOM register 9 interrupt control register	- - 00h
CC10	FE94h	4Ah	CAPCOM register 10	0000h
CC10IC**b**	FF8Ch	C6h	CAPCOM register 10 interrupt control register	- - 00h
CC11	FE96h	4Bh	CAPCOM register 11	0000h
CC11IC**b**	FF8Eh	C7h	CAPCOM register 11 interrupt control register	- - 00h
CC12	FE98h	4Ch	CAPCOM register 12	0000h
CC12IC**b**	FF90h	C8h	CAPCOM register 12 interrupt control register	- - 00h
CC13	FE9Ah	4Dh	CAPCOM register 13	0000h
CC13IC**b**	FF92h	C9h	CAPCOM register 13 interrupt control register	- - 00h
CC14	FE9Ch	4Eh	CAPCOM register 14	0000h
CC14IC**b**	FF94h	CAh	CAPCOM register 14 interrupt control register	- - 00h
CC15	FE9Eh	4Fh	CAPCOM register 15	0000h
CC15IC**b**	FF96h	CBh	CAPCOM register 15 interrupt control register	- - 00h
CC16	FE60h	30h	CAPCOM register 16	0000h
CC16IC**b**	F160h**E**	B0h	CAPCOM register 16 interrupt control register	- - 00h
CC17	FE62h	31h	CAPCOM register 17	0000h
CC17IC**b**	F162h**E**	B1h	CAPCOM register 17 interrupt control register	- - 00h
CC18	FE64h	32h	CAPCOM register 18	0000h
CC18IC**b**	F164h**E**	B2h	CAPCOM register 18 interrupt control register	- - 00h
CC19	FE66h	33h	CAPCOM register 19	0000h
CC19IC**b**	F166h**E**	B3h	CAPCOM register 19 interrupt control register	- - 00h
CC20	FE68h	34h	CAPCOM register 20	0000h
CC20IC**b**	F168h**E**	B4h	CAPCOM register 20 interrupt control register	- - 00h
CC21	FE6Ah	35h	CAPCOM register 21	0000h

Table 45. List of special function registers (continued)

Name	Physical address	8-bit address	Description	Reset value
PW2	FE34h	1Ah	PWM module pulse width register 2	0000h
PW3	FE36h	1Bh	PWM module pulse width register 3	0000h
PWMCON0**b**	FF30h	98h	PWM module control register 0	0000h
PWMCON1**b**	FF32h	99h	PWM module control register 1	0000h
PWMIC**b**	F17Eh**E**	BFh	PWM module interrupt control register	- - 00h
QR0	F004h**E**	02h	MAC unit offset register r0	0000h
QR1	F006h**E**	03h	MAC unit offset register R1	0000h
QX0	F000h**E**	00h	MAC unit offset register X0	0000h
QX1	F002h**E**	01h	MAC unit offset register X1	0000h
RP0H**b**	F108h**E**	84h	System start-up configuration register (read only)	- - XXh
S0BG	FEB4h	5Ah	Serial channel 0 baudrate generator reload register	0000h
S0CON**b**	FFB0h	D8h	Serial channel 0 control register	0000h
S0EIC**b**	FF70h	B8h	Serial channel 0 error interrupt control register	- - 00h
S0RBUF	FEB2h	59h	Serial channel 0 receive buffer register (read only)	- - XXh
S0RIC**b**	FF6Eh	B7h	Serial channel 0 receive interrupt control register	- - 00h
S0TBIC**b**	F19Ch**E**	CEh	Serial channel 0 transmit buffer interrupt control reg.	- - 00h
S0TBUF	FEB0h	58h	Serial channel 0 transmit buffer register (write only)	0000h
S0TIC**b**	FF6Ch	B6h	Serial channel 0 transmit interrupt control register	- - 00h
SP	FE12h	09h	CPU system stack pointer register	FC00h
SSCBR	F0B4h**E**	5Ah	SSC baudrate register	0000h
SSCCON**b**	FFB2h	D9h	SSC control register	0000h
SSCEIC**b**	FF76h	BBh	SSC error interrupt control register	- - 00h
SSCRB	F0B2h**E**	59h	SSC receive buffer (read only)	XXXXh
SSCRIC**b**	FF74h	BAh	SSC receive interrupt control register	- - 00h
SSCTB	F0B0h**E**	58h	SSC transmit buffer (write only)	0000h
SSCTIC**b**	FF72h	B9h	SSC transmit interrupt control register	- - 00h
STKOV	FE14h	0Ah	CPU stack overflow pointer register	FA00h
STKUN	FE16h	0Bh	CPU stack underflow pointer register	FC00h
SYSCON**b**	FF12h	89h	CPU system configuration register	0xx0h(1)
T0	FE50h	28h	CAPCOM timer 0 register	0000h
T01CON**b**	FF50h	A8h	CAPCOM timer 0 and timer 1 control register	0000h
T0IC**b**	FF9Ch	CEh	CAPCOM timer 0 interrupt control register	- - 00h
T0REL	FE54h	2Ah	CAPCOM timer 0 reload register	0000h
T1	FE52h	29h	CAPCOM timer 1 register	0000h

Table 46. List of X-bus registers (continued)

Name	Physical address	Description	Reset value
XPWMCON1SET	EC0Ah	XPWM module set control register 0 (write only)	0000h
XPWMPORT	EC80h	XPWM module port control register	0000h
XS1BG	E906h	XASC baudrate generator reload register	0000h
XS1CON	E900h	XASC control register	0000h
XS1CONCLR	E904h	XASC clear control register (write only)	0000h
XS1CONSET	E902h	XASC set control register (write only)	0000h
XS1PORT	E980h	XASC port control register	0000h
XS1RBUF	E90Ah	XASC receive buffer register	0000h
XS1TBUF	E908h	XASC transmit buffer register	0000h
XSSCBR	E80Ah	XSSC baudrate register	0000h
XSSCCON	E800h	XSSC control register	0000h
XSSCCONCLR	E804h	XSSC clear control register (write only)	0000h
XSSCCONSET	E802h	XSSC set control register (write only)	0000h
XSSCPORT	E880h	XSSC port control register	0000h
XSSCRB	E808h	XSSC receive buffer	XXXXh
XSSCTB	E806h	XSSC transmit buffer	0000h

Table 54. Thermal characteristics

Symbol	Description	Value (typical)	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP 144 - 20 x 20 mm/0.5 mm pitch LQFP 144 - 20 x 20 mm/0.5 mm pitch on four-layer FR4 board (2 layers signals/2 layers power)	40 35	°C/W

Based on thermal characteristics of the package and with reference to the power consumption figures provided in the next tables and diagrams, the following product classification can be proposed. However, the exact power consumption of the device inside the application must be computed according to different working conditions, thermal profiles, real thermal resistance of the system (including printed circuit board or other substrata), I/O activity, and so on.

Table 55. Package characteristics

Package	Ambient temperature range	CPU frequency range
LQFP 144	-40 to +125°C	1 to 40 MHz

24.4 Parameter interpretation

The parameters listed in the following tables represent the characteristics of the ST10F272M and its demands on the system.

Where the ST10F272M logic provides signals with their respective timing characteristics, the symbol '**CC**' for controller characteristics, is included in the 'Symbol' column. Where the external system must provide signals with their respective timing characteristics to the ST10F272M, the symbol '**SR**' for system requirement, is included in the 'Symbol' column.

24.8.16 Multiplexed bus

V_{DD} = 5 V ± 10 %, V_{SS} = 0 V, T_A = -40 to +125 °C, CL = 50 pF,
ALE cycle time = 6 TCL + $2t_A$ + t_C + t_F (75 ns at 40 MHz CPU clock without wait states)

Table 70. Multiplexed bus timings

Symbol		Parameter	f_{CPU} = 40 MHz TCL = 12.5 ns		Variable CPU clock 1/2 TCL = 1 to 40 MHz		Unit
			Min	Max	Min	Max	
t_5	CC	ALE high time	4 + t_A	–	TCL – 8.5 + t_A	–	ns
t_6	CC	Address setup to ALE	1.5 + t_A	–	TCL – 11 + t_A	–	ns
t_7	CC	Address hold after ALE	4 + t_A	–	TCL – 8.5 + t_A	–	ns
t_8	tCC	ALE falling edge to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	4 + t_A	–	TCL – 8.5 + t_A	–	ns
t_9	CC	ALE falling edge to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	– 8.5 + t_A	–	– 8.5 + t_A	–	ns
t_{10}	CC	Address float after $\overline{RD}$, $\overline{WR}$ (with RW-delay)	–	6	–	6	ns
t_{11}	CC	Address float after $\overline{RD}$, $\overline{WR}$ (no RW-delay)	–	18.5	–	TCL + 6	ns
t_{12}	CC	$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	15.5 + t_C	–	2TCL – 9.5 + t_C	–	ns
t_{13}	CC	$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	28 + t_C	–	3TCL – 9.5 + t_C	–	ns
t_{14}	SR	$\overline{RD}$ to valid data in (with RW-delay)	–	6 + t_C	–	2TCL – 19 + t_C	ns
t_{15}	SR	$\overline{RD}$ to valid data in (no RW-delay)	–	18.5 + t_C	–	3TCL – 19 + t_C	ns
t_{16}	SR	ALE low to valid data in	–	17.5 + t_A + t_C	–	3TCL – 20 + t_A + t_C	ns
t_{17}	SR	Address/unlatched $\overline{CS}$ to valid data in	–	20 + $2t_A$ + t_C	–	4TCL – 30 + $2t_A$ + t_C	ns
t_{18}	SR	Data hold after $\overline{RD}$ rising edge	0	–	0	–	ns
t_{19}	SR	Data float after $\overline{RD}$	–	16.5 + t_F	–	2TCL – 8.5 + t_F	ns
t_{22}	CC	Data valid to $\overline{WR}$	10 + t_C	–	2TCL – 15 + t_C	–	ns
t_{23}	CC	Data hold after $\overline{WR}$	4 + t_F	–	2TCL – 8.5 + t_F	–	ns
t_{25}	CC	ALE rising edge after $\overline{RD}$, $\overline{WR}$	15 + t_F	–	2TCL – 10 + t_F	–	ns
t_{27}	CC	Address/unlatched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	10 + t_F	–	2TCL – 15 + t_F	–	ns
t_{38}	CC	ALE falling edge to latched $\overline{CS}$	– 4 – t_A	10 – t_A	– 4 – t_A	10 – t_A	ns
t_{39}	SR	Latched $\overline{CS}$ low to valid data in	–	16.5 + t_C + $2t_A$	–	3TCL - 21 + t_C + $2t_A$	ns
t_{40}	CC	Latched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$	27 + t_F	–	3TCL - 10.5 + t_F	–	ns

24.8.17 Demultiplexed bus

V_{DD} = 5 V ± 10%, V_{SS} = 0 V, T_A = -40 to +125 °C, CL = 50 pF,
ALE cycle time = 4 TCL + 2 t_A + t_C + t_F (50 ns at 40 MHz CPU clock without wait states).

Table 71. Demultiplexed bus timings

Symbol		Parameter	f_{CPU} = 40 MHz TCL = 12.5 ns		Variable CPU clock 1/2 TCL = 1 to 40 MHz		Unit
			Min	Max	Min	Max	
t_5	CC	ALE high time	4 + t_A	–	TCL - 8.5 + t_A	–	ns
t_6	CC	Address setup to ALE	1.5 + t_A	–	TCL - 11 + t_A	–	ns
t_{80}	CC	Address/Unlatched $\overline{CS}$ setup to $\overline{RD}$, $\overline{WR}$ (with RW-delay)	12.5 + 2t_A	–	2TCL - 12.5 + 2t_A	–	ns
t_{81}	CC	Address/Unlatched $\overline{CS}$ setup to $\overline{RD}$, $\overline{WR}$ (no RW-delay)	0.5 + 2t_A	–	TCL - 12 + 2t_A	–	ns
t_{12}	CC	$\overline{RD}$, $\overline{WR}$ low time (with RW-delay)	15.5 + t_C	–	2TCL - 9.5 + t_C	–	ns
t_{13}	CC	$\overline{RD}$, $\overline{WR}$ low time (no RW-delay)	28 + t_C	–	3TCL - 9.5 + t_C	–	ns
t_{14}	SR	$\overline{RD}$ to valid data in (with RW-delay)	–	6 + t_C	–	2TCL - 19 + t_C	ns
t_{15}	SR	$\overline{RD}$ to valid data in (no RW-delay)	–	18.5 + t_C	–	3TCL - 19 + t_C	ns
t_{16}	SR	ALE low to valid data in	–	17.5 + t_A + t_C	–	3TCL - 20 + t_A + t_C	ns
t_{17}	SR	Address/Unlatched $\overline{CS}$ to valid data in	–	20 + 2t_A + t_C	–	4TCL - 30 + 2t_A + t_C	ns
t_{18}	SR	Data hold after $\overline{RD}$ rising edge	0	–	0	–	ns
t_{20}	SR	Data float after $\overline{RD}$ rising edge (with RW-delay)(1)	–	16.5 + t_F	–	2TCL - 8.5 + t_F + 2t_A	ns
t_{21}	SR	Data float after $\overline{RD}$ rising edge (no RW-delay)(1)	–	4 + t_F	–	TCL - 8.5 + t_F + 2t_A	ns
t_{22}	CC	Data valid to $\overline{WR}$	10 + t_C	–	2TCL - 15 + t_C	–	ns
t_{24}	CC	Data hold after $\overline{WR}$	4 + t_F	–	TCL - 8.5 + t_F	–	ns
t_{26}	CC	ALE rising edge after $\overline{RD}$, $\overline{WR}$	-10 + t_F	–	-10 + t_F	–	ns
t_{28}	CC	Address/unlatched $\overline{CS}$ hold after $\overline{RD}$, $\overline{WR}$(2)	0 + t_F	–	0 + t_F	–	ns
t_{28h}	CC	Address/unlatched $\overline{CS}$ hold after $\overline{WRH}$	-5 + t_F	–	-5 + t_F	–	ns
t_{38}	CC	ALE falling edge to latched $\overline{CS}$	-4 - t_A	6 - t_A	-4 - t_A	6 - t_A	ns
t_{39}	SR	Latched $\overline{CS}$ low to valid data in	–	16.5 + t_C + 2t_A	–	3TCL - 21 + t_C + 2t_A	ns

Figure 54. External memory cycle: Demultiplexed bus, with/without r/w delay, normal ALE

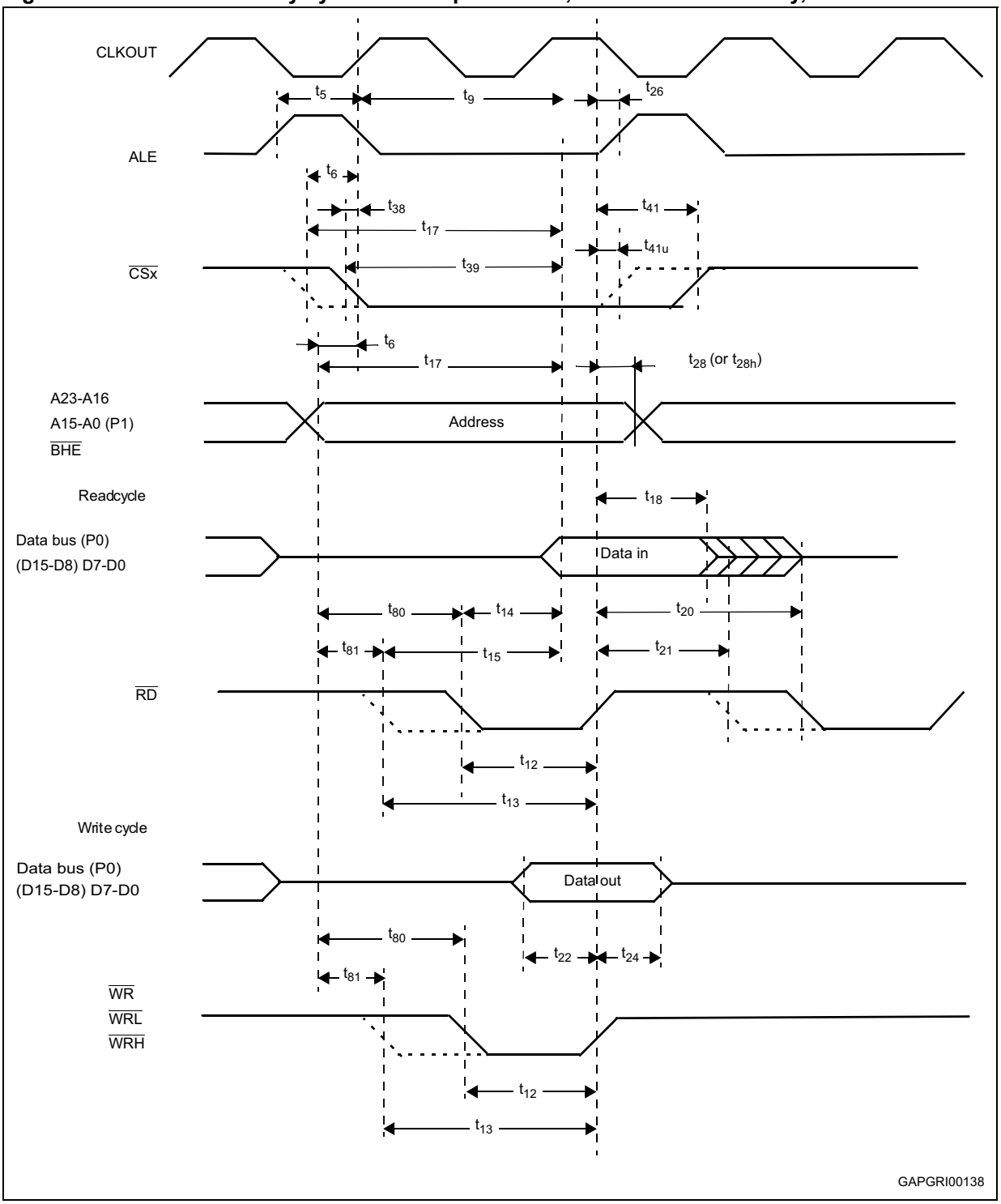


Figure 55. External memory cycle: Demultiplexed bus, with/without r/w delay, extended ALE

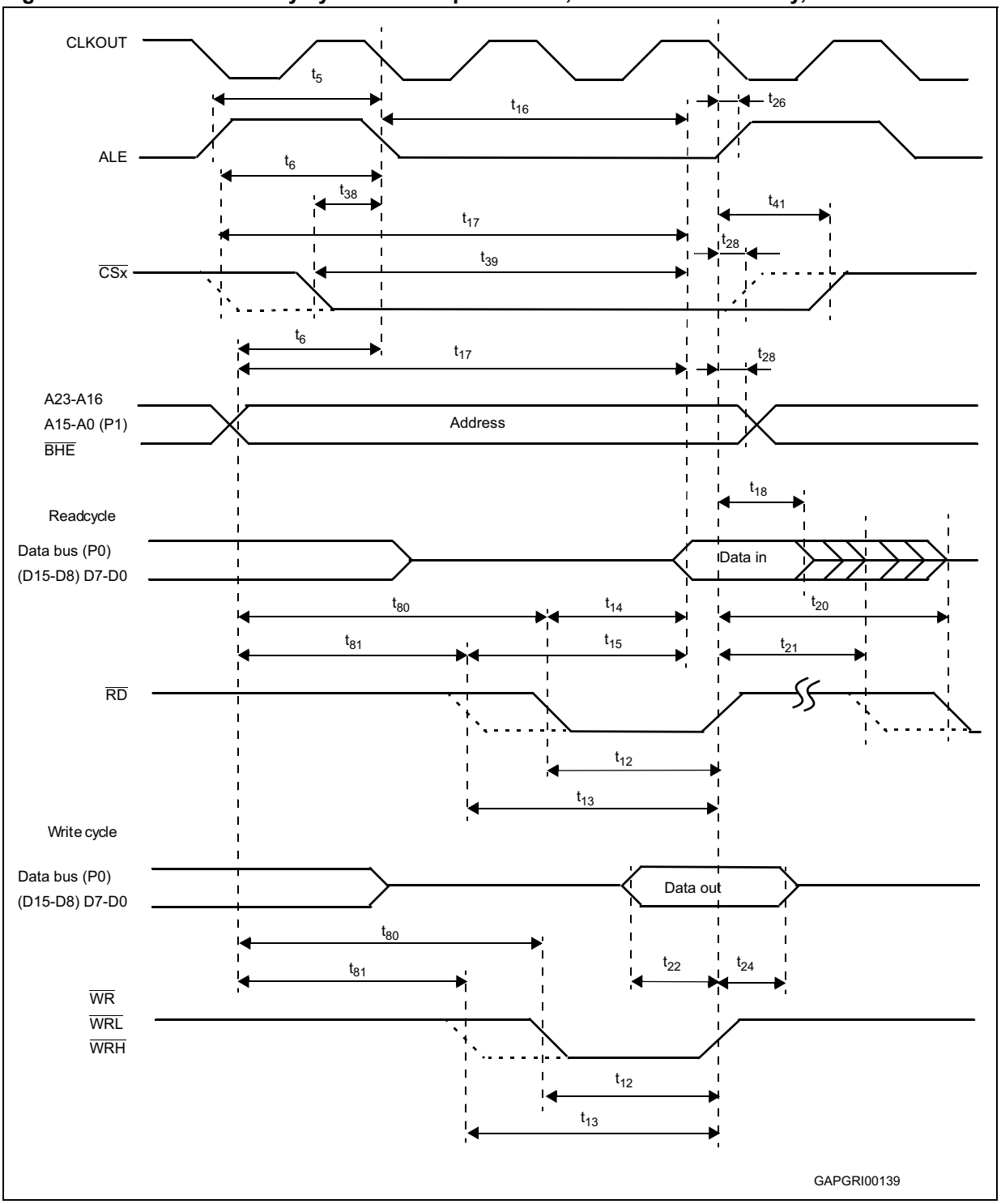
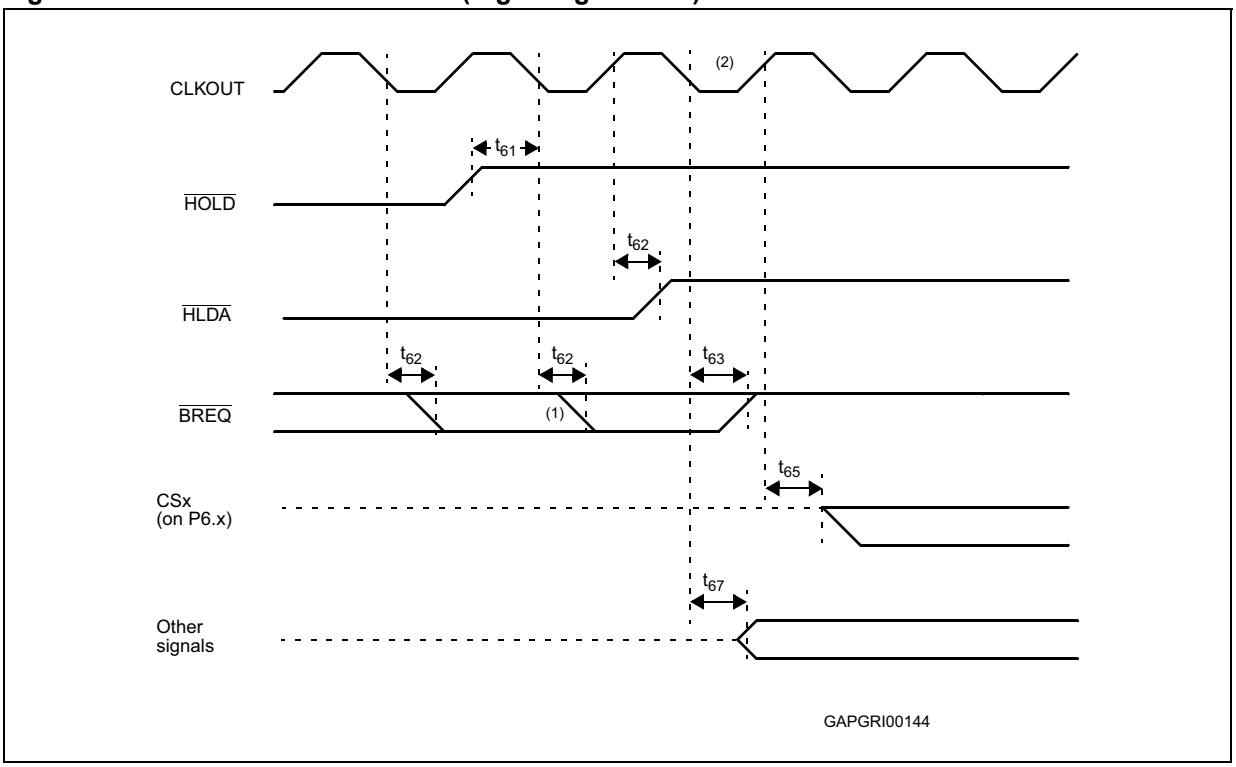


Figure 60. External bus arbitration (regaining the bus)



1. This is the last chance for $\overline{BREQ}$ to trigger the indicated regain-sequence. Even if $\overline{BREQ}$ is activated earlier, the regain-sequence is initiated by $\overline{HOLD}$ going high. Please note that $\overline{HOLD}$ may also be deactivated without the ST10F272M requesting the bus.
2. The next ST10F272M driven bus cycle may start here.

24.8.20 High-speed synchronous serial interface (SSC) timing

24.8.20.1 Master mode

V_{DD} = 5 V ±10 %, V_{SS} = 0 V, T_A = -40 to +125 °C, C_L = 50 pF

Table 74. SSC master mode timings

Symbol		Parameter	Maximum baudrate 6.6 Mbaud(1) @ f_{CPU} = 40 MHz (<SSCBR> = 0002h)		Variable baudrate (<SSCBR> = 0001h - FFFFh)		Unit
			Min	Max	Min	Max	
t_{300}	CC	SSC clock cycle time(2)	150	150	8TCL	262144 TCL	ns
t_{301}	CC	SSC clock high time	63	–	t_{300}/2 - 12	–	ns
t_{302}	CC	SSC clock low time	63	–	t_{300}/2 - 12	–	ns
t_{303}	CC	SSC clock rise time	–	10	–	10	ns
t_{304}	CC	SSC clock fall time	–	10	–	10	ns
t_{305}	CC	Write data valid after shift edge	–	15	–	15	ns
t_{306}	CC	Write data hold after shift edge(3)	-2	–	-2	–	ns