



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, HDMI-CEC, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 16x12b, 21x16b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f378cct6

Contents

1	Introduction	9
2	Description	10
3	Functional overview	13
3.1	ARM® Cortex®-M4 core with embedded Flash and SRAM	13
3.2	Memory protection unit	13
3.3	Embedded Flash memory	14
3.4	Cyclic redundancy check (CRC) calculation unit	14
3.5	Embedded SRAM	14
3.6	Boot modes	14
3.7	Power management	14
3.7.1	Power supply schemes	14
3.7.2	Power supply supervisor	15
3.7.3	Low-power modes	15
3.8	Clocks and startup	15
3.9	General-purpose input/outputs (GPIOs)	15
3.10	Direct memory access (DMA)	16
3.11	Interrupts and events	16
3.11.1	Nested vectored interrupt controller (NVIC)	16
3.11.2	Extended interrupt/event controller (EXTI)	16
3.12	12-bit analog-to-digital converter (ADC)	17
3.12.1	Temperature sensor	17
3.12.2	Internal voltage reference (V _{REFINT})	17
3.12.3	V _{BAT} battery voltage monitoring	17
3.13	16-bit sigma delta analog-to-digital converters (SDADC)	18
3.14	Digital-to-analog converter (DAC)	18
3.15	Fast comparators (COMP)	19
3.16	Touch sensing controller (TSC)	19
3.17	Timers and watchdogs	21
3.17.1	General-purpose timers (TIM2 to TIM5, TIM12 to TIM17, TIM19)	22
3.17.2	Basic timers (TIM6, TIM7, TIM18)	22

List of tables

Table 1.	Device summary	1
Table 2.	Device overview	11
Table 3.	Capacitive sensing GPIOs available on STM32F378xx devices	19
Table 4.	No. of capacitive sensing channels available on STM32F378xx devices.	20
Table 5.	Timer feature comparison.	21
Table 6.	Comparison of I ² C analog and digital filters	24
Table 7.	STM32F378xx I ² C implementation	24
Table 8.	STM32F378xx USART implementation	25
Table 9.	STM32F378xx SPI/I2S implementation	26
Table 10.	Legend/abbreviations used in the pinout table	33
Table 11.	STM32F378xx pin definitions	34
Table 12.	Alternate functions for port PA	41
Table 13.	Alternate functions for port PB	43
Table 14.	Alternate functions for port PC	44
Table 15.	Alternate functions for port PD	45
Table 16.	Alternate functions for port PE	46
Table 17.	Alternate functions for port PF	47
Table 18.	STM32F378xx peripheral register boundary addresses.	49
Table 19.	Voltage characteristics	55
Table 20.	Current characteristics	56
Table 21.	Thermal characteristics.	56
Table 22.	General operating conditions	57
Table 23.	Operating conditions at power-up / power-down	58
Table 24.	Embedded internal reference voltage calibration values	59
Table 25.	Embedded internal reference voltage.	59
Table 26.	Typical and maximum current consumption from V _{DD} supply at V _{DD} = 1.8V	60
Table 27.	Typical and maximum current consumption from V _{DDA} supply	62
Table 28.	Typical and maximum V _{DD} consumption in Stop mode	62
Table 29.	Typical and maximum V _{DDA} consumption in Stop mode	62
Table 30.	Typical and maximum current consumption from V _{BAT} supply.	63
Table 31.	Typical current consumption in Run mode, code with data processing running from Flash	64
Table 32.	Typical current consumption in Sleep mode, code running from Flash or RAM.	66
Table 33.	Switching output I/O current consumption	68
Table 34.	Peripheral current consumption	69
Table 35.	Low-power mode wakeup timings	71
Table 36.	High-speed external user clock characteristics.	71
Table 37.	Low-speed external user clock characteristics	72
Table 38.	HSE oscillator characteristics	73
Table 39.	LSE oscillator characteristics (f _{LSE} = 32.768 kHz)	75
Table 40.	HSI oscillator characteristics.	76
Table 41.	LSI oscillator characteristics	77
Table 42.	PLL characteristics	77
Table 43.	Flash memory characteristics	78
Table 44.	Flash memory endurance and data retention.	78
Table 45.	EMS characteristics	79
Table 46.	EMI characteristics	80
Table 47.	ESD absolute maximum ratings	80
Table 48.	Electrical sensitivities	81

Table 49.	I/O current injection susceptibility	82
Table 50.	I/O static characteristics	83
Table 51.	Output voltage characteristics	85
Table 52.	I/O AC characteristics	86
Table 53.	NRST pin characteristics	87
Table 54.	NPOR pin characteristics	88
Table 55.	I2C characteristics	89
Table 56.	I ² C analog filter characteristics	90
Table 57.	SPI characteristics	91
Table 58.	I ² S characteristics	94
Table 59.	ADC characteristics	96
Table 60.	R _{SRC} max for f _{ADC} = 14 MHz	97
Table 61.	ADC accuracy	97
Table 62.	DAC characteristics	99
Table 63.	Comparator characteristics	101
Table 64.	Temperature sensor calibration values	103
Table 65.	TS characteristics	103
Table 66.	V _{BAT} monitoring characteristics	103
Table 67.	TIMx characteristics	104
Table 68.	IWDG min/max timeout period at 40 kHz (LSI)	104
Table 69.	WWDG min-max timeout value @72 MHz (PCLK)	104
Table 70.	SDADC characteristics	105
Table 71.	VREFSD+ pin characteristics	110
Table 72.	UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data	111
Table 73.	UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)	112
Table 74.	WLCSP66 - 66-pin, 3.767 x 4.229 mm, 0.4 mm pitch wafer level chip scale package mechanical data	114
Table 75.	LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data	117
Table 76.	LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data	120
Table 77.	LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data	123
Table 78.	Package thermal characteristics	125
Table 79.	Ordering information scheme	128
Table 80.	Document revision history	129

List of figures

Figure 1.	Block diagram	12
Figure 2.	STM32F378xx LQFP48 pinout	28
Figure 3.	STM32F378xx LQFP64 pinout	29
Figure 4.	STM32F378xx LQFP100 pinout	30
Figure 5.	STM32F378xx UFBGA100 ballout	31
Figure 6.	STM32F378xx WLCSP66 ballout	32
Figure 7.	STM32F378xx memory map	48
Figure 8.	Pin loading conditions	52
Figure 9.	Pin input voltage	52
Figure 10.	Power supply scheme	53
Figure 11.	Current consumption measurement scheme	54
Figure 12.	Typical V_{BAT} current consumption (LSE and RTC ON/LSEDRV[1:0]='00')	63
Figure 13.	High-speed external clock source AC timing diagram	72
Figure 14.	Low-speed external clock source AC timing diagram	73
Figure 15.	Typical application with an 8 MHz crystal	74
Figure 16.	Typical application with a 32.768 kHz crystal	76
Figure 17.	HSI oscillator accuracy characterization results	77
Figure 18.	TC and TTA I/O input characteristics	84
Figure 19.	Five volt tolerant (FT and FTf) I/O input characteristics	84
Figure 20.	I/O AC characteristics definition	87
Figure 21.	Recommended NRST pin protection	88
Figure 22.	I ² C bus AC waveforms and measurement circuit	90
Figure 23.	SPI timing diagram - slave mode and CPHA = 0	92
Figure 24.	SPI timing diagram - slave mode and CPHA = 1 ⁽¹⁾	92
Figure 25.	SPI timing diagram - master mode ⁽¹⁾	93
Figure 26.	I ² S slave timing diagram (Philips protocol) ⁽¹⁾	95
Figure 27.	I ² S master timing diagram (Philips protocol) ⁽¹⁾	95
Figure 28.	ADC accuracy characteristics	98
Figure 29.	Typical connection diagram using the ADC	98
Figure 30.	12-bit buffered /non-buffered DAC	100
Figure 31.	Maximum V_{REFINT} scaler startup time from power down	102
Figure 32.	UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline	111
Figure 33.	UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint	112
Figure 34.	UFBGA100 marking example (package top view)	113
Figure 35.	WLCSP66 - 66-pin, 3.767 x 4.229 mm, 0.4 mm pitch wafer level chip scale package outline	114
Figure 36.	WLCSP66 marking example (package top view)	115
Figure 37.	LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline	116
Figure 38.	LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint	118
Figure 39.	LQFP100 marking example (package top view)	118
Figure 40.	LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline	119
Figure 41.	LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint	121
Figure 42.	LQFP64 marking example (package top view)	121
Figure 43.	LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline	122

3.3 Embedded Flash memory

All STM32F378xx devices feature up to 256 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

3.4 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

3.5 Embedded SRAM

All STM32F378xx devices feature up to 32 Kbytes of embedded SRAM with hardware parity check. The memory can be accessed in read/write at CPU clock speed with 0 wait states.

3.6 Boot modes

At startup, Boot0 pin and Boot1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

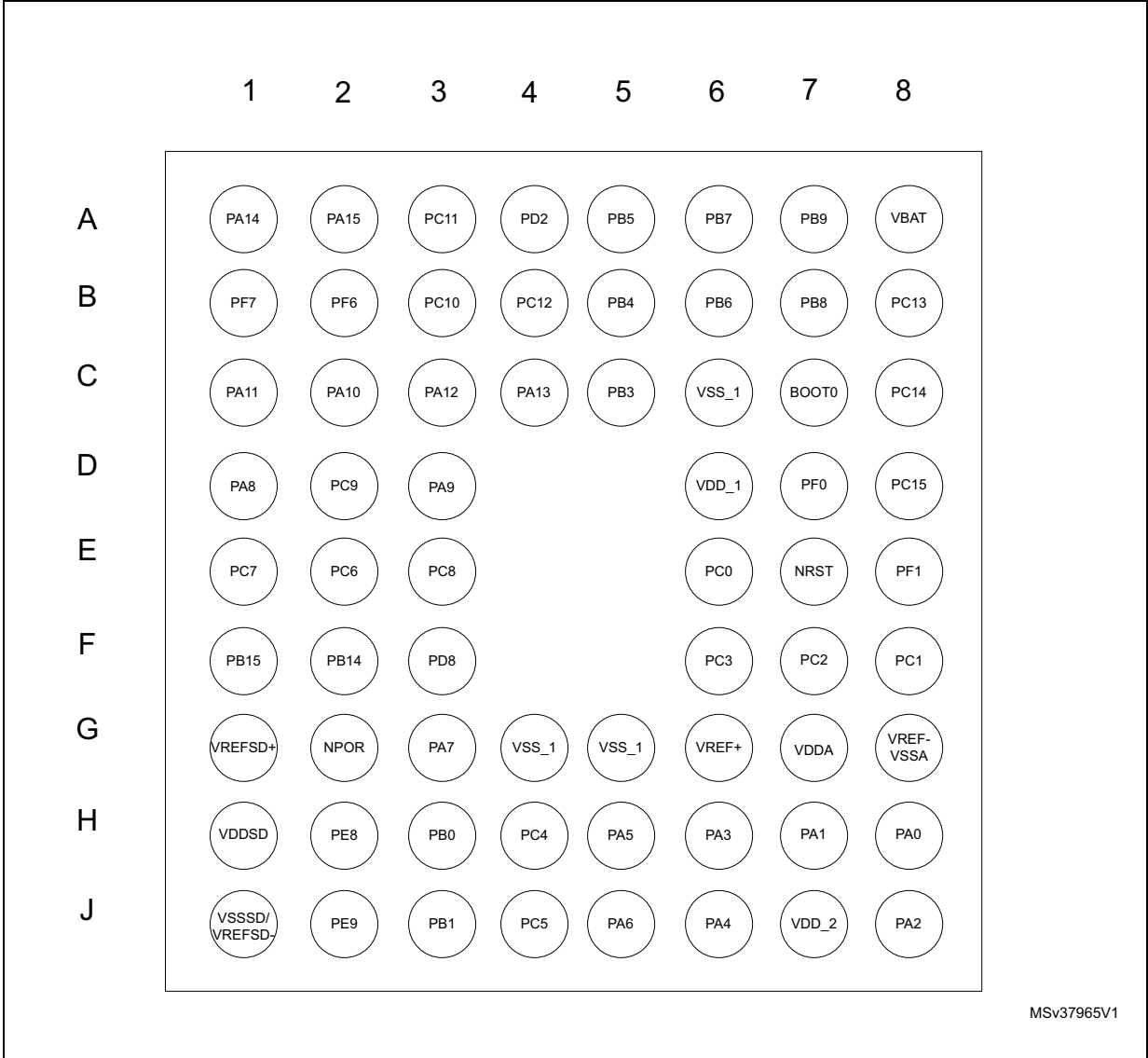
The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART2 (PD5/PD6) or I2C (PB6/PB7).

3.7 Power management

3.7.1 Power supply schemes

- V_{DD} : external power supply for I/Os and core. It is provided externally through V_{DD} pins, and can be 1.8 V +/- 8%.
- V_{DDA} = 1.65 to 3.6 V:
 - external analog power supplies for Reset blocks, RCs and PLL
 - supply voltage for 12-bit ADC, DACs and comparators (minimum voltage to be applied to V_{DDA} is 2.4 V when the 12-bit ADC and DAC are used).
- V_{DDSD12} and V_{DDSD3} = 2.2 to 3.6 V: supply voltages for SDADC1/2 and SDADCD3 sigma delta ADCs. Independent from V_{DD}/V_{DDA} .
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers when V_{DD} is not present.

Figure 6. STM32F378xx WLCSP66 ballout



1. The above figure shows the package top view.

Table 11. STM32F378xx pin definitions (continued)

Pin numbers					Pin name (function after reset)	Pin type	Notes	I/O structure	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48	WLCSP66					Alternate function	Additional functions
93	B4	59	43	A6	PB7	I/O	-	FTf	I2C1_SDA, USART1_RX, TIM17_CH1N, TIM3_CH4, TIM4_CH2, TIM19_CH2, TIM15_CH2, TSC_G5_IO4	-
94	A4	60	44	C7	BOOT0	I	-	B	Boot memory selection	
95	A3	61	45	B7	PB8	I/O	-	FTf	SPI2_SCK/I2S2_CK, I2C1_SCL, USART3_TX, CAN_RX, CEC, TIM16_CH1, TIM4_CH3, TIM19_CH3, COMP1_OUT, TSC_SYNC	-
96	B3	62	46	A7	PB9	I/O	-	FTf	SPI2_NSS/I2S2_WS, I2C1_SDA, USART3_RX, CAN_TX, IR_OUT, TIM17_CH1, TIM4_CH4, TIM19_CH4, COMP2_OUT	-
97	C3	-	-	-	PE0	I/O	(1)	FT	USART1_TX, TIM4_ETR	-
98	A2	-	-	-	PE1	I/O	(1)	FT	USART1_RX	-
99	D3	63	47	C6	VSS_1	S	-	-	Ground	
-	-	-	-	G5	VSS_1	S	(1)	-	Ground	
-	-	-	-	G4	VSS_1	S	(1)	-	Ground	
100	C4	64	48	D6	VDD_1	S	-	-	Digital power supply	

- When using the small packages (48 and 64 pin packages), the GPIO pins which are not present on these packages, must not be configured in analog mode.
- PC13, PC14 and PC15 are supplied through the power switch. Since the switch sinks only a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is limited:
 - The speed should not exceed 2 MHz with a maximum load of 30 pF
 - These GPIOs must not be used as current sources (e.g. to drive an LED)
 After the first backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the Backup registers which is not reset by the main reset. For details on how to manage these GPIOs, refer to the Battery backup domain and BKP register description sections in the RM0313 reference manual.
- These pins are powered by V_{DDA} .
- These pins are powered by VDDSD12.
- These pins are powered by VDDSD3.



Table 12. Alternate functions for port PA (continued)

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF14	AF15
PA13	SWDIO -JTMS	TIM16_ CH1N	TIM5_ CH4	TSC_ G4_IO3	-	IR-OUT	SPI1_MISO /I2S1_MCK	USART3_CTS	-	-	TIM4_ CH3	-	-	EVENT OUT
PA14	SWCLK -JTCK	-	-	TSC_ G4_IO4	I2C1_ SDA	-	-	-	-	-	TIM12_ CH1	-	-	EVENT OUT
PA15	JTDI	TIM2_ CH1_ETR	-	TSC_ SYNC	I2C1_ SCL	SPI1_NSS/ I2S1_WS	SPI3_NSS/ I2S3_WS	-	-	-	TIM12_ CH2	-	-	EVENT OUT



Table 15. Alternate functions for port PD

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	-	EVENTOUT	TIM19_CH4	-	-	-	-	CAN_RX
PD1	-	EVENTOUT	TIM19_ETR	-	-	-	-	CAN_TX
PD2	-	EVENTOUT	TIM3_ETR	-	-	-	-	-
PD3	-	EVENTOUT	-	-	-	SPI2_MISO/I2S2_MCK	-	USART2_CTS
PD4	-	EVENTOUT	-	-	-	SPI2_MOSI/I2S2_SD	-	USART2_RTS
PD5	-	EVENTOUT	-	-	-	-	-	USART2_TX
PD6	-	EVENTOUT	-	-	-	SPI2_NSS/I2S2_WS	-	USART2_RX
PD7	-	EVENTOUT	-	-	-	SPI2_SCK/I2S2_CK	-	USART2_CK
PD8	-	EVENTOUT	-	TSC_G6_IO3	-	SPI2_SCK/I2S2_CK	-	USART3_TX
PD9	-	EVENTOUT	-	TSC_G6_IO4	-	-	-	USART3_RX
PD10	-	EVENTOUT	-	-	-	-	-	USART3_CK
PD11	-	EVENTOUT	-	-	-	-	-	USART3_CTS
PD12	-	EVENTOUT	TIM4_CH1	TSC_G8_IO1	-	-	-	USART3_RTS
PD13	-	EVENTOUT	TIM4_CH2	TSC_G8_IO2	-	-	-	-
PD14	-	EVENTOUT	TIM4_CH3	TSC_G8_IO3	-	-	-	-
PD15	-	EVENTOUT	TIM4_CH4	TSC_G8_IO4	-	-	-	-

Table 26. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 1.8V⁽¹⁾ (continued)

Symbol	Parameter	Conditions	f _{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T _A ⁽²⁾			Typ	Max @ T _A ⁽²⁾			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I _{DD}	Supply current in Run mode, code executing from RAM	HSE bypass, PLL on	72 MHz	65.5	77.8	78.1	86.6	31.6	35.1	35.6	38.0	mA
			64 MHz	58.7	69.0	69.5	76.5	28.2	31.2	31.7	33.7	
			48 MHz	44.8	51.6	52.2	56.6	21.4	23.3	23.9	25.1	
			32 MHz	30.4	34.2	34.9	37.1	14.4	15.6	16.1	16.8	
			24 MHz	23.1	25.7	26.2	27.6	10.9	11.8	12.2	12.8	
		HSE bypass, PLL off	8 MHz	7.7	8.4	8.9	9.5	3.6	4.0	4.4	5.0	
			1 MHz	1.0	1.3	1.7	2.2	0.5	0.7	1.1	1.7	
		HSI clock, PLL on	64 MHz	54.3	63.3	63.9	70.1	27.9	30.8	31.2	33.2	
			48 MHz	41.5	47.3	48.0	51.9	21.1	23.0	23.5	24.7	
			32 MHz	28.2	31.5	32.2	34.1	14.2	15.3	15.9	16.5	
			24 MHz	21.4	23.6	24.3	25.5	7.2	7.8	8.2	8.8	
		HSI clock, PLL off	8 MHz	7.3	7.9	8.4	9.1	3.6	4.0	4.4	4.9	
	Supply current in Sleep mode, code executing from Flash or RAM	HSE bypass, PLL on	72 MHz	46.4	54.0	54.8	59.5	7.2	7.9	8.4	9.0	
			64 MHz	41.5	48.0	48.8	52.6	6.5	7.1	7.5	8.1	
			48 MHz	31.6	35.9	36.7	39.0	4.9	5.3	5.8	6.4	
			32 MHz	21.4	23.8	24.7	25.7	3.3	3.7	4.2	4.7	
			24 MHz	16.2	17.9	18.6	19.4	2.5	2.8	3.3	3.8	
		HSE bypass, PLL off	8 MHz	5.4	5.9	6.5	7.0	0.8	1.1	1.6	2.1	
			1 MHz	0.7	1.0	1.4	1.9	0.1	0.3	0.7	1.3	
		HSI clock, PLL on	64 MHz	37.0	42.4	43.3	46.4	6.1	6.7	7.2	7.7	
			48 MHz	28.2	31.8	32.7	34.5	4.6	5.0	5.5	6.1	
			32 MHz	19.1	21.2	22.0	22.9	3.1	3.5	4.0	4.5	
			24 MHz	14.5	16.0	16.7	17.4	1.7	2.0	2.4	2.9	
		HSI clock, PLL off	8 MHz	5.0	5.5	6.0	6.6	0.8	1.1	1.5	2.0	

1. To calculate complete device consumption there must be added consumption from VDDA (Table 27).

2. Guaranteed by characterization results.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in [Table 50: I/O static characteristics](#).

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC and SDADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode. Under reset conditions all I/Os are configured in input floating mode - so if some inputs do not have a defined voltage level then they can generate additional consumption. This consumption is visible on V_{DD} supply and also on V_{DDSDx} supply because some I/Os are powered from SDADCx supply (all I/Os which have SDADC analog input functionality).

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see [Table 34: Peripheral current consumption](#)), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 35. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ @V _{DD} = 1.8 V, V _{DPA} = 3.3 V	Max	Unit
t _{WUSTOP}	Wakeup from Stop mode	-	3.6	5.21	μs
t _{WUSLEEP}	Wakeup from Sleep mode	After WFE instruction	6		CPU clock cycles
t _{WUPOR}	Wakeup from Power off state	Startup after NPOR pin release	62.6	100	μs

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

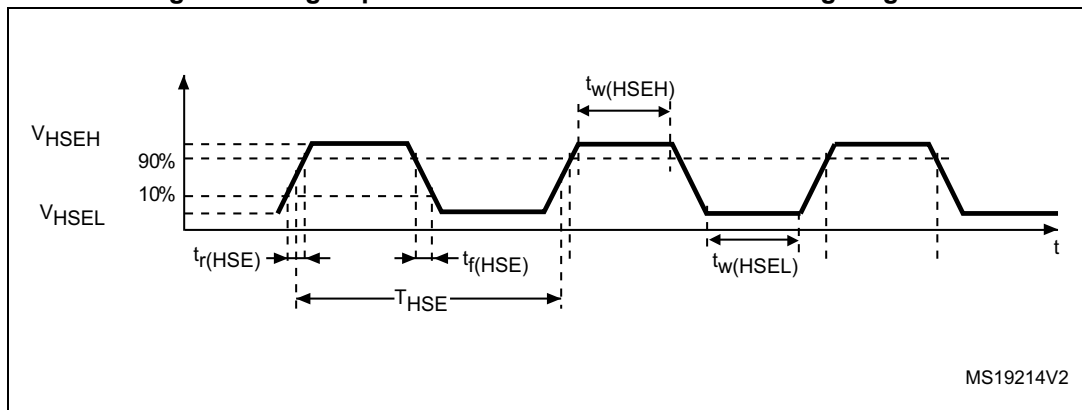
The external clock signal has to respect the I/O characteristics in [Section 6.3.13](#). However, the recommended clock input waveform is shown in [Figure 13](#).

Table 36. High-speed external user clock characteristics

Symbol	Parameter ⁽¹⁾	Conditions	Min	Typ	Max	Unit
f _{HSE_ext}	User external clock source frequency	CSS is on or PLL is used	1	8	32	MHz
		CSS is off, PLL not used	0			
V _{HSEH}	OSC_IN input pin high level voltage	-	0.7 V _{DD}	-	V _{DD}	V
V _{HSEL}	OSC_IN input pin low level voltage	-	V _{SS}	-	0.3 V _{DD}	
t _{w(HSEH)} t _{w(HSEL)}	OSC_IN high or low time	-	15	-	-	ns
t _{r(HSE)} t _{f(HSE)}	OSC_IN rise or fall time	-	-	-	20	

1. Guaranteed by design.

Figure 13. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in [Section 6.3.13](#). However, the recommended clock input waveform is shown in [Figure 14](#).

Table 37. Low-speed external user clock characteristics

Symbol	Parameter ⁽¹⁾	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time	-	-	-	50	

1. Guaranteed by design.

6.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in [Table 50](#) are derived from tests performed under the conditions summarized in [Table 22](#). All I/Os are CMOS and TTL compliant.

Table 50. I/O static characteristics ⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	$0.3V_{DD}+0.07^{(2)}$	V
		FT and FTf I/O	-	-	$0.475V_{DD}-0.2^{(2)}$	
		BOOT0	-	-	$0.3V_{DD}-0.3^{(2)}$	
		All I/Os except BOOT0 pin	-	-	$0.3V_{DD}$	
V_{IH}	High level input voltage	TC and TTa I/O	$0.445V_{DD}+0.398^{(2)}$	-	-	V
		FT and FTf I/O	$0.5V_{DD}+0.2^{(2)}$	-	-	
		BOOT0	$0.2V_{DD}+0.95^{(2)}$	-	-	
		All I/Os except BOOT0 pin	$0.7V_{DD}$	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	$200^{(2)}$	-	mV
		FT and FTf I/O	-	$100^{(2)}$	-	
		BOOT0	-	$300^{(2)}$	-	
I_{Ikg}	Input leakage current ⁽³⁾	TC, FT, FTf and POR I/O TTa in digital mode $V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	± 0.1	μA
		TTa in digital mode $V_{DD} \leq V_{IN} \leq V_{DDA}$	-	-	1	
		TTa in analog mode $V_{SS} \leq V_{IN} \leq V_{DDA}$	-	-	± 0.2	
		FT and FTf I/O ⁽³⁾ $V_{DD} \leq V_{IN} \leq 5 V$	-	-	10	
		POR $V_{DDA} \leq V_{IN} \leq 5 V$	-	-	10	
R_{PU}	Weak pull-up equivalent resistor ⁽⁴⁾	$V_{IN} = V_{SS}$	25	40	55	k Ω
R_{PD}	Weak pull-down equivalent resistor ⁽⁴⁾	$V_{IN} = V_{DD}$	25	40	55	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

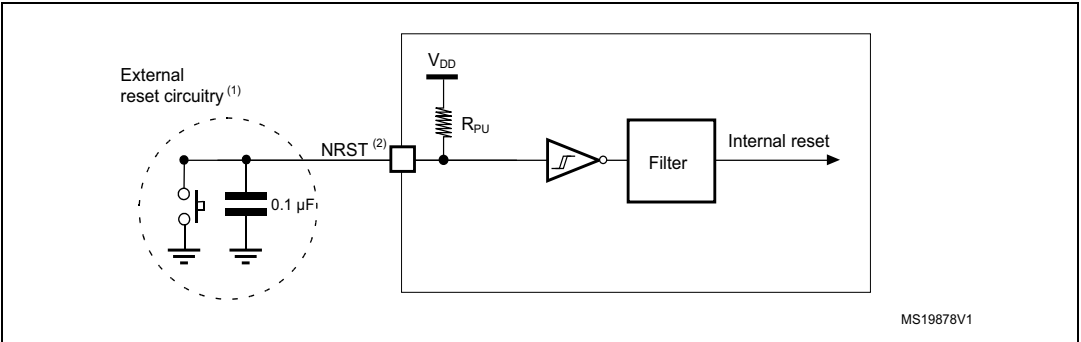
1. VDDSD12 is the external power supply for the PB10, and PE7 to PE15 I/O pins (the I/O pin ground is internally connected to VSS). VDDSD3 is the external power supply for PB14 to PB15 and PD8 to PD15 I/O pins (the I/O pin ground is internally connected to VSS). For those pins all V_{DD} supply references in this table are related to their given VDDSDx power supply.

2. Guaranteed by design.

3. Leakage could be higher than maximum value, if negative current is injected on adjacent pins.

4. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

Figure 21. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in [Table 53](#). Otherwise the reset will not be taken into account by the device.

NPOR pin characteristics

The NPOR pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor to the V_{DDA} , R_{PU} (see [Table 50](#)).

Unless otherwise specified, the parameters given in [Table 54](#) are derived from tests performed under ambient temperature and V_{DDA} supply voltage conditions summarized in [Table 22](#).

Table 54. NPOR pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NPOR)}^{(1)}$	NPOR Input low level voltage	-	-	-	$0.475V_{DDA} - 0.2$	V
$V_{IH(NPOR)}^{(1)}$	NPOR Input high level voltage	-	$0.5V_{DDA} + 0.2$	-	-	
$V_{hys(NPOR)}^{(1)}$	NPOR Schmitt trigger voltage hysteresis	-	-	100	-	mV
R_{PU}	Weak pull-up equivalent resistor ⁽²⁾	$V_{IN} = V_{SS}$	25	40	55	kΩ

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

6.3.16 12-bit ADC characteristics

Unless otherwise specified, the parameters given in [Table 59](#) are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in [Table 22](#).

Note: *It is recommended to perform a calibration after each power-up.*

Table 59. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	0	-	-	V
$I_{DDA(ADC)}^{(1)}$	Current consumption from V_{DDA}	$V_{DDA} = 3.3$ V	-	0.9	-	mA
I_{VREF}	Current on the V_{REF} input pin	-	-	160 ⁽²⁾	220 ⁽²⁾	μA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
$f_S^{(3)}$	Sampling rate	-	0.05	-	1	MHz
$f_{TRIG}^{(3)}$	External trigger frequency	$f_{ADC} = 14$ MHz	-	-	823	kHz
		-	-	-	17	1/ f_{ADC}
V_{AIN}	Conversion voltage range	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
$R_{SRC}^{(3)}$	Signal source impedance	See Equation 1 and Table 60 for details	-	-	50	kΩ
$R_{ADC}^{(3)}$	Sampling switch resistance	-	-	-	1	kΩ
$C_{ADC}^{(3)}$	Internal sample and hold capacitor	-	-	-	8	pF
$t_{CAL}^{(3)}$	Calibration time	$f_{ADC} = 14$ MHz	5.9			μs
		-	83			1/ f_{ADC}
$t_{lat}^{(3)}$	Injection trigger conversion latency	$f_{ADC} = 14$ MHz	-	-	0.214	μs
		-	-	-	2 ⁽⁴⁾	1/ f_{ADC}
$t_{latr}^{(3)}$	Regular trigger conversion latency	$f_{ADC} = 14$ MHz	-	-	0.143	μs
		-	-	-	2 ⁽⁴⁾	1/ f_{ADC}
$t_S^{(3)}$	Sampling time	$f_{ADC} = 14$ MHz	0.107	-	17.1	μs
		-	1.5	-	239.5	1/ f_{ADC}
$t_{STAB}^{(3)}$	Power-up time	-	-	-	1	μs
$t_{CONV}^{(3)}$	Total conversion time (including sampling time)	$f_{ADC} = 14$ MHz	1	-	18	μs
		-	14 to 252 (t_S for sampling +12.5 for successive approximation)			1/ f_{ADC}

1. During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 μA on I_{DDA} and 60 μA on I_{DD} is present
2. Guaranteed by characterization results.
3. Guaranteed by design.
4. For external triggers, a delay of 1/ f_{PCLK2} must be added to the latency specified in [Table 59](#)

6.3.18 Comparator characteristics

Table 63. Comparator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max ⁽¹⁾	Unit
V_{DDA}	Analog supply voltage	V_{REFINT} scaler not in use	1.65	-	3.6	V
		V_{REFINT} scaler in use	2			
V_{IN}	Comparator input voltage range	-	0	-	V_{DDA}	V
V_{BG}	V_{REFINT} scaler input voltage	-	-	1.2	-	V
V_{SC}	V_{REFINT} scaler offset voltage	-	-	± 5	± 10	mV
t_{S_SC}	Scaler startup time from power down	First V_{REFINT} scaler activation after device power on	-	-	1000 ⁽²⁾	ms
		Next activations			0.2	
t_{START}	Comparator startup time	Startup time to reach propagation delay specification	-	-	60	μs
t_D	Propagation delay for 200 mV step with 100 mV overdrive	Ultra-low power mode	-	2	4.5	μs
		Low power mode	-	0.7	1.5	
		Medium power mode	-	0.3	0.6	
		High speed mode	$V_{DDA} \geq 2.7$ V		100	ns
			$V_{DDA} < 2.7$ V		240	
	Propagation delay for full range step with 100 mV overdrive	Ultra-low power mode	-	2	7	μs
		Low power mode	-	0.7	2.1	
		Medium power mode	-	0.3	1.2	
		High speed mode	$V_{DDA} \geq 2.7$ V		180	ns
			$V_{DDA} < 2.7$ V		300	
V_{offset}	Comparator offset error	-	-	± 4	± 10	mV
dV_{offset}/dT	Offset error temperature coefficient	-	-	18	-	$\mu V/^{\circ}C$
$I_{DD(COMP)}$	COMP current consumption	Ultra-low power mode	-	1.2	1.5	μA
		Low power mode	-	3	5	
		Medium power mode	-	10	15	
		High speed mode	-	75	100	

Technical drawing of a rectangular plate with dimensions and hole locations. The plate has a total width of 9.70 and a total height of 9.70. The drawing shows a grid of holes with the following dimensions and labels:

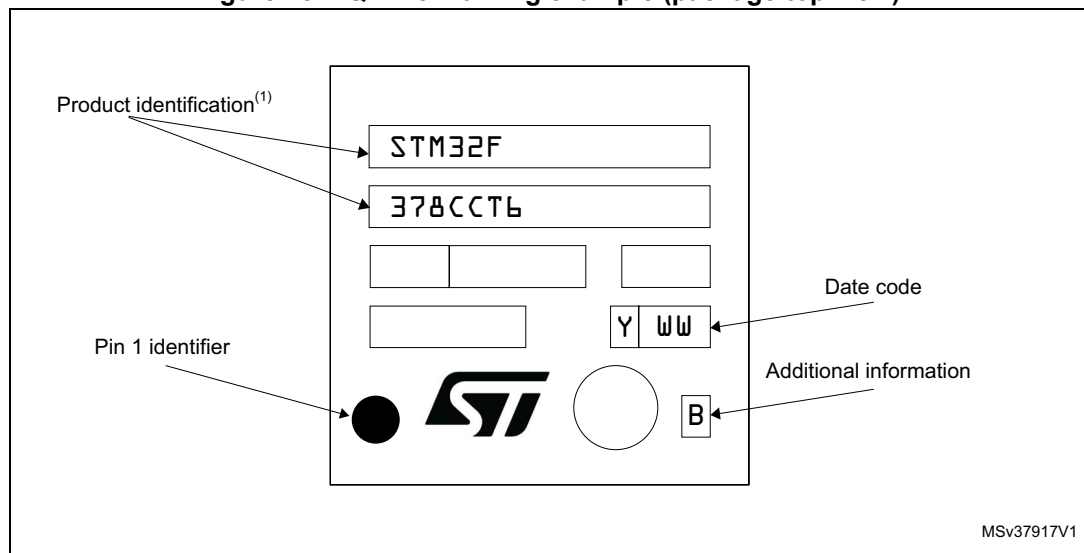
- Top Row:** 12 holes, labeled 1 to 12. The distance from the left edge to the center of the first hole is 5.80. The distance between the centers of the first and last hole is 5.80. The distance from the center of the last hole to the right edge is 1.20. The distance from the center of the first hole to the top edge is 7.30. The distance from the center of the last hole to the top edge is 7.30. The distance from the center of the first hole to the center of the last hole is 5.80. The distance from the center of the first hole to the center of the last hole is 5.80. The distance from the center of the first hole to the center of the last hole is 5.80.
- Bottom Row:** 12 holes, labeled 13 to 24. The distance from the left edge to the center of the first hole is 5.80. The distance between the centers of the first and last hole is 5.80. The distance from the center of the last hole to the right edge is 1.20. The distance from the center of the first hole to the bottom edge is 7.30. The distance from the center of the last hole to the bottom edge is 7.30. The distance from the center of the first hole to the center of the last hole is 5.80. The distance from the center of the first hole to the center of the last hole is 5.80. The distance from the center of the first hole to the center of the last hole is 5.80.
- Left Column:** 12 holes, labeled 25 to 36. The distance from the left edge to the center of the first hole is 5.80. The distance between the centers of the first and last hole is 5.80. The distance from the center of the last hole to the left edge is 1.20. The distance from the center of the first hole to the top edge is 7.30. The distance from the center of the last hole to the top edge is 7.30. The distance from the center of the first hole to the center of the last hole is 5.80. The distance from the center of the first hole to the center of the last hole is 5.80. The distance from the center of the first hole to the center of the last hole is 5.80.
- Right Column:** 12 holes, labeled 37 to 48. The distance from the left edge to the center of the first hole is 5.80. The distance between the centers of the first and last hole is 5.80. The distance from the center of the last hole to the right edge is 1.20. The distance from the center of the first hole to the bottom edge is 7.30. The distance from the center of the last hole to the bottom edge is 7.30. The distance from the center of the first hole to the center of the last hole is 5.80. The distance from the center of the first hole to the center of the last hole is 5.80. The distance from the center of the first hole to the center of the last hole is 5.80.

Additional dimensions and labels include:

- 0.50: Distance from the center of the first hole in the top row to the center of the first hole in the bottom row.
- 0.20: Distance from the center of the first hole in the top row to the center of the first hole in the bottom row.
- 0.30: Distance from the center of the first hole in the top row to the center of the first hole in the bottom row.

Device marking for LQFP48

Figure 45. LQFP48 marking example (package top view)



- 

9 Revision history

Table 80. Document revision history

Date	Revision	Changes
04-Mar-2014	1	Initial release.
09-Apr-2014	2	Removed sub-set part number (64KB and 128KB). Updated Part numbering on page 128
21-Jul-2015	3	Updated Section 7 Updated Section 3.13 Updated Section 3.7.1, Section 3.7.3 Updated Table 2: Device overview, Table 11: STM32F378xx pin definitions, Table 22: General operating conditions, Table 47: ESD absolute maximum ratings, Table 70: SDADC characteristics, Table 74: WLCSP66 - 66-pin, 3.767 x 4.229 mm, 0.4 mm pitch wafer level chip scale package mechanical data and Table 75: LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data, Table 78: Package thermal characteristics and Table 79: Ordering information scheme Updated Figure 5: STM32F378xx UFBGA100 ballout, Figure 10: Power supply scheme, Figure 35: WLCSP66 - 66-pin, 3.767 x 4.229 mm, 0.4 mm pitch wafer level chip scale package outline, Figure 36: WLCSP66 marking example (package top view), Figure 38: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint, Figure 39: LQFP100 marking example (package top view), Figure 40: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline, Figure 41: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint, Figure 42: LQFP64 marking example (package top view), Figure 44: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint, Figure 45: LQFP48 marking example (package top view). Added Table 30: Typical and maximum current consumption from VBAT supply, Table 63: Comparator characteristics, Table 73: UFBGA100 recommended PCB design rules (0.5 mm pitch BGA) Added Figure 12: Typical VBAT current consumption (LSE and RTC ON/LSEDRV[1:0]='00'), Figure 31: Maximum VREFINT scaler startup time from power down and Figure 33: UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2016 STMicroelectronics – All rights reserved