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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	35
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 16x12b, 21x16b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f378cct6

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3.3 Embedded Flash memory

All STM32F378xx devices feature up to 256 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

3.4 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

3.5 Embedded SRAM

All STM32F378xx devices feature up to 32 Kbytes of embedded SRAM with hardware parity check. The memory can be accessed in read/write at CPU clock speed with 0 wait states.

3.6 Boot modes

At startup, Boot0 pin and Boot1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

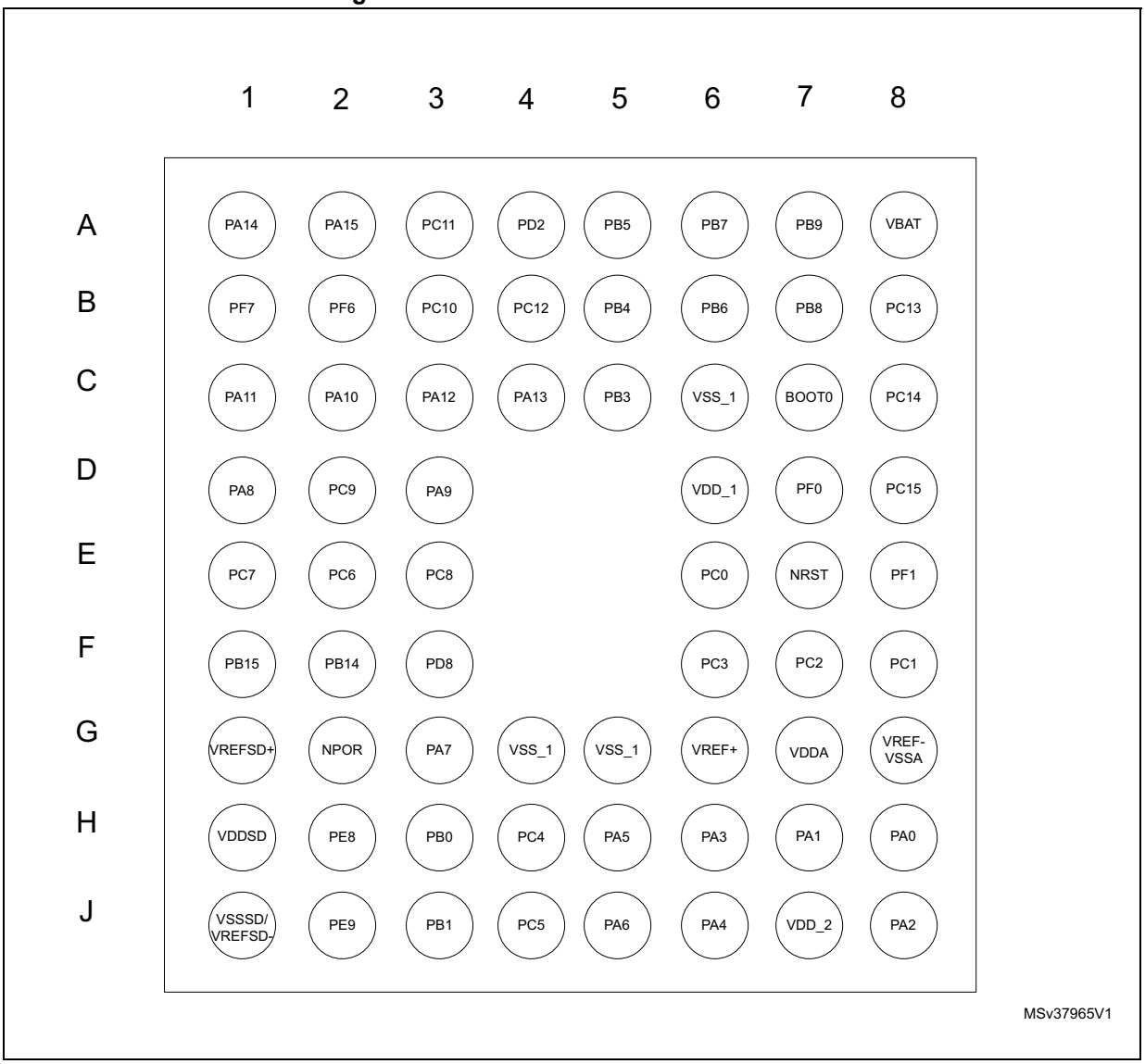
The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART2 (PD5/PD6) or I2C (PB6/PB7).

3.7 Power management

3.7.1 Power supply schemes

- V_{DD}: external power supply for I/Os and core. It is provided externally through V_{DD} pins, and can be 1.8 V +/- 8%.
- V_{DDA} = 1.65 to 3.6 V:
  - external analog power supplies for Reset blocks, RCs and PLL
  - supply voltage for 12-bit ADC, DACs and comparators (minimum voltage to be applied to V_{DDA} is 2.4 V when the 12-bit ADC and DAC are used).
- V_{DDSD12} and V_{DDSD3} = 2.2 to 3.6 V: supply voltages for SDADC1/2 and SDADCD3 sigma delta ADCs. Independent from V_{DD}/V_{DDA}.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers when V_{DD} is not present.

Figure 6. STM32F378xx WLCSP66 ballout



1. The above figure shows the package top view.

Table 11. STM32F378xx pin definitions (continued)

Pin numbers					Pin name (function after reset)	Pin type	Notes	I/O structure	Pin functions	
LQFP100	BGA100	LQFP64	LQFP48	WLCSP66					Alternate function	Additional functions
93	B4	59	43	A6	PB7	I/O	-	FTf	I2C1_SDA, USART1_RX, TIM17_CH1N, TIM3_CH4, TIM4_CH2, TIM19_CH2, TIM15_CH2, TSC_G5_IO4	-
94	A4	60	44	C7	BOOT0	I	-	B	Boot memory selection	
95	A3	61	45	B7	PB8	I/O	-	FTf	SPI2_SCK/I2S2_CK, I2C1_SCL, USART3_TX, CAN_RX, CEC, TIM16_CH1, TIM4_CH3, TIM19_CH3, COMP1_OUT, TSC_SYNC	-
96	B3	62	46	A7	PB9	I/O	-	FTf	SPI2_NSS/I2S2_WS, I2C1_SDA, USART3_RX, CAN_TX, IR_OUT, TIM17_CH1, TIM4_CH4, TIM19_CH4, COMP2_OUT	-
97	C3	-	-	-	PE0	I/O	(1)	FT	USART1_TX, TIM4_ETR	-
98	A2	-	-	-	PE1	I/O	(1)	FT	USART1_RX	-
99	D3	63	47	C6	VSS_1	S	-	-	Ground	
-	-	-	-	G5	VSS_1	S	(1)	-	Ground	
-	-	-	-	G4	VSS_1	S	(1)	-	Ground	
100	C4	64	48	D6	VDD_1	S	-	-	Digital power supply	

1. When using the small packages (48 and 64 pin packages), the GPIO pins which are not present on these packages, must not be configured in analog mode.
2. PC13, PC14 and PC15 are supplied through the power switch. Since the switch sinks only a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (e.g. to drive an LED)
   After the first backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the Backup registers which is not reset by the main reset. For details on how to manage these GPIOs, refer to the Battery backup domain and BKP register description sections in the RM0313 reference manual.
3. These pins are powered by V_{DDA}.
4. These pins are powered by VDDSD12.
5. These pins are powered by VDDSD3.

Table 12. Alternate functions for port PA (continued)

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF14	AF15
PA13	SWDIO -JTMS	TIM16_ CH1N	TIM5_ CH4	TSC_ G4_IO3	-	IR-OUT	SPI1_MISO /I2S1_MCK	USART3_CTS	-	-	TIM4_ CH3	-	-	EVENT OUT
PA14	SWCLK -JTCK	-	-	TSC_ G4_IO4	I2C1_ SDA	-	-	-	-	-	TIM12 _CH1	-	-	EVENT OUT
PA15	JTDI	TIM2_ CH1_ETR	-	TSC_ SYNC	I2C1_ SCL	SPI1_NSS/ I2S1_WS	SPI3_NSS/ I2S3_WS	-	-	-	TIM12 _CH2	-	-	EVENT OUT

Table 15. Alternate functions for port PD

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	-	EVENTOUT	TIM19_CH4	-	-	-	-	CAN_RX
PD1	-	EVENTOUT	TIM19_ETR	-	-	-	-	CAN_TX
PD2	-	EVENTOUT	TIM3_ETR	-	-	-	-	-
PD3	-	EVENTOUT	-	-	-	SPI2_MISO/I2S2_MCK	-	USART2_CTS
PD4	-	EVENTOUT	-	-	-	SPI2_MOSI/I2S2_SD	-	USART2_RTS
PD5	-	EVENTOUT	-	-	-	-	-	USART2_TX
PD6	-	EVENTOUT	-	-	-	SPI2_NSS/I2S2_WS	-	USART2_RX
PD7	-	EVENTOUT	-	-	-	SPI2_SCK/I2S2_CK	-	USART2_CK
PD8	-	EVENTOUT	-	TSC_G6_IO3	-	SPI2_SCK/I2S2_CK	-	USART3_TX
PD9	-	EVENTOUT	-	TSC_G6_IO4	-	-	-	USART3_RX
PD10	-	EVENTOUT	-	-	-	-	-	USART3_CK
PD11	-	EVENTOUT	-	-	-	-	-	USART3_CTS
PD12	-	EVENTOUT	TIM4_CH1	TSC_G8_IO1	-	-	-	USART3_RTS
PD13	-	EVENTOUT	TIM4_CH2	TSC_G8_IO2	-	-	-	-
PD14	-	EVENTOUT	TIM4_CH3	TSC_G8_IO3	-	-	-	-
PD15	-	EVENTOUT	TIM4_CH4	TSC_G8_IO4	-	-	-	-

Table 26. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 1.8V(1) (continued)

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, code executing from RAM	HSE bypass, PLL on	72 MHz	65.5	77.8	78.1	86.6	31.6	35.1	35.6	38.0	mA
			64 MHz	58.7	69.0	69.5	76.5	28.2	31.2	31.7	33.7	
			48 MHz	44.8	51.6	52.2	56.6	21.4	23.3	23.9	25.1	
			32 MHz	30.4	34.2	34.9	37.1	14.4	15.6	16.1	16.8	
			24 MHz	23.1	25.7	26.2	27.6	10.9	11.8	12.2	12.8	
		HSE bypass, PLL off	8 MHz	7.7	8.4	8.9	9.5	3.6	4.0	4.4	5.0	
			1 MHz	1.0	1.3	1.7	2.2	0.5	0.7	1.1	1.7	
		HSI clock, PLL on	64 MHz	54.3	63.3	63.9	70.1	27.9	30.8	31.2	33.2	
			48 MHz	41.5	47.3	48.0	51.9	21.1	23.0	23.5	24.7	
			32 MHz	28.2	31.5	32.2	34.1	14.2	15.3	15.9	16.5	
			24 MHz	21.4	23.6	24.3	25.5	7.2	7.8	8.2	8.8	
		HSI clock, PLL off	8 MHz	7.3	7.9	8.4	9.1	3.6	4.0	4.4	4.9	
	Supply current in Sleep mode, code executing from Flash or RAM	HSE bypass, PLL on	72 MHz	46.4	54.0	54.8	59.5	7.2	7.9	8.4	9.0	
			64 MHz	41.5	48.0	48.8	52.6	6.5	7.1	7.5	8.1	
			48 MHz	31.6	35.9	36.7	39.0	4.9	5.3	5.8	6.4	
			32 MHz	21.4	23.8	24.7	25.7	3.3	3.7	4.2	4.7	
			24 MHz	16.2	17.9	18.6	19.4	2.5	2.8	3.3	3.8	
		HSE bypass, PLL off	8 MHz	5.4	5.9	6.5	7.0	0.8	1.1	1.6	2.1	
			1 MHz	0.7	1.0	1.4	1.9	0.1	0.3	0.7	1.3	
		HSI clock, PLL on	64 MHz	37.0	42.4	43.3	46.4	6.1	6.7	7.2	7.7	
			48 MHz	28.2	31.8	32.7	34.5	4.6	5.0	5.5	6.1	
			32 MHz	19.1	21.2	22.0	22.9	3.1	3.5	4.0	4.5	
			24 MHz	14.5	16.0	16.7	17.4	1.7	2.0	2.4	2.9	
		HSI clock, PLL off	8 MHz	5.0	5.5	6.0	6.6	0.8	1.1	1.5	2.0	

1. To calculate complete device consumption there must be added consumption from VDDA (*Table 27*).
2. Guaranteed by characterization results.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 50: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC and SDADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode. Under reset conditions all I/Os are configured in input floating mode - so if some inputs do not have a defined voltage level then they can generate additional consumption. This consumption is visible on V_{DD} supply and also on V_{DDSDx} supply because some I/Os are powered from SDADCx supply (all I/Os which have SDADC analog input functionality).

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 34: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 35. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ @V_{DD} = 1.8 V, V_{DDA} = 3.3 V	Max	Unit
t_{WUSTOP}	Wakeup from Stop mode	-	3.6	5.21	µs
$t_{WUSLEEP}$	Wakeup from Sleep mode	After WFE instruction	6		CPU clock cycles
t_{WUPOR}	Wakeup from Power off state	Startup after NPOR pin release	62.6	100	µs

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

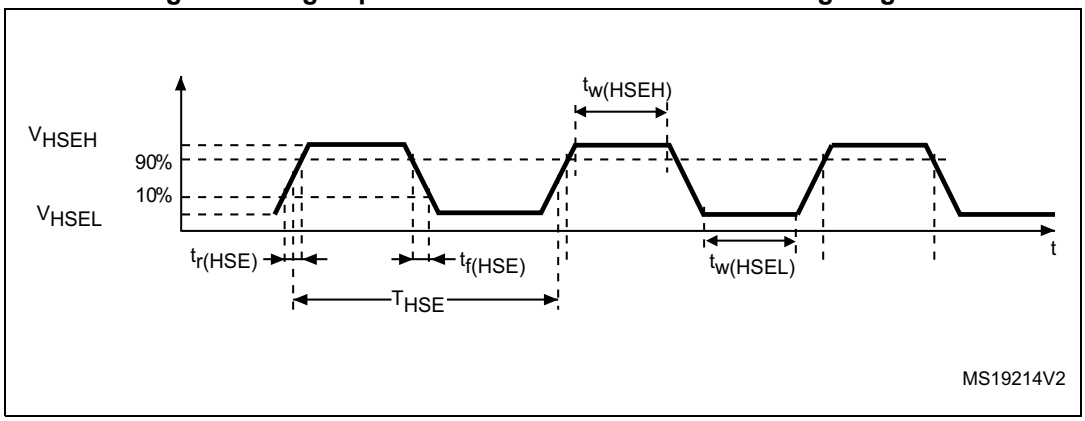
The external clock signal has to respect the I/O characteristics in *Section 6.3.13*. However, the recommended clock input waveform is shown in *Figure 13*.

Table 36. High-speed external user clock characteristics

Symbol	Parameter[1]	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	CSS is on or PLL is used	1	8	32	MHz
		CSS is off, PLL not used	0			
V_{HSEH}	OSC_IN input pin high level voltage	-	0.7 V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DD}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	-	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time	-	-	-	20	

1. Guaranteed by design.

Figure 13. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in *Section 6.3.13*. However, the recommended clock input waveform is shown in *Figure 14*.

Table 37. Low-speed external user clock characteristics

Symbol	Parameter(1)	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time	-	-	-	50	

1. Guaranteed by design.

6.3.13 I/O port characteristics

General input/output characteristics

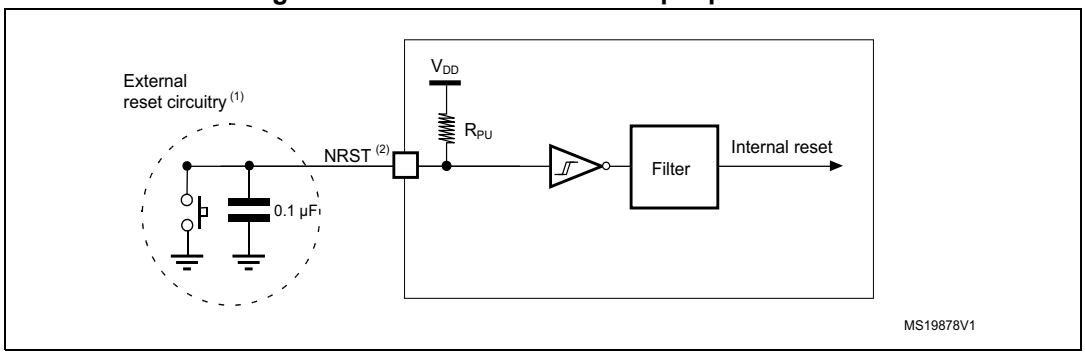
Unless otherwise specified, the parameters given in *Table 50* are derived from tests performed under the conditions summarized in *Table 22*. All I/Os are CMOS and TTL compliant.

Table 50. I/O static characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	$0.3V_{DD}+0.07$(2)	V
		FT and FTf I/O	-	-	$0.475V_{DD}-0.2$(2)	
		BOOT0	-	-	$0.3V_{DD}-0.3$(2)	
		All I/Os except BOOT0 pin	-	-	$0.3V_{DD}$	
V_{IH}	High level input voltage	TC and TTa I/O	$0.445V_{DD}+0.398$(2)	-	-	
		FT and FTf I/O	$0.5V_{DD+0.2}$(2)	-	-	
		BOOT0	$0.2V_{DD}+0.95$(2)	-	-	
		All I/Os except BOOT0 pin	$0.7V_{DD}$	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	200(2)	-	mV
		FT and FTf I/O	-	100(2)	-	
		BOOT0	-	300(2)	-	
I_{lkg}	Input leakage current (3)	TC, FT, FTf and POR I/O TTa in digital mode $V_{SS} \le V_{IN} \le V_{DD}$	-	-	±0.1	µA
		TTa in digital mode $V_{DD} \le V_{IN} \le V_{DDA}$	-	-	1	
		TTa in analog mode $V_{SS} \le V_{IN} \le V_{DDA}$	-	-	±0.2	
		FT and FTf I/O (3) $V_{DD} \le V_{IN} \le 5$ V	-	-	10	
		POR $V_{DDA} \le V_{IN} \le 5$ V	-	-	10	
R_{PU}	Weak pull-up equivalent resistor(4)	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(4)	$V_{IN} = V_{DD}$	25	40	55	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. VDDSD12 is the external power supply for the PB10, and PE7 to PE15 I/O pins (the I/O pin ground is internally connected to VSS). VDDSD3 is the external power supply for PB14 to PB15 and PD8 to PD15 I/O pins (the I/O pin ground is internally connected to VSS). For those pins all V_{DD} supply references in this table are related to their given VDDSDx power supply.
2. Guaranteed by design.
3. Leakage could be higher than maximum value, if negative current is injected on adjacent pins.
4. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

Figure 21. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 53*. Otherwise the reset will not be taken into account by the device.

NPOR pin characteristics

The NPOR pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor to the V_{DDA}, R_{PU} (see *Table 50*).

Unless otherwise specified, the parameters given in *Table 54* are derived from tests performed under ambient temperature and V_{DDA} supply voltage conditions summarized in *Table 22*.

Table 54. NPOR pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NPOR)}$(1)	NPOR Input low level voltage	-	-	-	$0.475V_{DDA}$ - 0.2	V
$V_{IH(NPOR)}$(1)	NPOR Input high level voltage	-	$0.5V_{DDA}$ + 0.2	-	-	
$V_{hys(NPOR)}$(1)	NPOR Schmitt trigger voltage hysteresis	-	-	100	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

6.3.16 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 59* are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 22*.

Note: It is recommended to perform a calibration after each power-up.

Table 59. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	0	-	-	V
$I_{DDA(ADC)}$(1)	Current consumption from V_{DDA}	V_{DDA} = 3.3 V	-	0.9	-	mA
I_{VREF}	Current on the V_{REF} input pin	-	-	160(2)	220(2)	µA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S(3)	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}(3)	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{SRC}(3)	Signal source impedance	See *Equation 1* and *Table 60* for details	-	-	50	kΩ
R_{ADC}(3)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(3)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(3)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	83			$1/f_{ADC}$
t_{lat}(3)	Injection trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.214	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_{latr}(3)	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.143	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(3)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(3)	Power-up time	-	-	-	1	µs
t_{CONV}(3)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	µs
		-	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

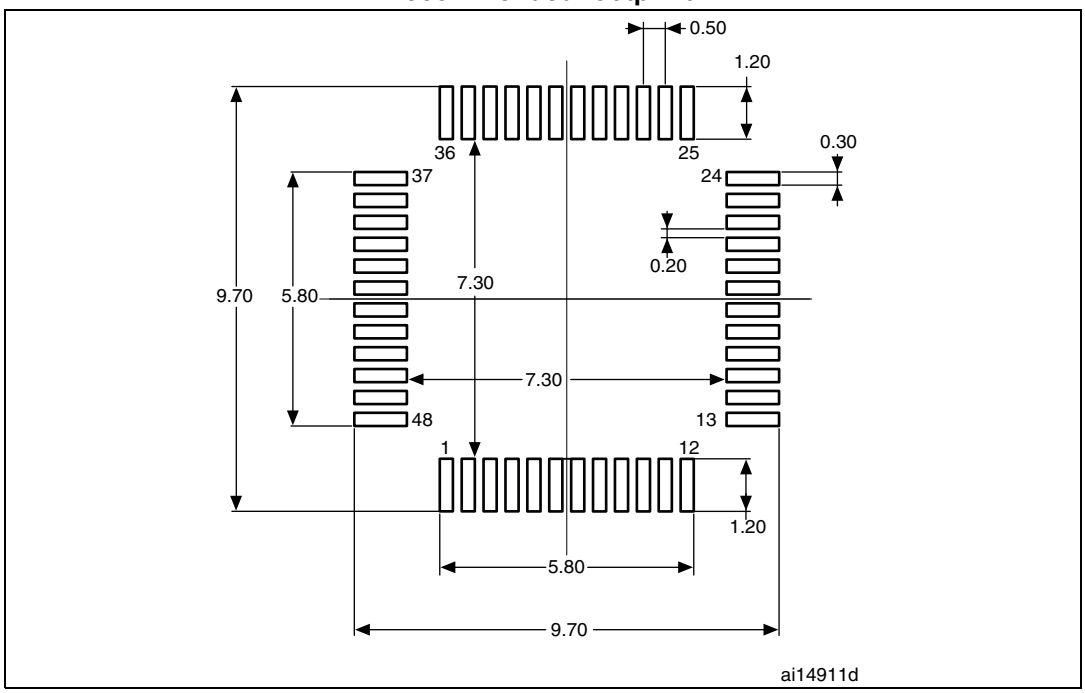
1. During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 µA on I_{DDA} and 60 µA on I_{DD} is present
2. Guaranteed by characterization results.
3. Guaranteed by design.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 59*

6.3.18 Comparator characteristics

Table 63. Comparator characteristics

Symbol	Parameter	Conditions		Min	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	V_{REFINT} scaler not in use		1.65	-	3.6	V
		V_{REFINT} scaler in use		2			
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	V
V_{BG}	V_{REFINT} scaler input voltage	-		-	1.2	-	V
V_{SC}	V_{REFINT} scaler offset voltage	-		-	±5	±10	mV
t_{S_SC}	Scaler startup time from power down	First V_{REFINT} scaler activation after device power on		-	-	1000(2)	ms
		Next activations				0.2	
t_{START}	Comparator startup time	Startup time to reach propagation delay specification		-	-	60	µs
t_D	Propagation delay for 200 mV step with 100 mV overdrive	Ultra-low power mode		-	2	4.5	µs
		Low power mode		-	0.7	1.5	
		Medium power mode		-	0.3	0.6	
		High speed mode	$V_{DDA} \geq 2.7$ V	-	50	100	ns
			$V_{DDA} < 2.7$ V	-	100	240	
	Propagation delay for full range step with 100 mV overdrive	Ultra-low power mode		-	2	7	µs
		Low power mode		-	0.7	2.1	
		Medium power mode		-	0.3	1.2	
		High speed mode	$V_{DDA} \geq 2.7$ V	-	90	180	ns
			$V_{DDA} < 2.7$ V	-	110	300	
V_{offset}	Comparator offset error	-		-	±4	±10	mV
dV_{offset}/dT	Offset error temperature coefficient	-		-	18	-	µV/°C
$I_{DD(COMP)}$	COMP current consumption	Ultra-low power mode		-	1.2	1.5	µA
		Low power mode		-	3	5	
		Medium power mode		-	10	15	
		High speed mode		-	75	100	

Figure 44. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint

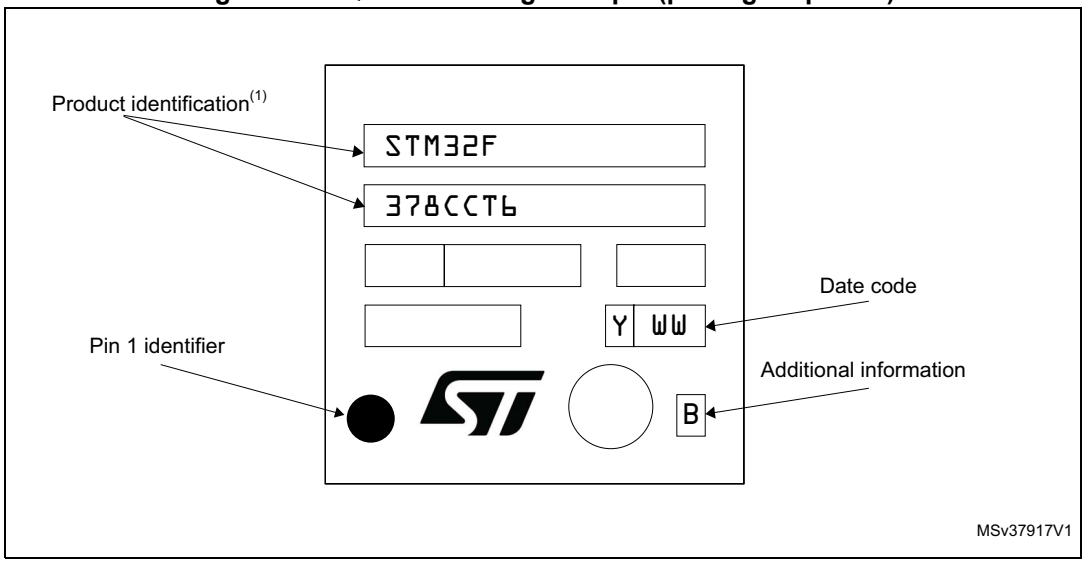


1. Dimensions are expressed in millimeters.

Device marking for LQFP48

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 45. LQFP48 marking example (package top view)



1. Samples marked “ES” are to be considered as “Engineering Samples”: i.e. they are intended to be sent to customer for electrical compatibility evaluation and may be used to start customer qualification where specifically authorized by ST in writing. In no event ST will be liable for any customer usage in production. Only if ST has authorized in writing the customer qualification Engineering Samples can be used for reliability qualification trials.

9 Revision history

Table 80. Document revision history

Date	Revision	Changes
04-Mar-2014	1	Initial release.
09-Apr-2014	2	Removed sub-set part number (64KB and 128KB). Updated *Part numbering on page 128*
21-Jul-2015	3	Updated *Section 7* Updated *Section 3.13* Updated *Section 3.7.1*, *Section 3.7.3* Updated *Table 2: Device overview*, *Table 11: STM32F378xx pin definitions*, *Table 22: General operating conditions*, *Table 47: ESD absolute maximum ratings*, *Table 70: SDADC characteristics*, *Table 74: WLCSP66 - 66-pin, 3.767 x 4.229 mm, 0.4 mm pitch wafer level chip scale package mechanical data* and *Table 75: LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data*, *Table 78: Package thermal characteristics* and *Table 79: Ordering information scheme* Updated *Figure 5: STM32F378xx UFBGA100 ballout*, *Figure 10: Power supply scheme*, *Figure 35: WLCSP66 - 66-pin, 3.767 x 4.229 mm, 0.4 mm pitch wafer level chip scale package outline*, *Figure 36: WLCSP66 marking example (package top view)*, *Figure 38: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint*, *Figure 39: LQFP100 marking example (package top view)*, *Figure 40: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline*, *Figure 41: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint*, *Figure 42: LQFP64 marking example (package top view)*, *Figure 44: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint*, *Figure 45: LQFP48 marking example (package top view)*. Added *Table 30: Typical and maximum current consumption from VBAT supply*, *Table 63: Comparator characteristics*, *Table 73: UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)* Added *Figure 12: Typical VBAT current consumption (LSE and RTC ON/LSEDRV[1:0]='00')*, *Figure 31: Maximum VREFINT scaler startup time from power down* and *Figure 33: UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint*.

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