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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 16x12b, 21x16b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f378rct6

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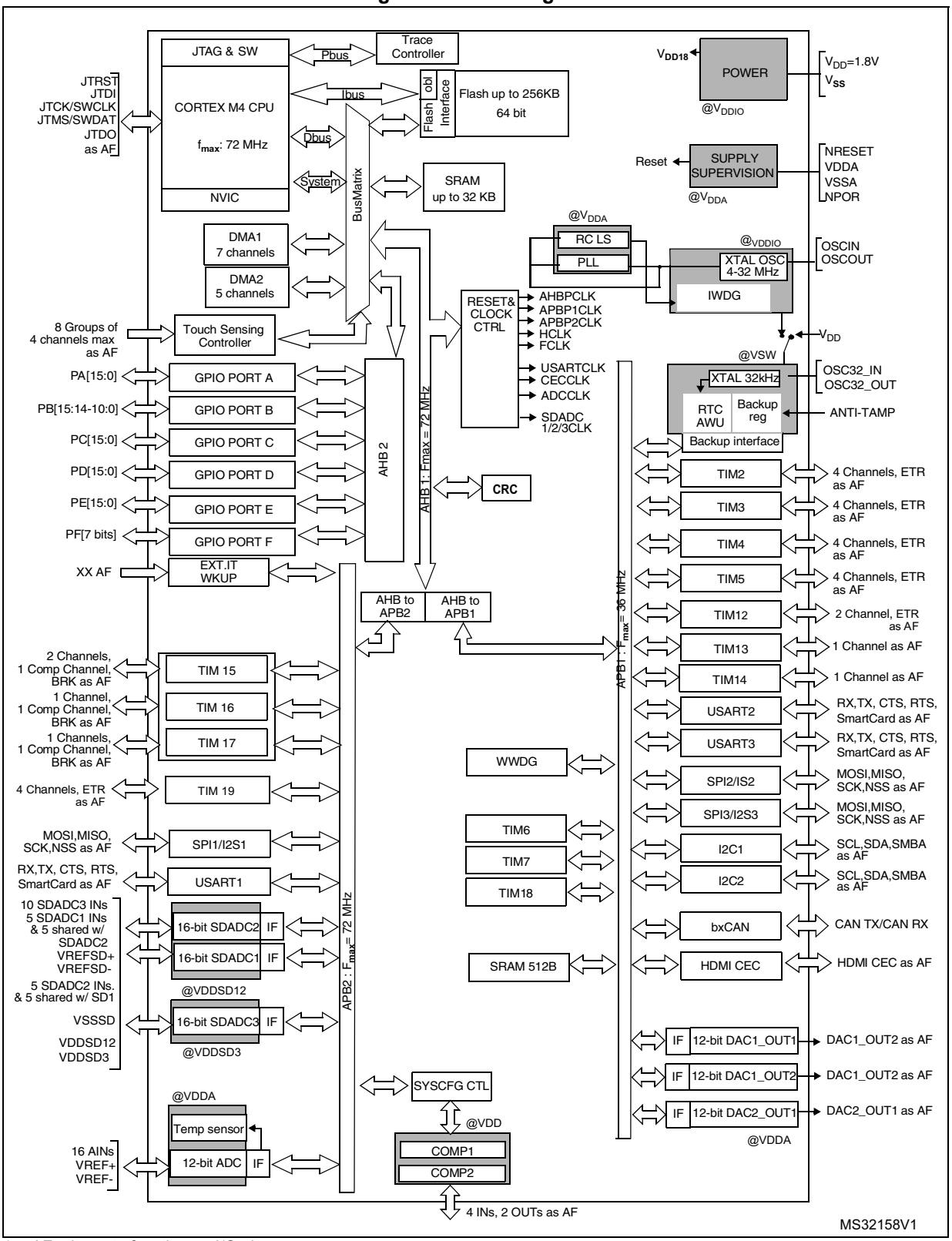
Figure 1. Block diagram



1. AF: alternate function on I/O pins.

Table 7. STM32F378xx I²C implementation (continued)

I²C features(1)	I2C1	I2C2
SMBus	X	X
Wakeup from STOP	X	X

1. X = supported.

3.20 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F378xx embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

All USARTs interfaces are able to communicate at speeds of up to 9 Mbit/s.

They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode, Smartcard mode (ISO/IEC 7816 compliant), autobaudrate feature and have LIN Master/Slave capability. The USART interfaces can be served by the DMA controller.

Refer to *Table 8* for the features of USART1, USART2 and USART3.

Table 8. STM32F378xx USART implementation

USART modes/features(1)	USART1	USART2	USART3
Hardware flow control for modem	X	X	X
Continuous communication using DMA	X	X	X
Multiprocessor communication	X	X	X
Synchronous mode	X	X	X
Smartcard mode	X	X	X
Single-wire half-duplex communication	X	X	X
IrDA SIR ENDEC block	X	X	X
LIN mode	X	X	X
Dual clock domain and wakeup from Stop mode	X	X	X
Receiver timeout interrupt	X	X	X
Modbus communication	X	X	X
Auto baud rate detection	X	X	X
Driver Enable	X	X	X

1. X = supported.

3.21 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I^2S)

Up to three SPIs are able to communicate at up to 18 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The SPIs can be served by the DMA controller.

Three standard I^2S interfaces (multiplexed with SPI1, SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency. All I2S interfaces can operate in half-duplex mode only.

Refer to *Table 9* for the features between SPI1, SPI2 and SPI3.

Table 9. STM32F378xx SPI/I2S implementation

SPI features(1)	SPI1	SPI2	SPI3
Hardware CRC calculation	X	X	X
Rx/Tx FIFO	X	X	X
NSS pulse mode	X	X	X
I2S mode	X	X	X
TI mode	X	X	X
I2S full-duplex mode	-	-	-

1. X = supported.

3.22 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

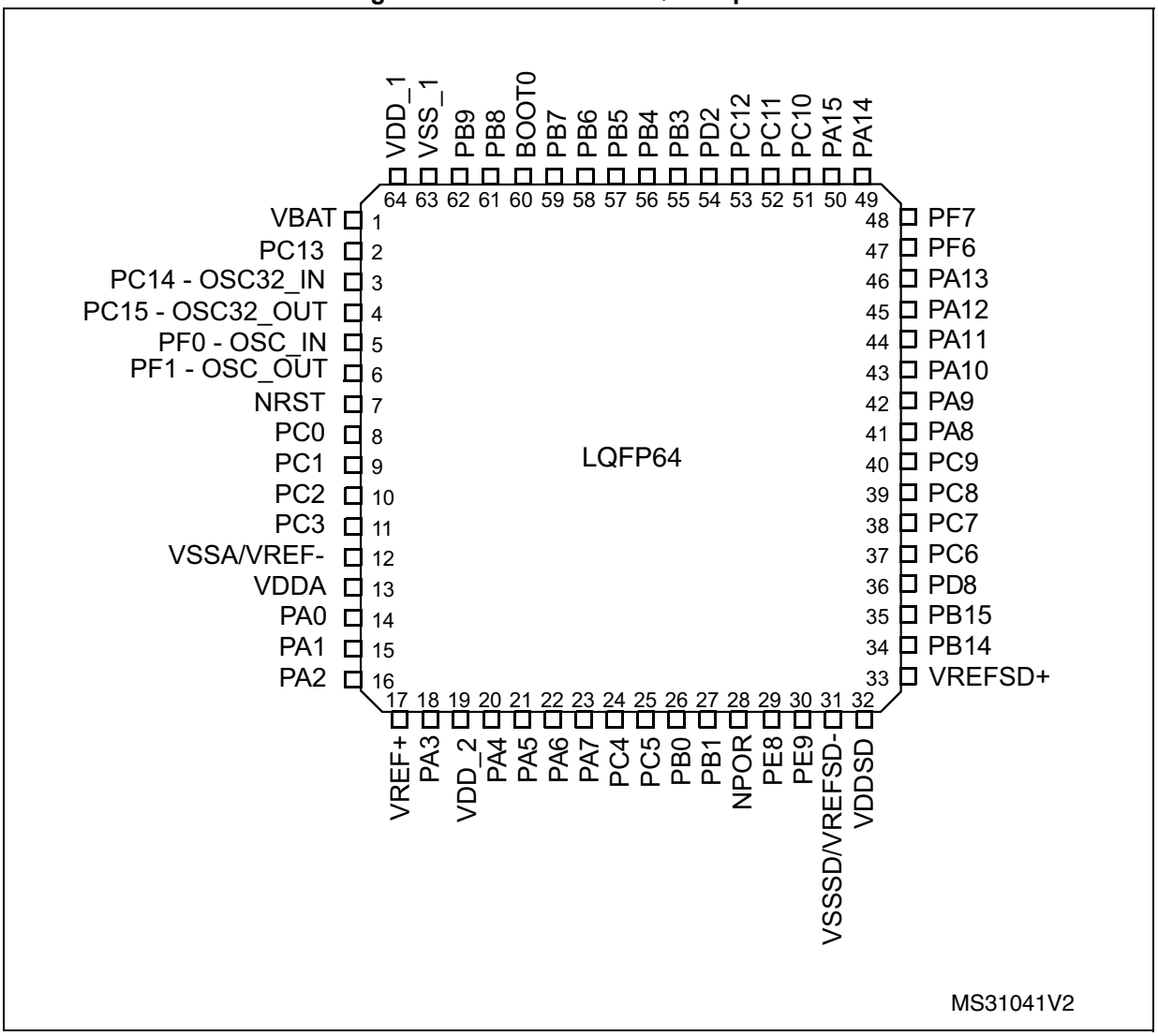
The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI_CEC controller to wakeup the MCU from Stop mode on data reception.

3.23 Controller area network (CAN)

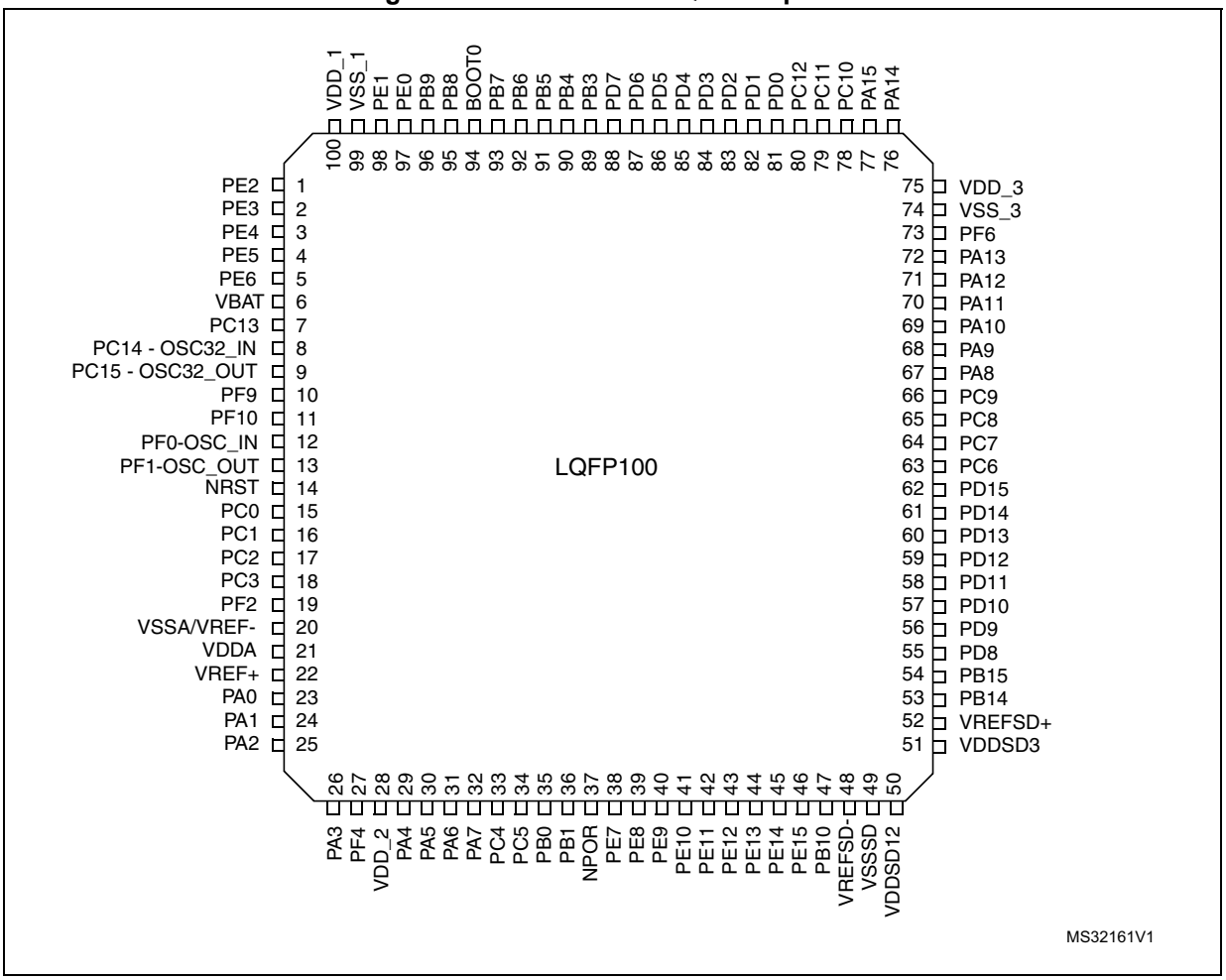
The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

Figure 3. STM32F378xx LQFP64 pinout



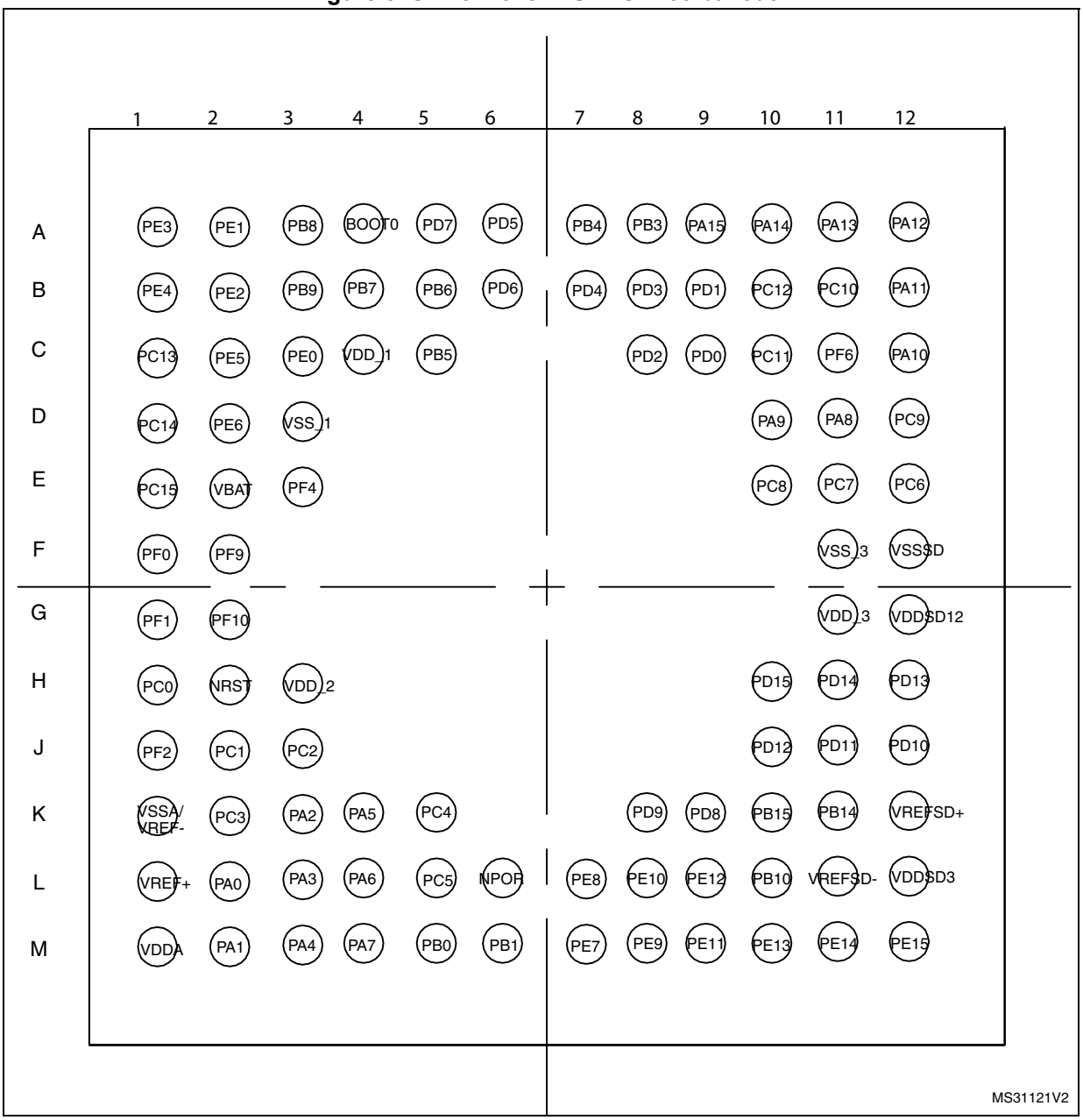
1. The above figure shows the package top view.

Figure 4. STM32F378xx LQFP100 pinout



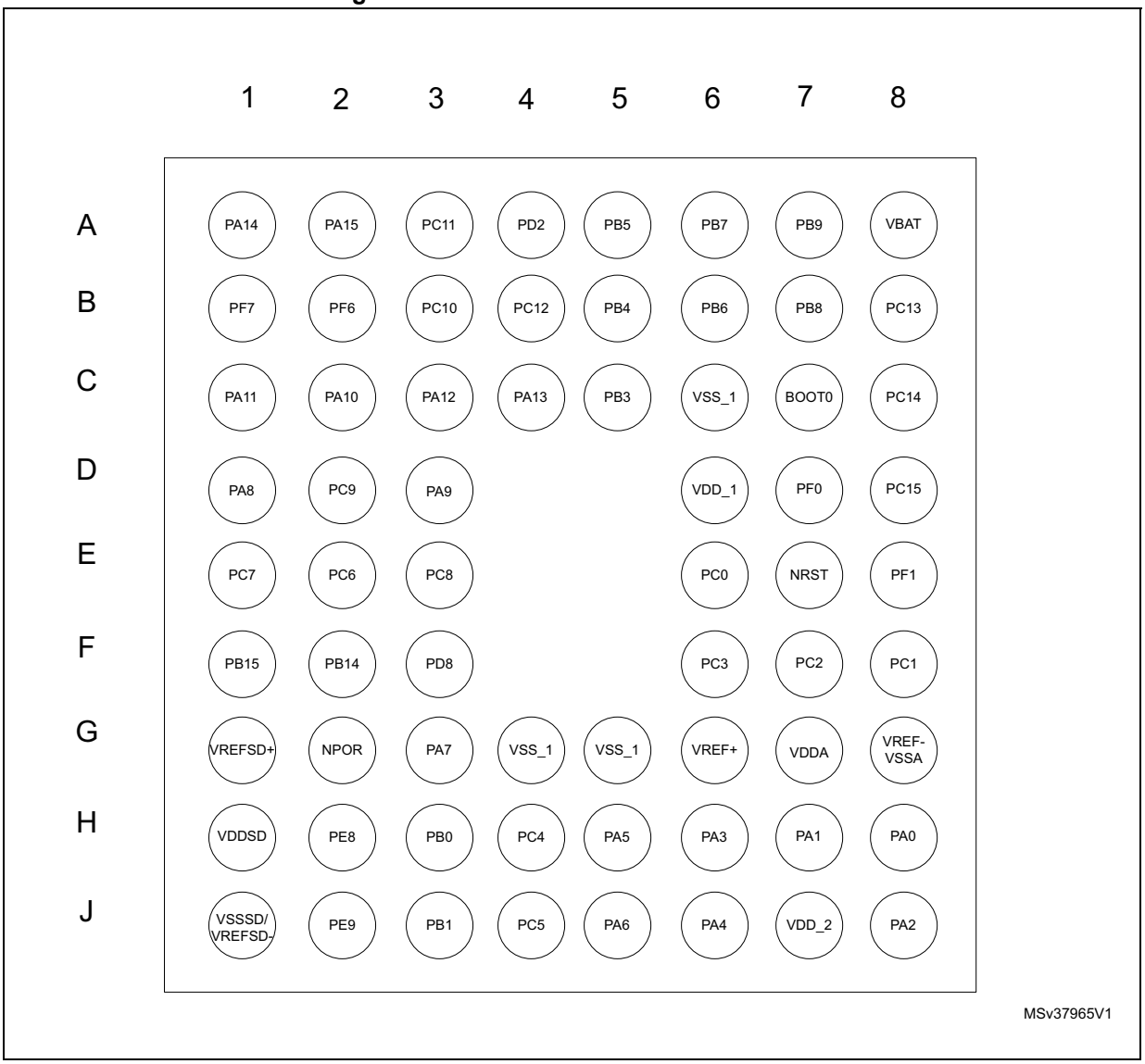
1. The above figure shows the package top view.

Figure 5. STM32F378xx UFBGA100 ballout



1. The above figure shows the package top view.

Figure 6. STM32F378xx WLCSP66 ballout



1. The above figure shows the package top view.

Table 10. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	3.3 V tolerant I/O directly connected to ADC or SDADC
		POR	External power on reset pin with embedded weak pull-up resistor, powered from V_{DDA}
		TC	Standard 3.3V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 12. Alternate functions for port PA

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF14	AF15
PA0	-	TIM2_CH1_ETR	TIM5_CH1_ETR	TSC_G1_IO1	-	-	-	USART2_CTS	COMP1_OUT	-	-	TIM19_CH1	-	EVENTOUT
PA1	RTC_REFIN	TIM2_CH2	TIM5_CH2	TSC_G1_IO2	-	-	SPI3_SCK/I2S3_CK	USART2_RTS	-	TIM15_CH1N	-	TIM19_CH2	-	EVENTOUT
PA2	-	TIM2_CH3	TIM5_CH3	TSC_G1_IO3	-	-	SPI3_MISO/I2S3_MCK	USART2_TX	COMP2_OUT	TIM15_CH1	-	TIM19_CH3	-	EVENTOUT
PA3	-	TIM2_CH4	TIM5_CH4	TSC_G1_IO4	-	-	SPI3_MOSI/I2S3_SD	USART2_RX	-	TIM15_CH2	-	TIM19_CH4	-	EVENTOUT
PA4	-	-	TIM3_CH2	TSC_G2_IO1	-	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	USART2_CK	-	-	TIM12_CH1	-	-	EVENTOUT
PA5	-	TIM2_CH1_ETR	-	TSC_G2_IO2	-	SPI1_SCK/I2S1_CK	-	CEC	-	TIM14_CH1	TIM12_CH2	-	-	EVENTOUT
PA6	-	TIM16_CH1	TIM3_CH1	TSC_G2_IO3	-	SPI1_MISO/I2S1_MCK	-	-	COMP1_OUT	TIM13_CH1	-	-	-	EVENTOUT
PA7	-	TIM17_CH1	TIM3_CH2	TSC_G2_IO4	-	SPI1_MOSI/I2S1_SD	-	-	COMP2_OUT	TIM14_CH1	-	-	-	EVENTOUT
PA8	MCO	-	TIM5_CH1_ETR	-	I2C2_SMBA	SPI2_SCK/I2S2_CK	-	USART1_CK	-	-	TIM4_ETR	-	-	EVENTOUT
PA9	-	-	TIM13_CH1	TSC_G4_IO1	I2C2_SCL	SPI2_MISO/I2S2_MCK	-	USART1_TX	-	TIM15_BKIN	TIM2_CH3	-	-	EVENTOUT
PA10	-	TIM17_BKIN	-	TSC_G4_IO2	I2C2_SDA	SPI2_MOSI/I2S2_SD	-	USART1_RX	-	TIM14_CH1	TIM2_CH4	-	-	EVENTOUT
PA11	-	-	TIM5_CH2	-	-	SPI2_NSS/I2S2_WS	SPI1_NSS/I2S1_WS	USART1_CTS	COMP1_OUT	CAN_RX	TIM4_CH1	-	-	EVENTOUT
PA12	-	TIM16_CH1	TIM5_CH3	-	-	-	SPI1_SCK/I2S1_CK	USART1_RTS	COMP2_OUT	CAN_TX	TIM4_CH2	-	-	EVENTOUT

Table 15. Alternate functions for port PD

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	-	EVENTOUT	TIM19_CH4	-	-	-	-	CAN_RX
PD1	-	EVENTOUT	TIM19_ETR	-	-	-	-	CAN_TX
PD2	-	EVENTOUT	TIM3_ETR	-	-	-	-	-
PD3	-	EVENTOUT	-	-	-	SPI2_MISO/I2S2_MCK	-	USART2_CTS
PD4	-	EVENTOUT	-	-	-	SPI2_MOSI/I2S2_SD	-	USART2_RTS
PD5	-	EVENTOUT	-	-	-	-	-	USART2_TX
PD6	-	EVENTOUT	-	-	-	SPI2_NSS/I2S2_WS	-	USART2_RX
PD7	-	EVENTOUT	-	-	-	SPI2_SCK/I2S2_CK	-	USART2_CK
PD8	-	EVENTOUT	-	TSC_G6_IO3	-	SPI2_SCK/I2S2_CK	-	USART3_TX
PD9	-	EVENTOUT	-	TSC_G6_IO4	-	-	-	USART3_RX
PD10	-	EVENTOUT	-	-	-	-	-	USART3_CK
PD11	-	EVENTOUT	-	-	-	-	-	USART3_CTS
PD12	-	EVENTOUT	TIM4_CH1	TSC_G8_IO1	-	-	-	USART3_RTS
PD13	-	EVENTOUT	TIM4_CH2	TSC_G8_IO2	-	-	-	-
PD14	-	EVENTOUT	TIM4_CH3	TSC_G8_IO3	-	-	-	-
PD15	-	EVENTOUT	TIM4_CH4	TSC_G8_IO4	-	-	-	-

SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 57* for SPI or in *Table 58* for I²S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 22*.

Refer to *Section 6.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 57. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$ (1)	SPI clock frequency	Master mode (C = 30 pF)	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$ (1)	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	8	ns
DuCy(SCK)(1)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	2Tpclk	-	ns
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	4Tpclk	-	
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	Tpclk/2 - 3	Tpclk/2 + 3	
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode	5.5	-	
		Slave mode	6.5	-	
$t_{h(MI)}$ (1)	Data input hold time	Master mode	5	-	
$t_{h(SI)}$ (1)		Slave mode	5	-	
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode, f_{PCLK} = 24 MHz	0	4Tpclk	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	0	24	
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)	-	39	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-	3	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{h(MO)}$ (1)		Master mode (after enable edge)	4	-	

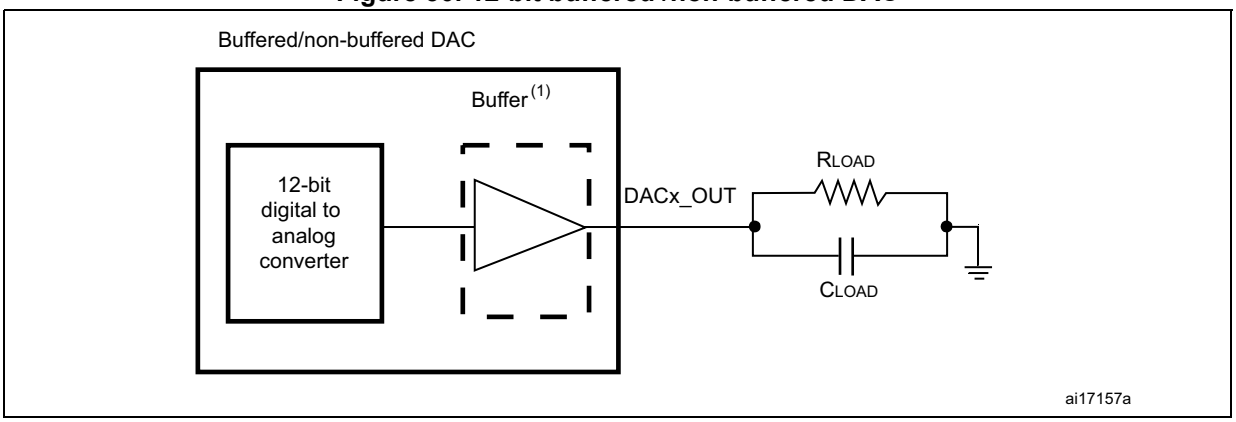
1. Guaranteed by characterization results.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Table 62. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Offset(3)	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{REF+}/2)	-	-	-	±10	mV
		Given for the DAC in 10-bit at V_{REF+} = 3.6 V	-	-	±3	LSB
		Given for the DAC in 12-bit at V_{REF+} = 3.6 V	-	-	±12	LSB
Gain error(3)	Gain error	Given for the DAC in 12bit configuration	-	-	±0.5	%
$t_{SETTLING}$(3)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ	-	3	4	µs
Update rate(3)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ	-	-	1	MS/s
t_{WAKEUP}(3)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.	-	6.5	10	µs
PSRR+ (1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement	No R_{LOAD}, C_{LOAD} = 50 pF	-	-67	-40	dB

1. Guaranteed by design.
2. Quiescent mode refers to the state of the DAC keeping a steady value on the output, so no dynamic consumption is involved.
3. Guaranteed by characterization.

Figure 30. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.22 CAN (controller area network) interface

Refer to *Section 6.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

6.3.23 SDADC characteristics

Table 70. SDADC characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Note
V_{DDSDx}	Power supply	Slow mode (f_{ADC} = 1.5 MHz)	2.2	-	V_{DDA}	V	-
		Normal mode (f_{ADC} = 6 MHz)	2.4	-	V_{DDA}		-
f_{ADC}	SDADC clock frequency	Slow mode (f_{ADC} = 1.5 MHz)	0.5	1.5	1.65	MHz	-
		Normal mode (f_{ADC} = 6 MHz)	0.5	6	6.3		-
V_{REFSD+}	Positive ref. voltage	-	1.1	-	V_{DDSDx}	V	-
V_{REFSD-}	Negative ref. voltage	-	-	V_{SSA}	-	V	-
I_{DDSDx}	Supply current (V_{DDSDx} = 3.3 V)	Normal mode (f_{ADC} = 6 MHz)	-	800	1200	µA	-
		Slow mode (f_{ADC} = 1.5 MHz)	-	-	600		-
		Standby	-	-	200		-
		Power down	-	-	2.5		-
		SD_ADC off	-	-	1		-
V_{AIN}	Common input voltage range	Single ended mode (zero reference)	V_{REFSD-}	-	V_{REFSD+} /gain	V	Voltage on AINP or AINN pin
		Single ended offset mode	V_{REFSD-}	-	V_{REFSD+}/ (gain*2)		
		Differential mode	V_{SSA}	-	V_{DDSDx}		
V_{DIFF}	Differential input voltage	Differential mode only	-V_{REFSD+}/ (gain*2)	-	V_{REFSD+}/ (gain*2)	-	Differential voltage between AINP and AINN
f_S	Sampling rate	Slow mode (f_{ADC} = 1.5 MHz)	-	4.166	-	kHz	f_{ADC}/360
		Slow mode one channel only (f_{ADC} = 1.5 MHz)	-	12.5	-		f_{ADC}/120
		Normal mode multiplexed channel (f_{ADC} = 6 MHz)	-	16.66	-		f_{ADC}/360
		Normal mode one channel only, FAST= 1 (f_{ADC} = 6 MHz)	-	50	-		f_{ADC}/120
t_{CONV}	Conversion time	-	-	1/fs	-	s	-

Table 70. SDADC characteristics (continued)(1)

Symbol	Parameter	Conditions					Min	Typ	Max	Unit	Note
SNR(5)	Signal to noise ratio	Differential mode	gain = 1	f_{ADC} = 1.5 MHz	V_{DDSDx} = 3.3	V_{REFSD+} = 3.3(3)	84	85	-	dB	-
				f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(4)	86	88	-		
						V_{REFSD+} = 3.3	88	92	-		
			gain = 8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(4)	76	78	-		
						V_{REFSD+} = 3.3	82	86	-		
				f_{ADC} = 1.5 MHz		V_{REFSD+} = 3.3(3)	76	80	-		
		Single ended mode	gain = 1	f_{ADC} = 1.5 MHz		V_{REFSD+} = 3.3	80	84	-		
				f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(4)	77	81	-		
						V_{REFSD+} = 3.3	85	90	-		
			gain = 8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(4)	66	71	-		
						V_{REFSD+} = 3.3	74	78	-		

Table 72. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
D1	5.450	5.500	5.550	0.2146	0.2165	0.2185
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
E1	5.450	5.500	5.550	0.2146	0.2165	0.2185
e	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 33. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint

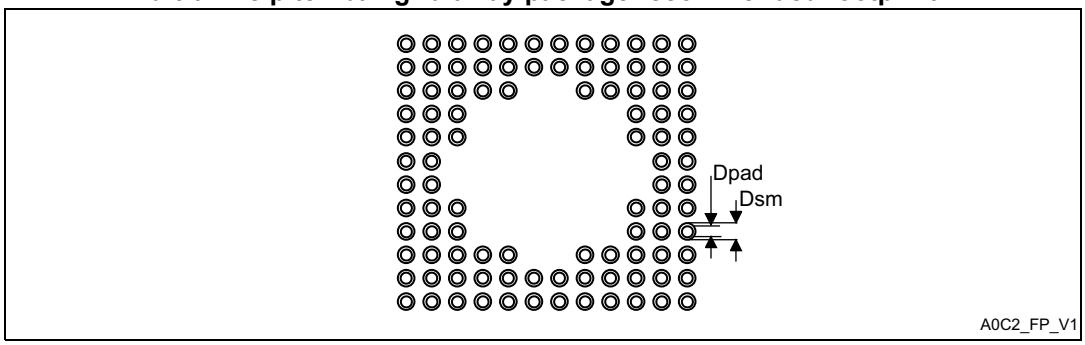


Table 73. UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm

Table 75. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.6 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 22: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times Q_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Q_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = S\ (V_{OL} \times I_{OL}) + S((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 78. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	°C/W
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	55	
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient BGA100 - 7 x 7 mm	59	
	Thermal resistance junction-ambient WLCSP66 - 0.400 mm	53	

7.6.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

9 Revision history

Table 80. Document revision history

Date	Revision	Changes
04-Mar-2014	1	Initial release.
09-Apr-2014	2	Removed sub-set part number (64KB and 128KB). Updated *Part numbering on page 128*
21-Jul-2015	3	Updated *Section 7* Updated *Section 3.13* Updated *Section 3.7.1*, *Section 3.7.3* Updated *Table 2: Device overview*, *Table 11: STM32F378xx pin definitions*, *Table 22: General operating conditions*, *Table 47: ESD absolute maximum ratings*, *Table 70: SDADC characteristics*, *Table 74: WLCSP66 - 66-pin, 3.767 x 4.229 mm, 0.4 mm pitch wafer level chip scale package mechanical data* and *Table 75: LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data*, *Table 78: Package thermal characteristics* and *Table 79: Ordering information scheme* Updated *Figure 5: STM32F378xx UFBGA100 ballout*, *Figure 10: Power supply scheme*, *Figure 35: WLCSP66 - 66-pin, 3.767 x 4.229 mm, 0.4 mm pitch wafer level chip scale package outline*, *Figure 36: WLCSP66 marking example (package top view)*, *Figure 38: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint*, *Figure 39: LQFP100 marking example (package top view)*, *Figure 40: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline*, *Figure 41: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint*, *Figure 42: LQFP64 marking example (package top view)*, *Figure 44: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint*, *Figure 45: LQFP48 marking example (package top view)*. Added *Table 30: Typical and maximum current consumption from VBAT supply*, *Table 63: Comparator characteristics*, *Table 73: UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)* Added *Figure 12: Typical VBAT current consumption (LSE and RTC ON/LSEDRV[1:0]='00')*, *Figure 31: Maximum VREFINT scaler startup time from power down* and *Figure 33: UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint*.