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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

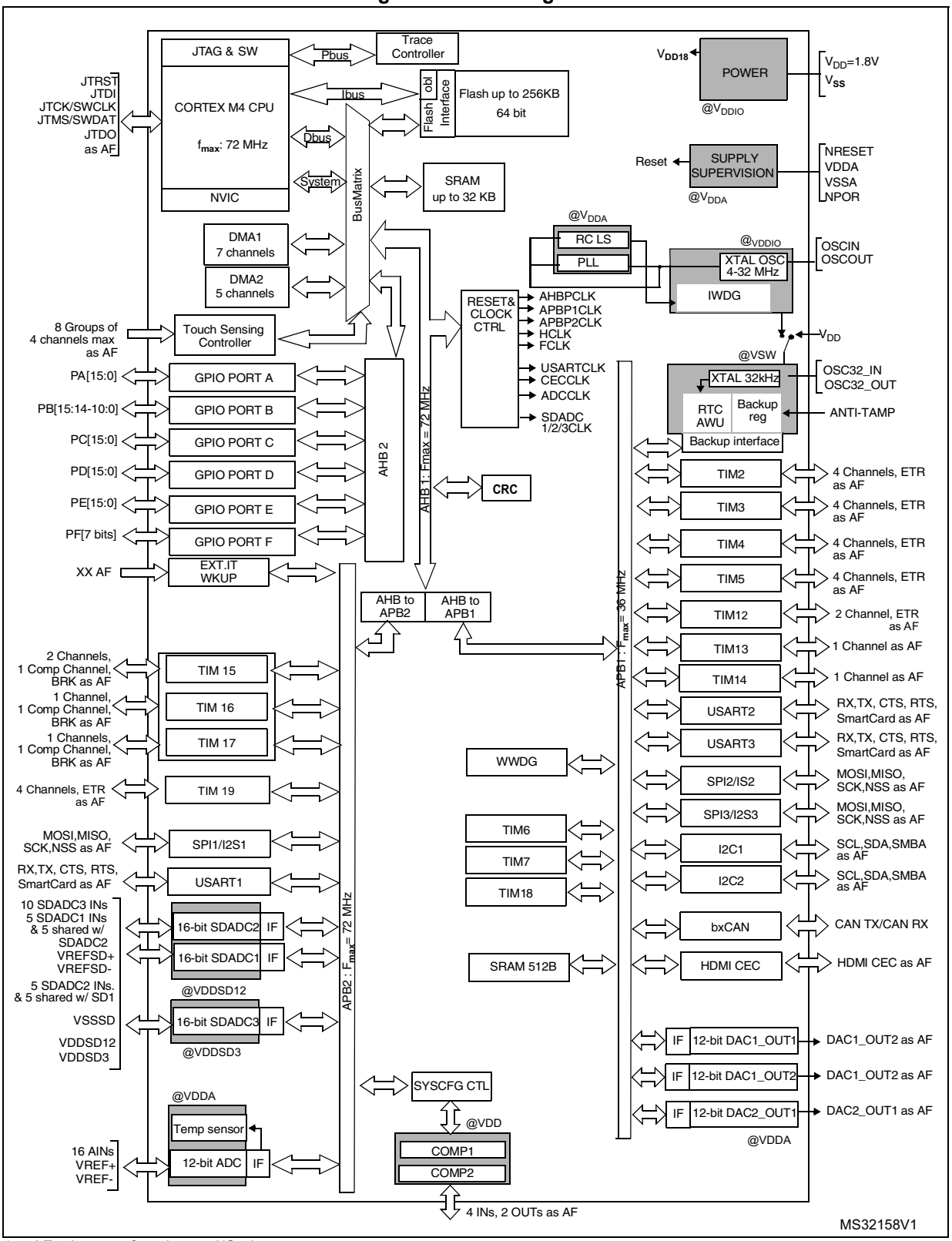
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	52
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 16x12b, 21x16b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	66-UFBGA, WLCSP
Supplier Device Package	66-WLCSP (3.8x4.2)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f378rcy6tr

Table 2. Device overview

Peripheral		STM32F 378Cx	STM32F 378Rx	STM32F 378Vx
Flash (Kbytes)		256		
SRAM (Kbytes)		32		
Timers	General purpose	9 (16-bit) 2 (32 bit)		
	Basic	3 (16-bit)		
Comm. interfaces	SPI/I2S	3		
	I^2C	2		
	USART	3		
	CAN	1		
Capacitive sensing channels		14	17	24
12-bit ADCs		1		
16-bit ADCs Sigma- Delta		3		
12-bit DACs outputs		3		
Analog comparator		2		
Max. CPU frequency		72 MHz		
Main operating voltage		1.8 V +/- 8%		
16-bit SDADC operating voltage		2.2 to 3.6 V		
Operating temperature		Ambient operating temperature: -40 to 85 °C / -40 to 105 °C Junction temperature: -40 to 105 °C / -40 to 125 °C		
Packages		LQFP48	LQFP64, WLCSP66	LQFP100, UFBGA100

Figure 1. Block diagram



1. AF: alternate function on I/O pins.

3 Functional overview

3.1 ARM® Cortex®-M4 core with embedded Flash and SRAM

The ARM Cortex-M4 processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM Cortex-M4 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32F378xx family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the STM32F378xx family.

3.2 Memory protection unit

The memory protection unit (MPU) is used to separate the processing of tasks from the data protection. The MPU can manage up to 8 protection areas that can all be further divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The memory protection unit is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

The Cortex-M4 processor is a high performance 32-bit processor designed for the microcontroller market. It offers significant benefits to developers, including:

- Outstanding processing performance combined with fast interrupt handling
- Enhanced system debug with extensive breakpoint and trace capabilities
- Efficient processor core, system and memories
- Ultralow power consumption with integrated sleep modes
- Platform security robustness with optional integrated memory protection unit (MPU).

With its embedded ARM core, the STM32F378xx devices are compatible with all ARM development tools and software.

3.3 Embedded Flash memory

All STM32F378xx devices feature up to 256 Kbytes of embedded Flash memory available for storing programs and data. The Flash memory access time is adjusted to the CPU clock frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).

3.4 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

3.5 Embedded SRAM

All STM32F378xx devices feature up to 32 Kbytes of embedded SRAM with hardware parity check. The memory can be accessed in read/write at CPU clock speed with 0 wait states.

3.6 Boot modes

At startup, Boot0 pin and Boot1 option bit are used to select one of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10), USART2 (PD5/PD6) or I2C (PB6/PB7).

3.7 Power management

3.7.1 Power supply schemes

- V_{DD}: external power supply for I/Os and core. It is provided externally through V_{DD} pins, and can be 1.8 V +/- 8%.
- V_{DDA} = 1.65 to 3.6 V:
  - external analog power supplies for Reset blocks, RCs and PLL
  - supply voltage for 12-bit ADC, DACs and comparators (minimum voltage to be applied to V_{DDA} is 2.4 V when the 12-bit ADC and DAC are used).
- V_{DDSD12} and V_{DDSD3} = 2.2 to 3.6 V: supply voltages for SDADC1/2 and SDADCD3 sigma delta ADCs. Independent from V_{DD}/V_{DDA}.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers when V_{DD} is not present.

Table 12. Alternate functions for port PA

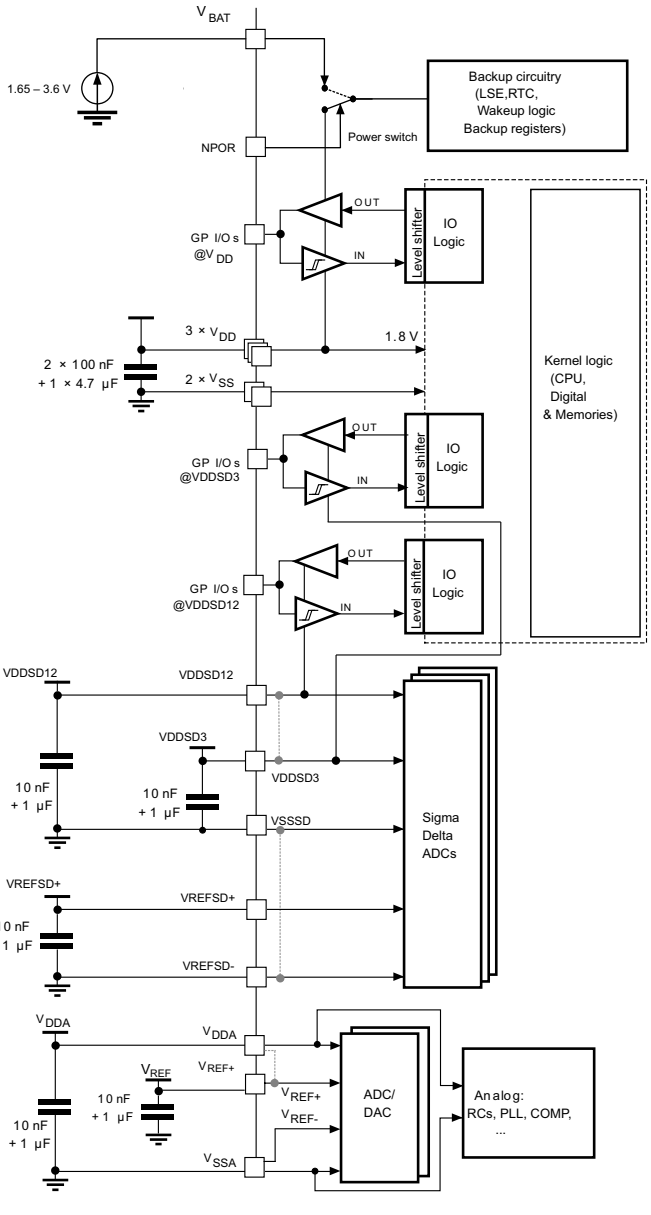
Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF14	AF15
PA0	-	TIM2_CH1_ETR	TIM5_CH1_ETR	TSC_G1_IO1	-	-	-	USART2_CTS	COMP1_OUT	-	-	TIM19_CH1	-	EVENTOUT
PA1	RTC_REFIN	TIM2_CH2	TIM5_CH2	TSC_G1_IO2	-	-	SPI3_SCK/I2S3_CK	USART2_RTS	-	TIM15_CH1N	-	TIM19_CH2	-	EVENTOUT
PA2	-	TIM2_CH3	TIM5_CH3	TSC_G1_IO3	-	-	SPI3_MISO/I2S3_MCK	USART2_TX	COMP2_OUT	TIM15_CH1	-	TIM19_CH3	-	EVENTOUT
PA3	-	TIM2_CH4	TIM5_CH4	TSC_G1_IO4	-	-	SPI3_MOSI/I2S3_SD	USART2_RX	-	TIM15_CH2	-	TIM19_CH4	-	EVENTOUT
PA4	-	-	TIM3_CH2	TSC_G2_IO1	-	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	USART2_CK	-	-	TIM12_CH1	-	-	EVENTOUT
PA5	-	TIM2_CH1_ETR	-	TSC_G2_IO2	-	SPI1_SCK/I2S1_CK	-	CEC	-	TIM14_CH1	TIM12_CH2	-	-	EVENTOUT
PA6	-	TIM16_CH1	TIM3_CH1	TSC_G2_IO3	-	SPI1_MISO/I2S1_MCK	-	-	COMP1_OUT	TIM13_CH1	-	-	-	EVENTOUT
PA7	-	TIM17_CH1	TIM3_CH2	TSC_G2_IO4	-	SPI1_MOSI/I2S1_SD	-	-	COMP2_OUT	TIM14_CH1	-	-	-	EVENTOUT
PA8	MCO	-	TIM5_CH1_ETR	-	I2C2_SMBA	SPI2_SCK/I2S2_CK	-	USART1_CK	-	-	TIM4_ETR	-	-	EVENTOUT
PA9	-	-	TIM13_CH1	TSC_G4_IO1	I2C2_SCL	SPI2_MISO/I2S2_MCK	-	USART1_TX	-	TIM15_BKIN	TIM2_CH3	-	-	EVENTOUT
PA10	-	TIM17_BKIN	-	TSC_G4_IO2	I2C2_SDA	SPI2_MOSI/I2S2_SD	-	USART1_RX	-	TIM14_CH1	TIM2_CH4	-	-	EVENTOUT
PA11	-	-	TIM5_CH2	-	-	SPI2_NSS/I2S2_WS	SPI1_NSS/I2S1_WS	USART1_CTS	COMP1_OUT	CAN_RX	TIM4_CH1	-	-	EVENTOUT
PA12	-	TIM16_CH1	TIM5_CH3	-	-	-	SPI1_SCK/I2S1_CK	USART1_RTS	COMP2_OUT	CAN_TX	TIM4_CH2	-	-	EVENTOUT

Table 14. Alternate functions for port PC

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0	-	EVENTOUT	TIM5_CH1_ETR	-	-	-	-	-
PC1	-	EVENTOUT	TIM5_CH2	-	-	-	-	-
PC2	-	EVENTOUT	TIM5_CH3	-	-	SPI2_MISO/I2S2_MCK	-	-
PC3	-	EVENTOUT	TIM5_CH4	-	-	SPI2_MOSI/I2S2_SD	-	-
PC4	-	EVENTOUT	TIM13_CH1	TSC_G3_IO1	-	-	-	USART1_TX
PC5	-	EVENTOUT	-	TSC_G3_IO2	-	-	-	USART1_RX
PC6	-	EVENTOUT	TIM3_CH1	-	-	SPI1_NSS/I2S1_WS	-	-
PC7	-	EVENTOUT	TIM3_CH2	-	-	SPI1_SCK/I2S1_CK	-	-
PC8	-	EVENTOUT	TIM3_CH3	-	-	SPI1_MISO/I2S1_MCK	-	-
PC9	-	EVENTOUT	TIM3_CH4	-	-	SPI1_MOSI/I2S1_SD	-	-
PC10	-	EVENTOUT	TIM19_CH1	-	-	-	SPI3_SCK/I2S3_CK	USART3_TX
PC11	-	EVENTOUT	TIM19_CH2	-	-	-	SPI3_MISO/I2S3_MCK	USART3_RX
PC12	-	EVENTOUT	TIM19_CH3	-	-	-	SPI3_MOSI/I2S3_SD	USART3_CK
PC13	-	-	-	-	-	-	-	-
PC14	-	-	-	-	-	-	-	-
PC15	-	-	-	-	-	-	-	-

6.1.6 Power supply scheme

Figure 10. Power supply scheme



1. Dotted lines represent the internal connections on low pin count packages, joining the dedicated supply pins.

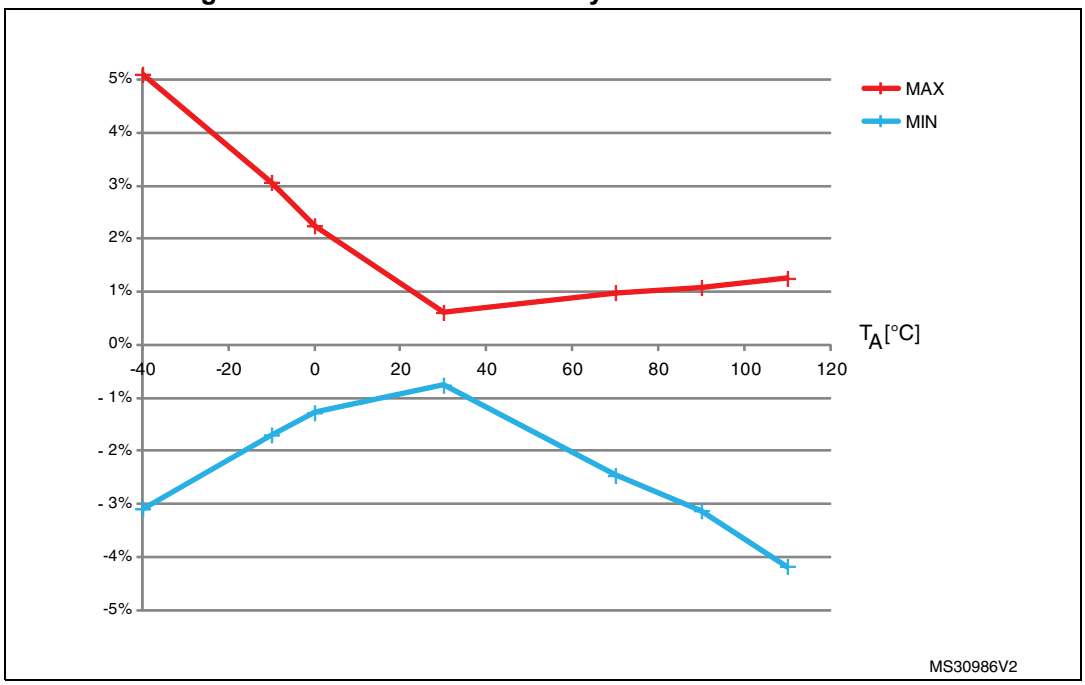
Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc..) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

Table 32. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Sleep mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash or RAM, PLL on	72 MHz	42.6	6.7	mA
			64 MHz	38.0	6.0	
			48 MHz	28.7	4.5	
			32 MHz	19.3	3.1	
			24 MHz	14.6	2.4	
			16 MHz	9.8	1.7	
		Running from HSE crystal clock 8 MHz, code executing from Flash or RAM, PLL off	8 MHz	4.8	0.8	
			4 MHz	3.0	0.7	
			2 MHz	1.9	0.6	
			1 MHz	1.3	0.6	
			500 kHz	1.0	0.6	
			125 kHz	0.8	0.5	
I_{DDA}(1)	Supply current in Sleep mode from V_{DDA} supply	Running from HSE crystal clock 8 MHz, code executing from Flash or RAM, PLL on	72 MHz	243.1	243.1	µA
			64 MHz	214.1	214.1	
			48 MHz	159.4	159.4	
			32 MHz	109.1	109.1	
			24 MHz	84.7	84.7	
			16 MHz	60.6	60.6	
		Running from HSE crystal clock 8 MHz, code executing from Flash or RAM, PLL off	8 MHz	1.0	1.0	
			4 MHz	1.0	1.0	
			2 MHz	1.0	1.0	
			1 MHz	1.0	1.0	
			500 kHz	1.0	1.0	
			125 kHz	1.0	1.0	

1. V_{DDA} monitoring is off, V_{DDSD12} monitoring is off.

Figure 17. HSI oscillator accuracy characterization results



Low-speed internal (LSI) RC oscillator

Table 41. LSI oscillator characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	60	kHz
$t_{su(LSI)}$(2)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(2)	LSI oscillator power consumption	-	0.75	1.2	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design.

6.3.8 PLL characteristics

The parameters given in *Table 42* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22*.

Table 42. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock(1)	1(2)	-	24(2)	MHz
	PLL input clock duty cycle	40(2)	-	60(2)	%
f_{PLL_OUT}	PLL multiplier output clock	16(2)	-	72	MHz
t_{LOCK}	PLL lock time	-	-	200(2)	µs
Jitter	Cycle-to-cycle jitter	-	-	300(2)	ps

1. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.
2. Guaranteed by design.

6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 45*. They are based on the EMS levels and classes defined in application note AN1709.

Table 45. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 1.8 V, LQFP100, T_A = +25 °C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 1.8 V, LQFP100, T_A = +25 °C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 48. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence or oscillator frequency deviation).

The test results are given in *Table 49*.

6.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 50* are derived from tests performed under the conditions summarized in *Table 22*. All I/Os are CMOS and TTL compliant.

Table 50. I/O static characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	$0.3V_{DD}+0.07$(2)	V
		FT and FTf I/O	-	-	$0.475V_{DD}-0.2$(2)	
		BOOT0	-	-	$0.3V_{DD}-0.3$(2)	
		All I/Os except BOOT0 pin	-	-	$0.3V_{DD}$	
V_{IH}	High level input voltage	TC and TTa I/O	$0.445V_{DD}+0.398$(2)	-	-	
		FT and FTf I/O	$0.5V_{DD+0.2}$(2)	-	-	
		BOOT0	$0.2V_{DD}+0.95$(2)	-	-	
		All I/Os except BOOT0 pin	$0.7V_{DD}$	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	200(2)	-	mV
		FT and FTf I/O	-	100(2)	-	
		BOOT0	-	300(2)	-	
I_{lkg}	Input leakage current (3)	TC, FT, FTf and POR I/O TTa in digital mode $V_{SS} \le V_{IN} \le V_{DD}$	-	-	±0.1	µA
		TTa in digital mode $V_{DD} \le V_{IN} \le V_{DDA}$	-	-	1	
		TTa in analog mode $V_{SS} \le V_{IN} \le V_{DDA}$	-	-	±0.2	
		FT and FTf I/O (3) $V_{DD} \le V_{IN} \le 5$ V	-	-	10	
		POR $V_{DDA} \le V_{IN} \le 5$ V	-	-	10	
R_{PU}	Weak pull-up equivalent resistor(4)	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(4)	$V_{IN} = V_{DD}$	25	40	55	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. VDDSD12 is the external power supply for the PB10, and PE7 to PE15 I/O pins (the I/O pin ground is internally connected to VSS). VDDSD3 is the external power supply for PB14 to PB15 and PD8 to PD15 I/O pins (the I/O pin ground is internally connected to VSS). For those pins all V_{DD} supply references in this table are related to their given VDDSDx power supply.
2. Guaranteed by design.
3. Leakage could be higher than maximum value, if negative current is injected on adjacent pins.
4. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

Note: I/O pins are powered from V_{DD} voltage except pins which can be used as SDADC inputs:

- The PB10 and PE7 to PE15 I/O pins are powered from V_{DDSD12}.

- PB14 to PB15 and PD8 to PD15 I/O pins are powered from V_{DDSD3}. All I/O pin ground is internally connected to V_{SS}.

V_{DD} mentioned in the Table 50 represents power voltage for a given I/O pin (V_{DD} or V_{DDSD12} or V_{DDSD3}).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology parameters. The coverage of these requirements is shown in *Figure 18* for standard I/Os, and in *Figure 19* for 5 V tolerant I/Os. The following curves are design simulation results, not tested in production.

Figure 18. TC and TTa I/O input characteristics

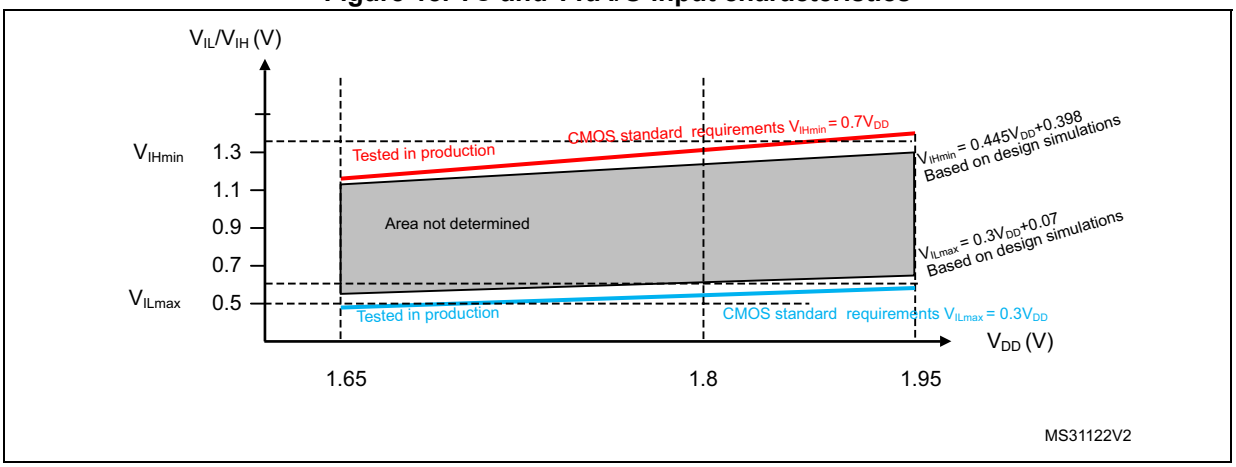
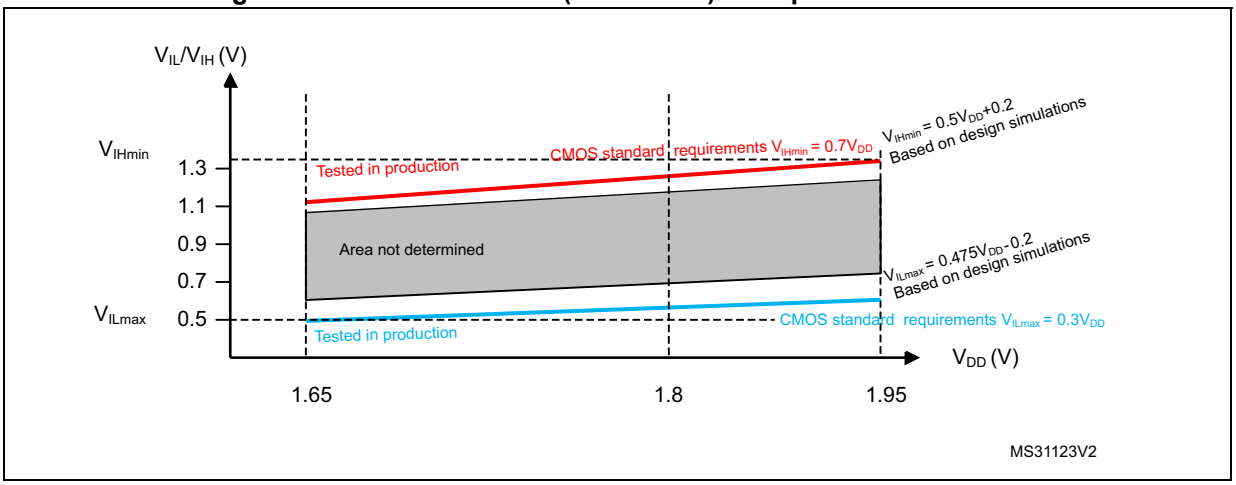


Figure 19. Five volt tolerant (FT and FTf) I/O input characteristics

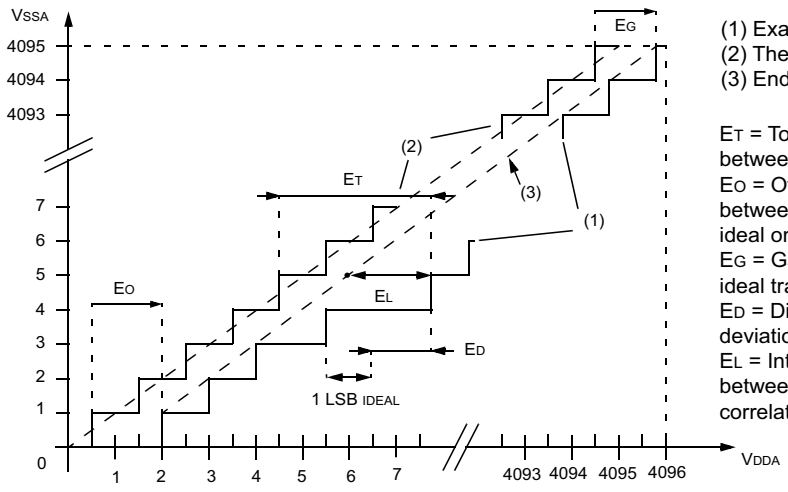


Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ± 8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}).

2. ADC accuracy vs. negative injection current: Injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.13* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Guaranteed by characterization results.

Figure 28. ADC accuracy characteristics

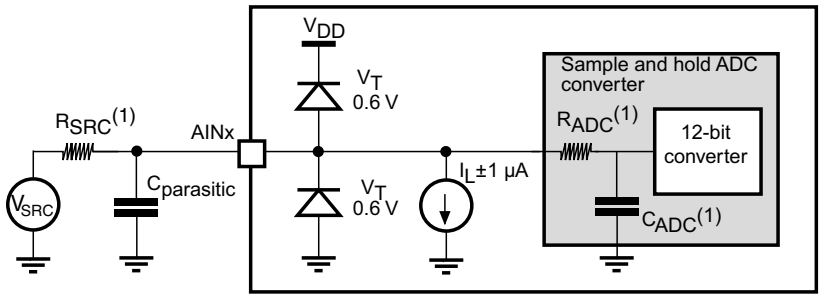


(1) Example of an actual transfer curve
(2) The ideal transfer curve
(3) End point correlation line

E_T = Total Unajusted Error: maximum deviation between the actual and ideal transfer curves.
E_O = Offset Error: maximum deviation between the first actual transition and the first ideal one.
E_G = Gain Error: deviation between the last ideal transition and the last actual one.
E_D = Differential Linearity Error: maximum deviation between actual steps and the ideal ones.
E_L = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

MS19880V2

Figure 29. Typical connection diagram using the ADC



MS32163V1

1. Refer to *Table 59* for the values of R_{SRC}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 10*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

Table 70. SDADC characteristics (continued)(1)

Symbol	Parameter	Conditions					Min	Typ	Max	Unit	Note
Rain	Analog input impedance	One channel, gain = 0.5, f_{ADC} = 1.5 MHz					-	540	-	kΩ	see reference manual for detailed description
		One channel, gain = 0.5, f_{ADC} = 6 MHz					-	135	-		
		One channel, gain = 8, f_{ADC} = 6 MHz					-	47	-		
t_{CALIB}	Calibration time	f_{ADC} = 6 MHz, one offset calibration					-	5120	-	µs	30720/f_{ADC}
t_{STAB}	Stabilization time	From power down f_{ADC} = 6 MHz					-	100	-	µs	600/f_{ADC}, 75/f_{ADC} if SLOWCK = 1
$t_{STANDBY}$	Wakeup from standby time	f_{ADC} = 6 MHz					-	50	-	µs	300/f_{ADC}
		f_{ADC} = 1.5 MHz					-	50	-		75/f_{ADC} if SLOWCK = 1
EO	Offset error	Differential mode	gain = 1	f_{ADC} = 1.5 MHz	V_{DDSDx} = 3.3	V_{REFSD+} = 3.3	-	-	110	uV	after offset calibration
				f_{ADC} = 6 MHz		V_{REFSD+} = 1.2	-	-	110		
						V_{REFSD+} = 3.3	-	-	100		
			gain = 8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2	-	-	70		
						V_{REFSD+} = 3.3	-	-	100		
				f_{ADC} = 1.5 MHz		V_{REFSD+} = 3.3	-	-	90		
		Single ended mode	gain = 1	-		V_{REFSD+} = 1.2	-	-	2100		
						V_{REFSD+} = 3.3	-	-	2000		
			gain = 8			V_{REFSD+} = 1.2	-	-	1500		
						V_{REFSD+} = 3.3	-	-	1800		
$D_{voffsettemp}$	Offset drift with temperature	Differential or single ended mode, gain = 1, V_{DDSDx} = 3.3 V					-	10	15	uV/K	-
EG	Gain error	All gains, differential mode, single ended mode					-2.4	-2.7	-3.1	%	negative gain error = data result are greater than ideal

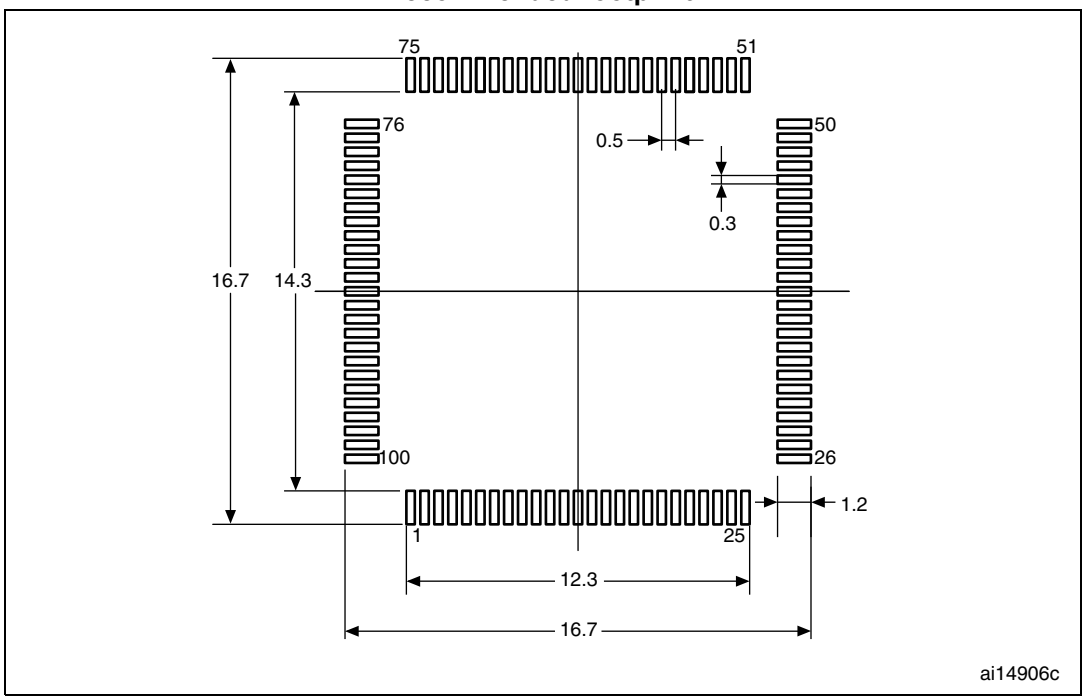
Table 70. SDADC characteristics (continued)(1)

Symbol	Parameter	Conditions				Min	Typ	Max	Unit	Note
EGT	Gain drift with temperature	gain = 1, differential mode, single ended mode				-	0	-	ppm /K	-
EL	Integral linearity error(2)	Differential mode	gain = 1	V_{DDSDx} = 3.3	V_{REFSD+} = 1.2	-	-	16	LSB	-
					V_{REFSD+} = 3.3	-	-	14		
			gain = 8		V_{REFSD+} = 1.2	-	-	26		
					V_{REFSD+} = 3.3	-	-	14		
		Single ended mode	gain = 1		V_{REFSD+} = 1.2	-	-	31		
					V_{REFSD+} = 3.3	-	-	23		
			gain = 8		V_{REFSD+} = 1.2	-	-	80		
					V_{REFSD+} = 3.3	-	-	35		
ED	Differential linearity error	Differential mode	gain = 1	V_{DDSDx} = 3.3	V_{REFSD+} = 1.2	-	-	2.4	LSB	-
					V_{REFSD+} = 3.3	-	-	1.8		
			gain = 8		V_{REFSD+} = 1.2	-	-	3.6		
					V_{REFSD+} = 3.3	-	-	2.9		
		Single ended mode	gain = 1		V_{REFSD+} = 1.2	-	-	3.2		
					V_{REFSD+} = 3.3	-	-	2.8		
			gain = 8		V_{REFSD+} = 1.2	-	-	4.1		
					V_{REFSD+} = 3.3	-	-	3.3		

Table 70. SDADC characteristics (continued)(1)

Symbol	Parameter	Conditions					Min	Typ	Max	Unit	Note
SNR(5)	Signal to noise ratio	Differential mode	gain = 1	f_{ADC} = 1.5 MHz	V_{DDSDx} = 3.3	V_{REFSD+} = 3.3(3)	84	85	-	dB	-
				f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(4)	86	88	-		
						V_{REFSD+} = 3.3	88	92	-		
			gain = 8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(4)	76	78	-		
						V_{REFSD+} = 3.3	82	86	-		
				f_{ADC} = 1.5 MHz		V_{REFSD+} = 3.3(3)	76	80	-		
		Single ended mode	gain = 1	f_{ADC} = 1.5 MHz		V_{REFSD+} = 3.3	80	84	-		
				f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(4)	77	81	-		
						V_{REFSD+} = 3.3	85	90	-		
			gain = 8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(4)	66	71	-		
						V_{REFSD+} = 3.3	74	78	-		

Figure 38. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint

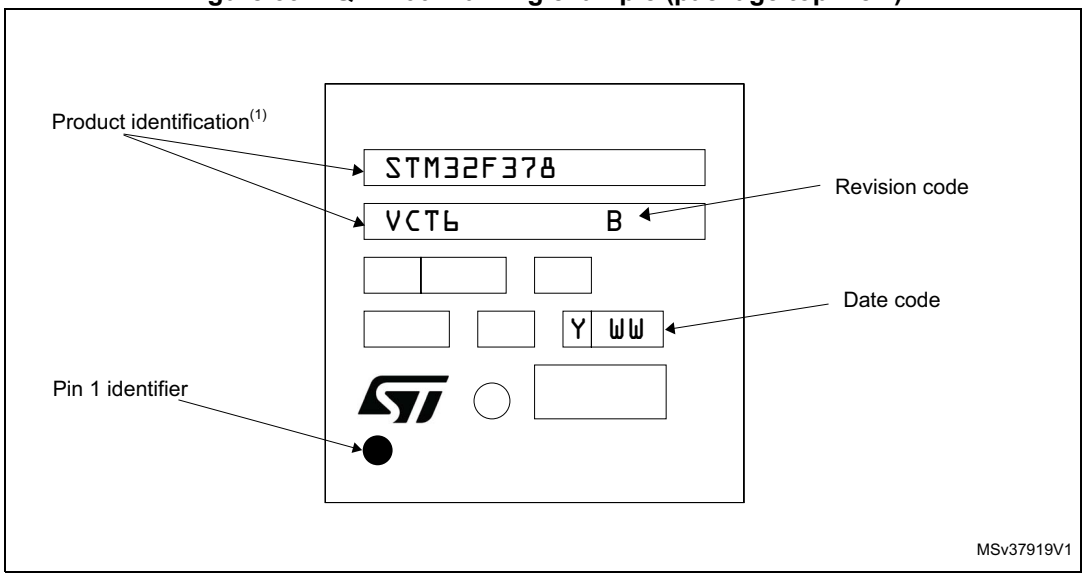


1. Dimensions are expressed in millimeters.

Device marking for LQFP100

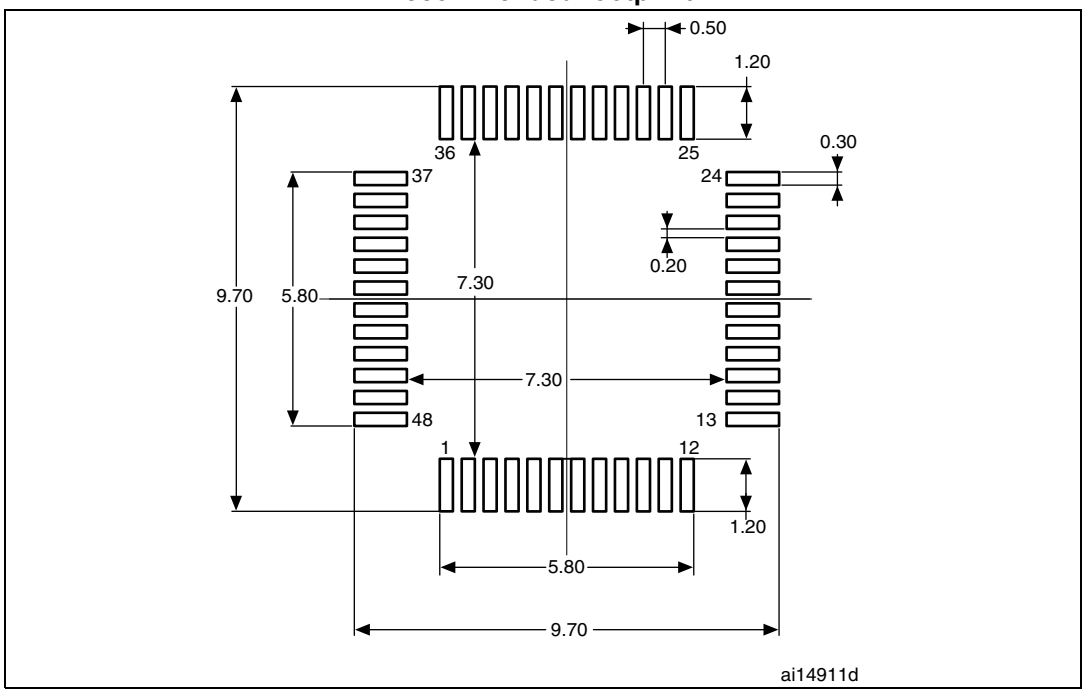
The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 39. LQFP100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Figure 44. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint

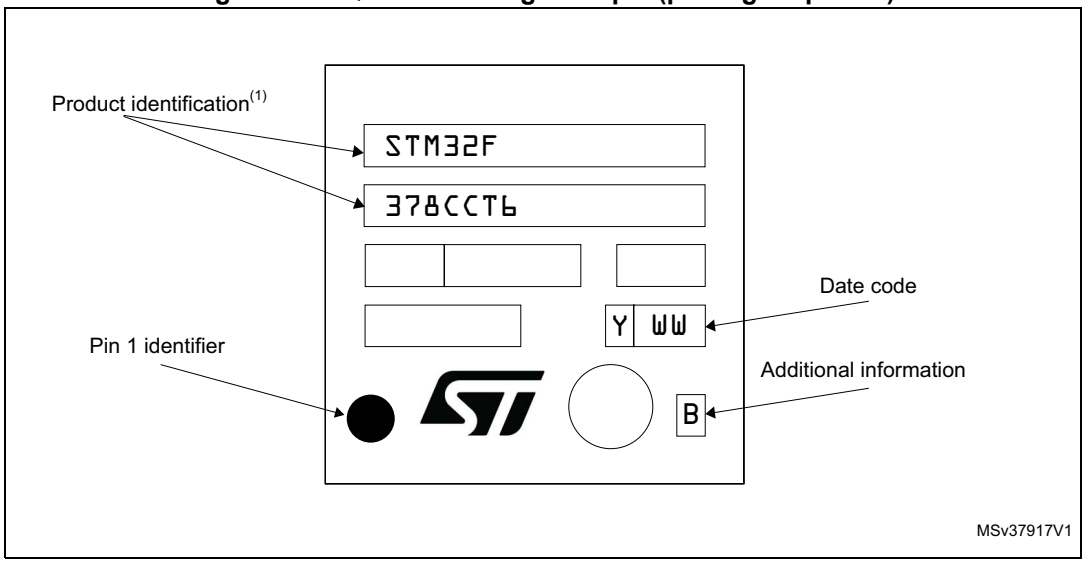


1. Dimensions are expressed in millimeters.

Device marking for LQFP48

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 45. LQFP48 marking example (package top view)



1. Samples marked “ES” are to be considered as “Engineering Samples”: i.e. they are intended to be sent to customer for electrical compatibility evaluation and may be used to start customer qualification where specifically authorized by ST in writing. In no event ST will be liable for any customer usage in production. Only if ST has authorized in writing the customer qualification Engineering Samples can be used for reliability qualification trials.

7.6 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 22: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times Q_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Q_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = S\ (V_{OL} \times I_{OL}) + S((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 78. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	°C/W
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	55	
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient BGA100 - 7 x 7 mm	59	
	Thermal resistance junction-ambient WLCSP66 - 0.400 mm	53	

7.6.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org