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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	83
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 16x12b, 21x16b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f378vct6

3.7.2 Power supply supervisor

Device power on reset is controlled through the external NPOR pin. The device remains in reset mode when NPOR is held low. NPOR pin has an internal pull-up resistor so the external driver can be open drain type.

To guarantee a proper power-on reset, the NPOR pin must be held low until V_{DD} is stable.

When V_{DD} is stable, the reset state can be exited by:

- either putting the NPOR pin in high impedance. NPOR pin has an internal pull up.
- or forcing the pin to high level by connecting it to V_{DDA}.

3.7.3 Low-power modes

The STM32F378xx supports two low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled.

  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the USARTs, the I2Cs, the CEC the COMPx and the RTC alarm.

3.8 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

3.9 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

Table 3. Capacitive sensing GPIOs available on STM32F378xx devices (continued)

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
3	TSC_G3_IO1	PC4	7	TSC_G7_IO1	PE2
	TSC_G3_IO2	PC5		TSC_G7_IO2	PE3
	TSC_G3_IO3	PB0		TSC_G7_IO3	PE4
	TSC_G3_IO4	PB1		TSC_G7_IO4	PE5
4	TSC_G4_IO1	PA9	8	TSC_G8_IO1	PD12
	TSC_G4_IO2	PA10		TSC_G8_IO2	PD13
	TSC_G4_IO3	PA13		TSC_G8_IO3	PD14
	TSC_G4_IO4	PA14		TSC_G8_IO4	PD15

1. This GPIO offers a reduced touch sensing sensitivity. It is thus recommended to use it as sampling capacitor I/O.

Table 4. No. of capacitive sensing channels available on STM32F378xx devices

Analog I/O group	Number of capacitive sensing channels		
	STM32F378Cx	STM32F378Rx	STM32F378Vx
G1	3	3	3
G2	2	3	3
G3	1	3	3
G4	3	3	3
G5	3	3	3
G6	2	2	3
G7	0	0	3
G8	0	0	3
Number of capacitive sensing channels	14	17	24

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} =1.8 V, V_{DDA} = V_{DDSDx} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC and SDADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

Figure 8. Pin loading conditions

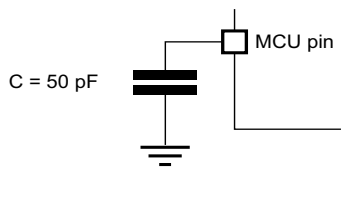


Figure 9. Pin input voltage

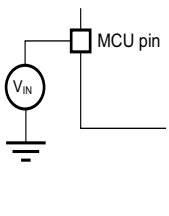
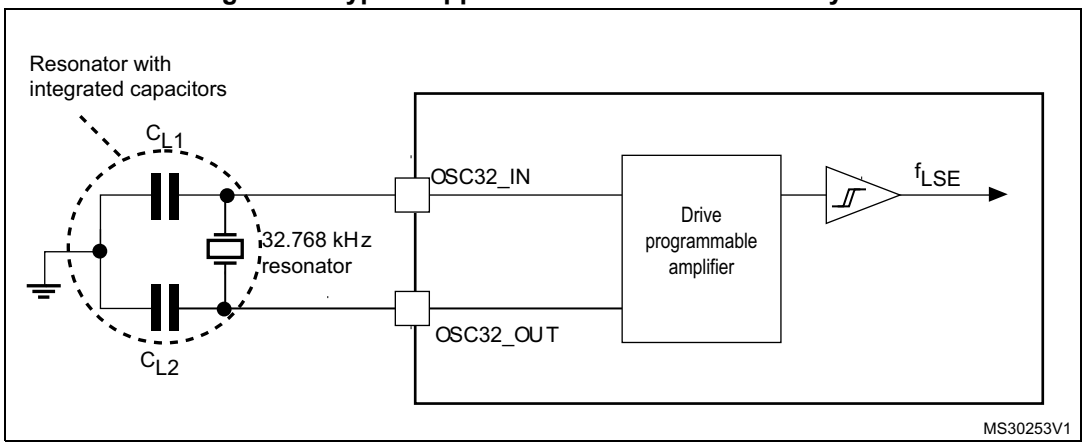


Figure 16. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.7 Internal clock source characteristics

The parameters given in *Table 40* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22*.

The provided curves are characterization results, not tested in production.

High-speed internal (HSI) RC oscillator

Table 40. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1(2)	%
$DuCy_{(HSI)}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI}	Accuracy of the HSI oscillator (factory calibrated)	T_A = –40 to 105 °C	–3.8(3)	-	4.6(3)	%
		T_A = –10 to 85 °C	–2.9(3)	-	2.9(3)	%
		T_A = 0 to 70 °C	–2.3(3)	-	–2.2(3)	%
		T_A = 25 °C	–1	-	1	%
$t_{su(HSI)}$	HSI oscillator startup time	-	1(3)	-	2(3)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	80	100(3)	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 48. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence or oscillator frequency deviation).

The test results are given in *Table 49*.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on all VDD_x and VDDSDx, plus the maximum Run consumption of the MCU sourced on V_{DD} cannot exceed the absolute maximum rating SI_{VDD} (see *Table 20*).
- The sum of the currents sunk by all the I/Os on all VSS_x and VSSSD, plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating SI_{VSS} (see *Table 20*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 51* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22*. All I/Os are CMOS and TTL compliant (FT, TTa or TC unless otherwise specified).

Table 51. Output voltage characteristics (1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(2)	Output low level voltage for an I/O pin	I_{IO} = +4 mA 1.65 V < V_{DD} < 1.95 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin	I_{IO} = +4 mA 1.65 V < V_{DD} < 1.95 V	V_{DD}–0.4	-	
V_{OL}(2)(4)	Output low level voltage for an I/O pin powered by VDDSDx(1)	I_{IO} = +8 mA 2.7 V < VDDSDx < 3.6 V	-	0.4	
V_{OH}(3)(4)	Output high level voltage for an I/O pin powered by VDDSDx(1)		VDDSDx –0.4	-	
V_{OL}(2)(4)	Output low level voltage for an I/O pin powered by VDDSDx(1)	I_{IO} = +20 mA 2.7 V < VDDSDx < 3.6 V	-	1.3	
V_{OH}(3)(4)	Output high level voltage for an I/O pin powered by VDDSDx(1)		VDDSDx –1.3	-	
V_{OLFM+}(2)	Output low level voltage for a FTf I/O pins in FM+ mode	I_{IO} = +10 mA 1.65 V < V_{DD} < 1.95 V	-	0.4	

1. VDDSD12 is the external power supply for the PB10, and PE7 to PE15 I/O pins (the I/O pin ground is internally connected to VSS). VDDSD3 is the external power supply for PB14 to PB15 and PD8 to PD15 I/O pins (the I/O pin ground is internally connected to VSS). For those pins all V_{DD} supply references in this table are related to their given VDDSDx power supply.
2. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 20* and the sum of I_{IO} (I/O ports and control pins) must not exceed $I_{VSS(\Sigma)}$.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 20* and the sum of I_{IO} (I/O ports and control pins) must not exceed $I_{VDD(\Sigma)}$.
4. Guaranteed by design.

Note: I/O pins are powered from V_{DD} voltage except pins which can be used as SDADC inputs:

- The PB10 and PE7 to PE15 I/O pins are powered from V_{DDSD12}.

- PB14 to PB15 and PD8 to PD15 I/O pins are powered from V_{DDSD3}. All I/O pin ground is internally connected to V_{SS}.

V_{DD} mentioned in the Table 51 represents power voltage for a given I/O pin (V_{DD} or V_{DDSD12} or V_{DDSD3}).

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 20* and *Table 52*, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22*.

Table 52. I/O AC characteristics(1)

OSPEEDRy [1:0] value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	1	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	4	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	62.5	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	62.5	
11	$f_{max(IO)out}$	Maximum frequency(2)(3)	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	25	ns
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	25	
FM+ configuration (4)	$f_{max(IO)out}$	Maximum frequency(2)	CL = 50 pF, V_{DD} = 1.65 V to 1.95 V	-	0.5	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	16	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	44	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the RM0313 reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 20*.
3. Guaranteed by design.
4. The I/O speed configuration is bypassed in FM+ I/O mode. Refer to the STM32F37xx reference manual RM0313 for a description of FM+ I/O mode configuration

Figure 23. SPI timing diagram - slave mode and CPHA = 0

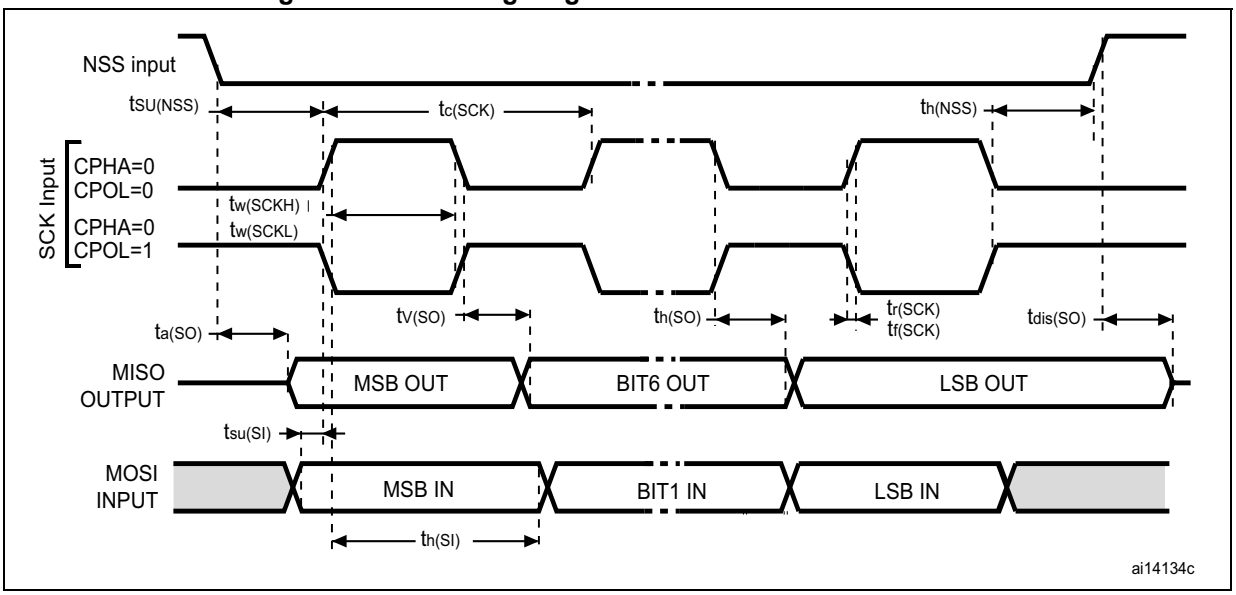
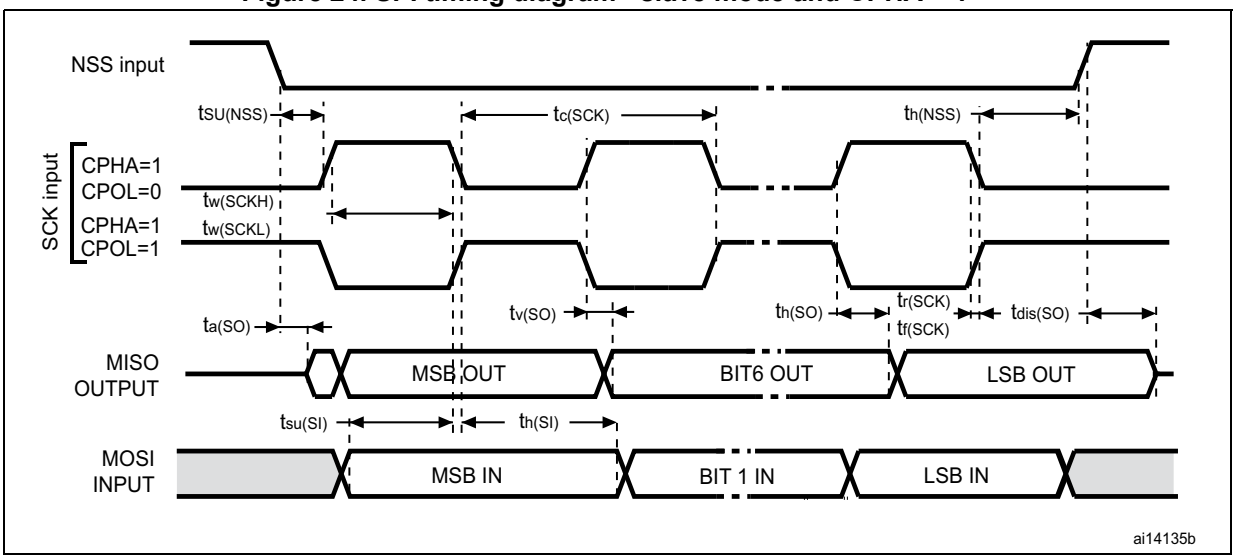


Figure 24. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at $0.5V_{DD}$ level and with external C_L = 30 pF.

Table 58. I^2S characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
DuCy(SCK)(1)	I2S slave input clock duty cycle	Slave mode	30	70	%
f_{CK}(1) $1/t_{c(CK)}$	I^2S clock frequency	Master mode (data: 16 bits, Audio frequency = 48 kHz)	1.528	1.539	MHz
		Slave mode	0	12.288	
$t_{r(CK)}$(1) $t_{f(CK)}$	I^2S clock rise and fall time	Capacitive load C_L = 30 pF	-	8	ns
$t_{v(WS)}$ (1)	WS valid time	Master mode	4	-	
$t_{h(WS)}$ (1)	WS hold time	Master mode	4	-	
$t_{su(WS)}$ (1)	WS setup time	Slave mode	2	-	
$t_{h(WS)}$ (1)	WS hold time	Slave mode	-	-	
$t_{w(CKH)}$ (1)	I2S clock high time	Master f_{PCLK}= 16 MHz, audio frequency = 48 kHz	306	-	
$t_{w(CKL)}$ (1)	I2S clock low time		312	-	
$t_{su(SD\_MR)}$ (1)	Data input setup time	Master receiver	6	-	
$t_{su(SD\_SR)}$ (1)		Slave receiver	3	-	
$t_{h(SD\_MR)}$(1)	Data input hold time	Master receiver	1.5	-	
$t_{h(SD\_SR)}$ (1)		Slave receiver	1.5	-	
$t_{v(SD\_ST)}$ (1)	Data output valid time	Slave transmitter (after enable edge)	-	16	
$t_{h(SD\_ST)}$ (1)	Data output hold time	Slave transmitter (after enable edge)	16	-	
$t_{v(SD\_MT)}$ (1)	Data output valid time	Master transmitter (after enable edge)	-	2	
$t_{h(SD\_MT)}$ (1)	Data output hold time	Master transmitter (after enable edge)	0	-	

1. Guaranteed by characterization results.

6.3.18 Comparator characteristics

Table 63. Comparator characteristics

Symbol	Parameter	Conditions		Min	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	V_{REFINT} scaler not in use		1.65	-	3.6	V
		V_{REFINT} scaler in use		2			
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	V
V_{BG}	V_{REFINT} scaler input voltage	-		-	1.2	-	V
V_{SC}	V_{REFINT} scaler offset voltage	-		-	±5	±10	mV
t_{S_SC}	Scaler startup time from power down	First V_{REFINT} scaler activation after device power on		-	-	1000(2)	ms
		Next activations				0.2	
t_{START}	Comparator startup time	Startup time to reach propagation delay specification		-	-	60	µs
t_D	Propagation delay for 200 mV step with 100 mV overdrive	Ultra-low power mode		-	2	4.5	µs
		Low power mode		-	0.7	1.5	
		Medium power mode		-	0.3	0.6	
		High speed mode	$V_{DDA} \geq 2.7$ V	-	50	100	ns
			$V_{DDA} < 2.7$ V	-	100	240	
	Propagation delay for full range step with 100 mV overdrive	Ultra-low power mode		-	2	7	µs
		Low power mode		-	0.7	2.1	
		Medium power mode		-	0.3	1.2	
		High speed mode	$V_{DDA} \geq 2.7$ V	-	90	180	ns
			$V_{DDA} < 2.7$ V	-	110	300	
V_{offset}	Comparator offset error	-		-	±4	±10	mV
dV_{offset}/dT	Offset error temperature coefficient	-		-	18	-	µV/°C
$I_{DD(COMP)}$	COMP current consumption	Ultra-low power mode		-	1.2	1.5	µA
		Low power mode		-	3	5	
		Medium power mode		-	10	15	
		High speed mode		-	75	100	

6.3.19 Temperature sensor characteristics

Table 64. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C ± 5 °C, V_{DDA}= 3.3 V	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C ± 5 °C V_{DDA}= 3.3 V	0x1FFF F7C2 - 0x1FFF F7C3

Table 65. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}(1)	Startup time	4	-	10	µs
T_{S_temp}(2)(1)	ADC sampling time when reading the temperature	17.1	-	-	µs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.20 V_{BAT} monitoring characteristics

Table 66. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	2	-	-
Er(1)	Error on Q	-1	-	+1	%
T_{S_vbat}(2)	ADC sampling time when reading the V_{BAT} 1mV accuracy	5	-	-	µs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.21 Timer characteristics

The parameters given in *Table 67* are guaranteed by design.

Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 67. TIMx(1) (2)characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	13.9	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 72 MHz	0	24	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2)	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	0.0139	910	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	-	59.65	s

1. TIMx is used as a general term to refer to the TIM2, TIM3, TIM4, TIM5, TIM6, TIM7, TIM12, TIM13, TIM14, TIM15, TIM16 , TIM17, TIM18 and TIM19 timers.
2. Guaranteed by characterization results.

Table 68. IWDG min/max timeout period at 40 kHz (LSI) (1)(2)

Prescaler divider	PR[2:0] bits	Min timeout (ms) RL[11:0]= 0x000	Max timeout (ms) RL[11:0]= 0xFFF
/4	0	0.1	409.6
/8	1	0.2	819.2
/16	2	0.4	1638.4
/32	3	0.8	3276.8
/64	4	1.6	6553.6
/128	5	3.2	13107.2
/256	7	6.4	26214.4

1. These timings are given for a 40 kHz clock but the microcontroller's internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.
2. Guaranteed by characterization results.

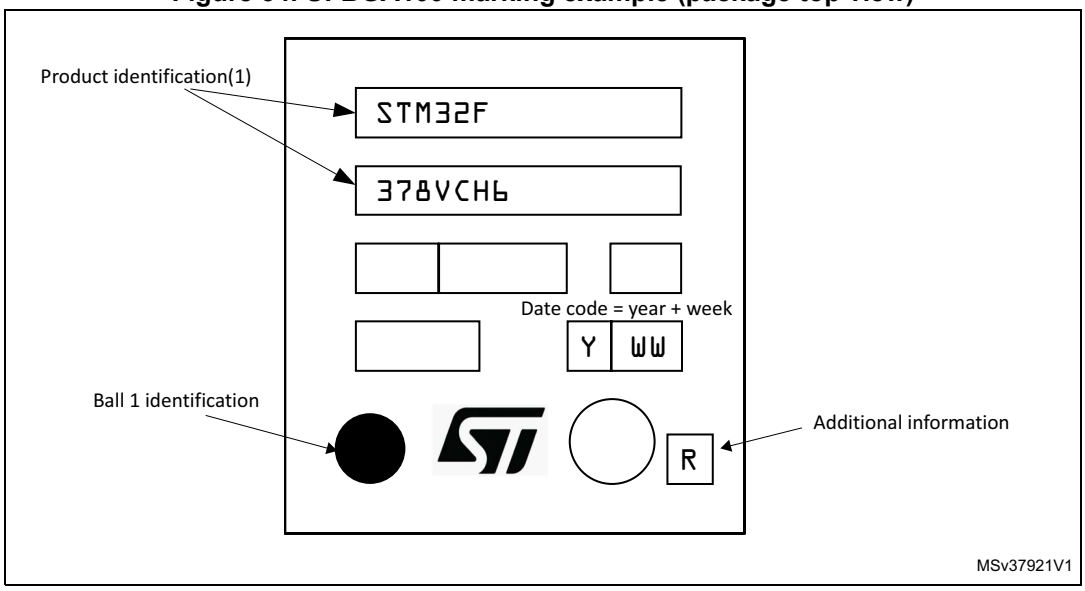
Table 69. WWDG min-max timeout value @72 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value
1	0	0.05687	3.6409
2	1	0.1137	7.2817
4	2	0.2275	14.564
8	3	0.4551	29.127

Device Marking for UFBGA100

The following figure gives an example of topside marking orientation versus ball 1 identifier location.

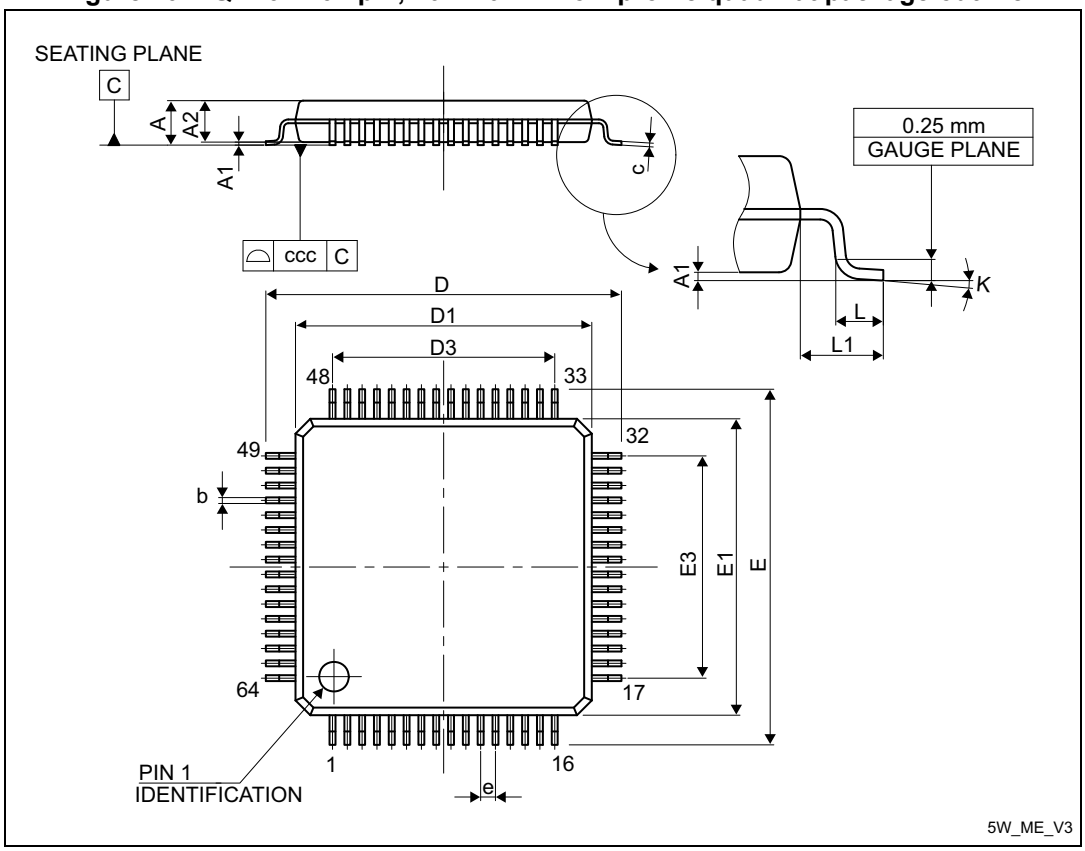
Figure 34. UFBGA100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.4 LQFP64 package information

Figure 40. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

7.6 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 22: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times Q_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Q_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = S\ (V_{OL} \times I_{OL}) + S((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 78. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	°C/W
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	55	
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient BGA100 - 7 x 7 mm	59	
	Thermal resistance junction-ambient WLCSP66 - 0.400 mm	53	

7.6.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.6.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Part numbering*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F378xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 1.8 V, maximum 3 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 2 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 1.8 V= 90 mW

P_{IOmax} = 3 × 8 mA × 0.4 V + 2 × 20 mA × 1.3 V = 61.6 mW

This gives: P_{INTmax} = 90 mW and P_{IOmax} = 61.6 mW:

P_{Dmax} = 90 + 61.6 = 151.6 mW

Thus: P_{Dmax} = 151.6 mW

Using the values obtained in *Table 78* T_{Jmax} is calculated as follows:

– For LQFP64, 45°C/W

T_{Jmax} = 82 °C + (45°C/W × 151.6 mW) = 82 °C + 6.8 °C = 88.8 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 8: Part numbering*).

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 115 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 1.8 V, maximum 9 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 1.8 V= 36 mW

P_{IOmax} = 9 × 8 mA × 0.4 V = 28.8 mW

This gives: P_{INTmax} = 36 mW and P_{IOmax} = 28.8 mW:

P_{Dmax} = 36+ 28.8 = 64.8 mW

Thus: P_{Dmax} = 64.8 mW

8 Part numbering

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 79. Ordering information scheme

Example: STM32 F 378 R C T 6 x

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Sub-family

378 = STM32F378xx

Pin count

C = 48 pins

R = 64/66 pins

V = 100 pins

Code size

C = 256 Kbytes of Flash memory

Package

T = LQFP

H = BGA

Y = WLCSP

Temperature range

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

Options

xxx = programmed parts

TR = tape and reel

Table 80. Document revision history (continued)

Date	Revision	Changes
10-Jun-2016	4	Updated: – *Table 3: Capacitive sensing GPIOs available on STM32F378xx devices* – *Table 19: Voltage characteristics* – *Table 25: Embedded internal reference voltage* – *Table 39: LSE oscillator characteristics (fLSE = 32.768 kHz)* – *Table 47: ESD absolute maximum ratings* – *Table 59: ADC characteristics* – *Table 62: DAC characteristics* – *Table 64: Temperature sensor calibration values* – *Table 70: SDADC characteristics* – *Table 78: Package thermal characteristics* – *Figure 18: TC and TTa I/O input characteristics* – *Figure 19: Five volt tolerant (FT and FTf) I/O input characteristics* Removed: – *Figure 19: TC and TTa I/O input characteristics - TTL port* – *Figure 21: Five volt tolerant (FT and FTf) I/O input characteristics - TTL port*