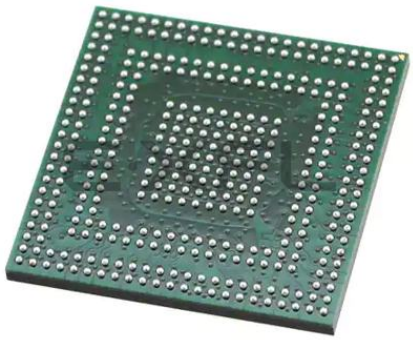


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Last Time Buy
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	Communications; QUICC Engine
RAM Controllers	DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	369-LFBGA
Supplier Device Package	369-PBGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8306scvmacdca

1 Overview

The MPC8306S incorporates the e300c3 (MPC603e-based) core built on Power Architecture® technology, which includes 16 Kbytes of each L1 instruction and data caches, dual integer units, and on-chip memory management units (MMUs). The MPC8306S also includes two DMA engines and a 16-bit DDR2 memory controller.

A new communications complex based on QUICC Engine technology forms the heart of the networking capability of the MPC8306S. The QUICC Engine block contains several peripheral controllers and a 32-bit RISC controller. Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs). A block diagram of the MPC8306S is shown in the following figure.

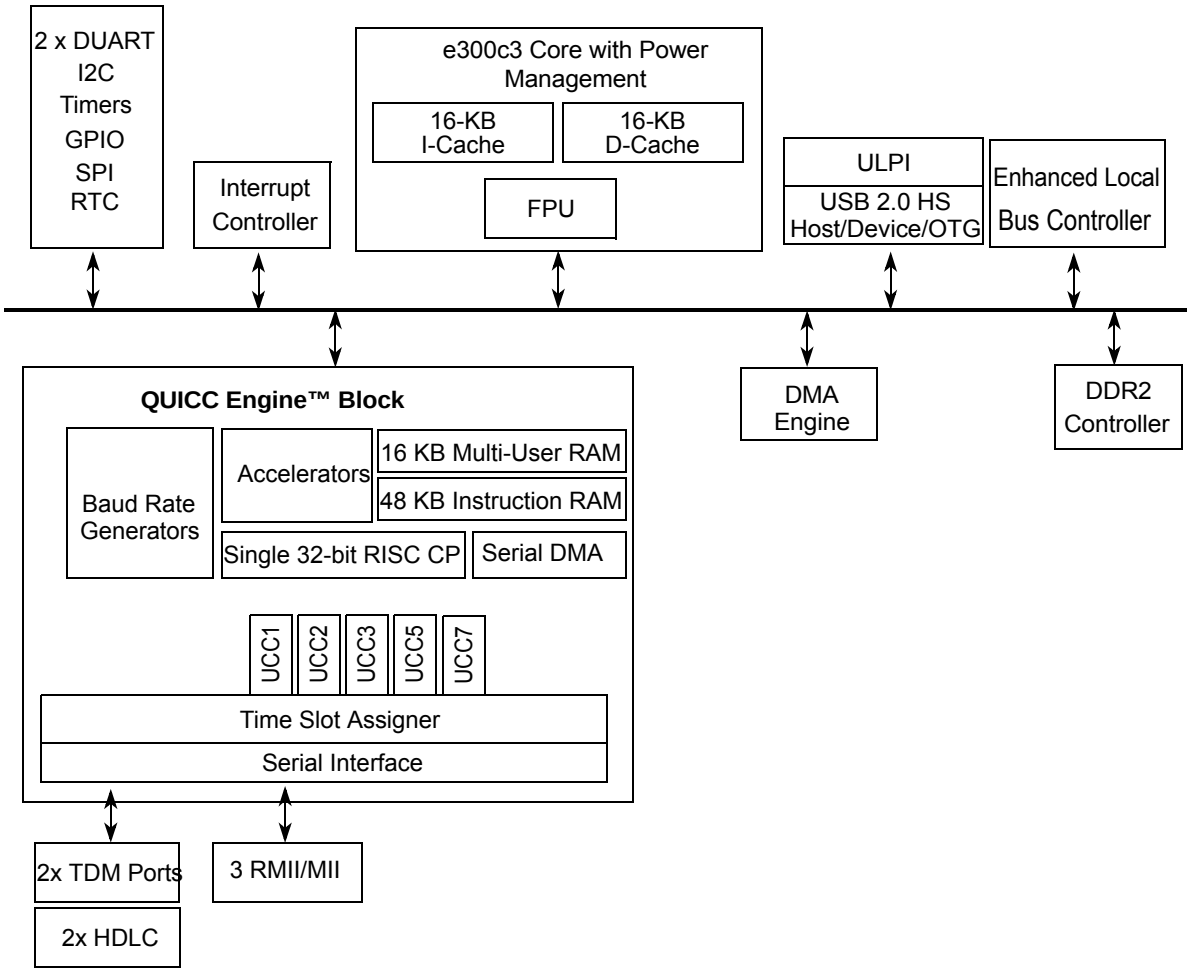


Figure 1. MPC8306S Block Diagram

Each of the five UCCs can support a variety of communication protocols such as 10/100 Mbps MII/RMII Ethernet, HDLC and TDM.

The following table provides the PLL lock times.

Table 10. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Note
PLL lock times	—	100	μs	—

5.1 Reset Signals DC Electrical Characteristics

The following table provides the DC electrical characteristics for the MPC8306S reset signals mentioned in Table 9.

Table 11. Reset Signals DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit	Note
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V	1
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V	1
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V	1
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V	1
Input low voltage	V_{IL}	—	–0.3	0.8	V	—
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	±5	μA	—

Note:
1. This specification applies when operating from 3.3 V supply.

6 DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR2 SDRAM interface of the MPC8306S. Note that DDR2 SDRAM is GV_{DD}(typ) = 1.8 V.

6.1 DDR2 SDRAM DC Electrical Characteristics

The following table provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8306S when GV_{DD}(typ) = 1.8 V.

Table 12. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	1.7	1.9	V	1
I/O reference voltage	MVREF	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MVREF – 0.04	MVREF + 0.04	V	3
Input high voltage	V_{IH}	MVREF+ 0.125	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MVREF – 0.125	V	—
Output leakage current	I_{OZ}	–9.9	9.9	μA	4

Table 12. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Note
Output high current (V_{OUT} = 1.35 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MVREF is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MVREF may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREF. This rail should track variations in the DC level of MVREF.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

The following table provides the DDR2 capacitance when GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM Capacitance for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.100 V, f = 1 MHz, T_A = 25 °C, V_{OUT} = GV_{DD} ÷ 2, V_{OUT} (peak-to-peak) = 0.2 V.

6.2 DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR2 SDRAM interface.

6.2.1 DDR2 SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR2 SDRAM (GV_{DD}(typ) = 1.8 V).

Table 14. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of 1.8 V± 100mV.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{IL}	—	MVREF – 0.25	V	—
AC input high voltage	V_{IH}	MVREF + 0.25	—	V	—

The following table provides the input AC timing specifications for the DDR2 SDRAM interface.

Table 15. DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.8V ± 100mV.

Parameter	Symbol	Min	Max	Unit	Note
Controller skew for MDQS—MDQ/MDM	t_{CISKEW}			ps	1, 2

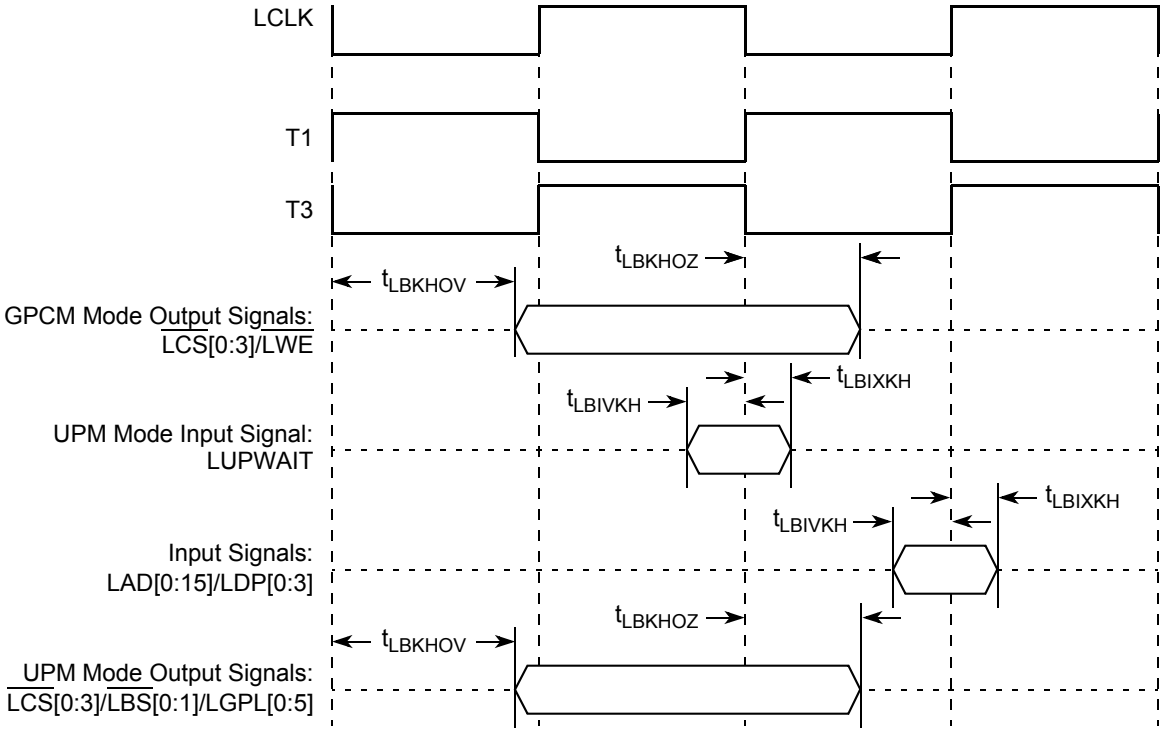


Figure 9. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2

The following figure shows the RMII transmit AC timing diagram.

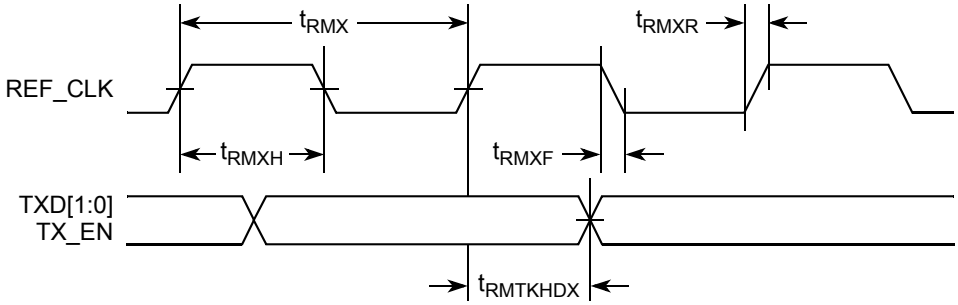


Figure 15. RMII Transmit AC Timing Diagram

8.2.2.2 RMII Receive AC Timing Specifications

The following table provides the RMII receive AC timing specifications.

Table 23. RMII Receive AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

12 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8306S.

12.1 DUART DC Electrical Characteristics

The following table provides the DC electrical characteristics for the DUART interface of the MPC8306S.

Table 32. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage OV_{DD}	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V
Input current (0 V ≤ V_{IN} ≤ OV_{DD})[1]	I_{IN}	—	±5	μA

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

12.2 DUART AC Electrical Specifications

The following table provides the AC timing parameters for the DUART interface of the MPC8306S.

Table 33. DUART AC Timing Specifications

Parameter	Value	Unit	Note
Minimum baud rate	256	baud	—
Maximum baud rate	>1,000,000	baud	1
Oversample rate	16	—	2

Notes:
1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

13 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8306S.

13.1 I²C DC Electrical Characteristics

The following table provides the DC electrical characteristics for the I²C interface of the MPC8306S.

Table 34. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 300mV.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	0.4	V	1
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	—
Input current ($0 V \le V_{IN} \le OV_{DD}$)	I_{IN}	—	±5	μA	4

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. Refer to the *MPC8306S PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for information on the digital filter used.
4. I/O pins obstructs the SDA and SCL lines if OV_{DD} is switched off.

13.2 I²C AC Electrical Specifications

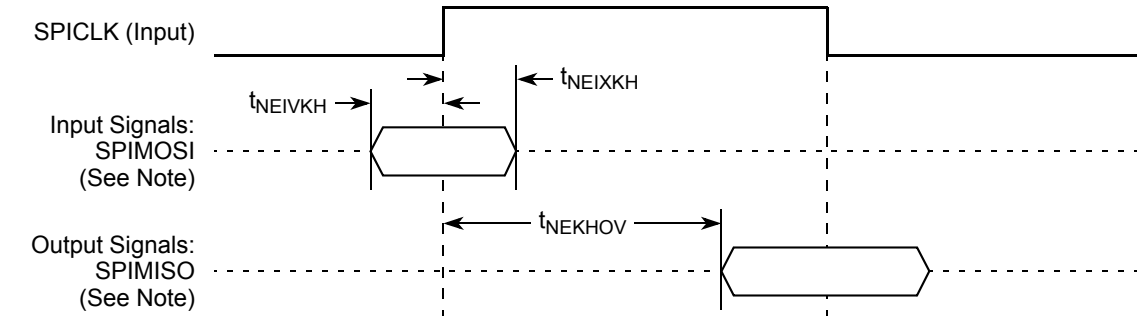
The following table provides the AC timing parameters for the I²C interface of the MPC8306S.

Table 35. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 34).

Parameter	Symbol[1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	ns
Data hold time: I²C bus devices	t_{I2DXKL}	300	0.9[3]	μs
Rise time of both SDA and SCL signals	t_{I2CR}	$20 + 0.1\ C_B$[4]	300	ns

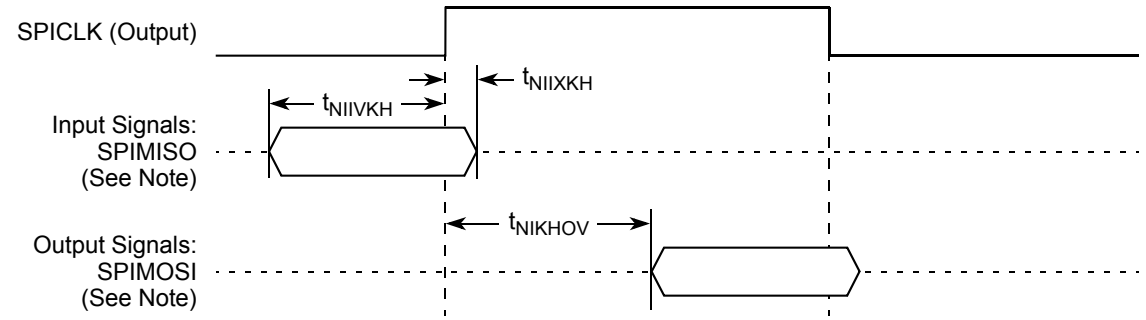
The following figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 30. SPI AC Timing in Slave Mode (External Clock) Diagram

The following figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 31. SPI AC Timing in Master Mode (Internal Clock) Diagram

18 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1™ (JTAG) interface of the MPC8306S.

18.1 JTAG DC Electrical Characteristics

The following table provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8306S.

Table 44. JTAG Interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Table 44. JTAG Interface DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	±5	μA

18.2 JTAG AC Electrical Characteristics

This section describes the AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8306S. The following table provides the JTAG AC timing specifications as defined in Figure 33 through Figure 36.

Table 45. JTAG AC Timing Specifications (Independent of SYS_CLK_IN)[1]

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	11	—	ns	—
JTAG external clock rise and fall times	t_{JTGR}, t_{JTGF}	0	2	ns	—
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 15 15	ns	5

Table 46. MPC8306S Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MEMC_MA[8]	T1	O	GV_{DD}	—
MEMC_MA[9]	P4	O	GV_{DD}	—
MEMC_MA[10]	L4	O	GV_{DD}	—
MEMC_MA[11]	T2	O	GV_{DD}	—
MEMC_MA[12]	U1	O	GV_{DD}	—
MEMC_MA[13]	U2	O	GV_{DD}	—
MEMC_MWE_B	K1	O	GV_{DD}	—
MEMC_MRAS_B	K2	O	GV_{DD}	—
MEMC_MCAS_B	J1	O	GV_{DD}	—
MEMC_MCS_B[0]	J4	O	GV_{DD}	—
MEMC_MCS_B[1]	H1	O	GV_{DD}	—
MEMC_MCKE[0]	U4	O	GV_{DD}	—
MEMC_MCK[0]	V1	O	GV_{DD}	—
MEMC_MCK_B[0]	W1	O	GV_{DD}	—
MEMC_MODT[0]	H2	O	GV_{DD}	—
MEMC_MODT[1]	H4	O	GV_{DD}	—
MEMC_MVREF	L8		GV_{DD}	—
Local Bus Controller Interface				
LAD[0]	B7	IO	OV_{DD}	—
LAD[1]	D9	IO	OV_{DD}	—
LAD[2]	A6	IO	OV_{DD}	—
LAD[3]	B8	IO	OV_{DD}	—
LAD[4]	A7	IO	OV_{DD}	—
LAD[5]	A8	IO	OV_{DD}	—
LAD[6]	A9	IO	OV_{DD}	—
LAD[7]	D10	IO	OV_{DD}	—
LAD[8]	B10	IO	OV_{DD}	—
LAD[9]	A10	IO	OV_{DD}	—
LAD[10]	B11	IO	OV_{DD}	—
LAD[11]	D12	IO	OV_{DD}	—
LAD[12]	D11	IO	OV_{DD}	—
LAD[13]	A11	IO	OV_{DD}	—
LAD[14]	A12	IO	OV_{DD}	—
LAD[15]	B13	IO	OV_{DD}	—
LA[16]	A13	IO	OV_{DD}	—

Table 46. MPC8306S Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Clock Interface				
QE_CLK_IN	P23	I	OV_{DD}	—
SYS_CLK_IN	R23	I	OV_{DD}	—
RTC_PIT_CLOCK	V23	I	OV_{DD}	—
Miscellaneous Signals				
QUIESCE_B	A2	O	OV_{DD}	—
THERM0	D6	I	OV_{DD}	—
GPIO				
GPIO[0]/MSRCID0 (DDR ID)	E5	IO	OV_{DD}	—
GPIO[1]/MSRCID1 (DDR ID)	E6	IO	OV_{DD}	—
GPIO[2]/MSRCID2 (DDR ID)	D4	IO	OV_{DD}	—
GPIO[3]/MSRCID3 (DDR ID)	C2	IO	OV_{DD}	—
GPIO[4]/MSRCID4 (DDR ID)	C1	IO	OV_{DD}	—
GPIO[5]/MDVAL (DDR ID)	B1	IO	OV_{DD}	—
GPIO[6]/QE_EXT_REQ_3	B3	IO	OV_{DD}	—
GPIO[7]/QE_EXT_REQ_1	B2	IO	OV_{DD}	—
USB				
USBDR_PWRFAULT/IIC_SDA2/CE_PIO_1	AC4	IO	OV_{DD}	2
USBDR_CLK/UART2_SIN[2]/UART2_CTS_B[1]	Y9	I	OV_{DD}	
USBDR_DIR/IIC_SCL2	AC3	IO	OV_{DD}	2
USBDR_NXT/UART2_SIN[1]/QE_EXT_REQ_4	AC2	IO	OV_{DD}	—
USBDR_PCTL[0]/UART2_SOUT[1]/ LB_POR_CFG_BOOT_ECC	AB3	IO	OV_{DD}	—
USBDR_PCTL[1]/UART2_SOUT[2]/ UART2_RTS_B1/LB_POR_BOOT_ERR	Y8	O	OV_{DD}	—
USBDR_STP/QE_EXT_REQ_2	W6	IO	OV_{DD}	—
USBDR_TXDRXD[0]/UART1_SOUT[1]/ GPIO[32]/QE_TRB_O	AB7	IO	OV_{DD}	—
USBDR_TXDRXD[1]/UART1_SIN[1]/GPIO[33]/ QE_TRB_I	AB8	IO	OV_{DD}	—
USBDR_TXDRXD[2]/UART1_SOUT[2]/ UART1_RTS_B1/QE_BRG[1]	AC6	IO	OV_{DD}	—
USBDR_TXDRXD[3]/UART1_SIN[2]/ UART1_CTS_B1/QE_BRG[2]	AC5	IO	OV_{DD}	—
USBDR_TXDRXD[4]/GPIO[34]/QE_BRG[3]	AB5	IO	OV_{DD}	—
USBDR_TXDRXD[5]/GPIO[35]/QE_BRG[4]	Y7	IO	OV_{DD}	—
USBDR_TXDRXD[6]/GPIO[36]/QE_BRG[9]	Y6	IO	OV_{DD}	—

Table 46. MPC8306S Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
USBDR_TXDRXD[7]/GPIO[37]/QE_BRG[11]	Y5	IO	OV_{DD}	—
DUART				
UART1_SOUT[1]/LSRCID4/LCS_B[4]	C23	O	OV_{DD}	—
UART1_SIN[1]/LDVAL/LCS_B[5]	F19	IO	OV_{DD}	—
UART1_SOUT[2]/UART1_RTS_B1/LCS_B[6]	D23	O	OV_{DD}	—
UART1_SIN[2]/UART1_CTS_B[1]/LCS_B[7]	D22	IO	OV_{DD}	—
Interrupts				
IRQ_B0_MCP_IN_B/CE_PI_0	E20	IO	OV_{DD}	—
IRQ_B1/MCP_OUT_B	E23	IO	OV_{DD}	—
IRQ_B2/CKSTOP_OUT_B	E22	IO	OV_{DD}	—
IRQ_B3/CKSTOP_IN_B	F20	I	OV_{DD}	—
I2C / SPI				
IIC_SDA1	G20	IO	OV_{DD}	2
IIC_SCL1	J20	IO	OV_{DD}	2
LCLK1/IIC_SCL2/CKSTOP_IN_B	H20	IO	OV_{DD}	2
SPISEL_BOOT/IIC_SDA2/CKSTOP_OUT_B	F23	O	OV_{DD}	2
SPIMOSI/LSRCID[2]	G22	IO	OV_{DD}	—
SPIMISO/LSRCID[3]	K20	IO	OV_{DD}	—
SPICLK/LSRCID[0]	G23	IO	OV_{DD}	—
SPISEL/LSRCID[1]	H22	I	OV_{DD}	—
FEC Management				
FEC_MDC	H23	O	OV_{DD}	—
FEC_MDIO	L20	IO	OV_{DD}	—
FEC1/GTM/GPIO				
FEC1_COL/GTM1_TIN[1]/GPIO[16]	AB20	IO	OV_{DD}	—
FEC1_CRS/GTM1_TGATE1_B/GPIO[17]	AC21	IO	OV_{DD}	—
FEC1_RX_CLK/GPIO[18]	Y17	IO	OV_{DD}	—
FEC1_RX_DV/GTM1_TIN[2]/GPIO[19]	Y18	IO	OV_{DD}	—
FEC1_RX_ER/GTM1_TGATE[2]_B/GPIO[20]	AB19	IO	OV_{DD}	—
FEC1_RXD0/GPIO[21]	AC20	IO	OV_{DD}	—
FEC1_RXD1/GTM1_TIN[3]/GPIO[22]	AC19	IO	OV_{DD}	—
FEC1_RXD2/GTM1_TGATE[3]_B/GPIO[23]	AC18	IO	OV_{DD}	—
FEC1_RXD3/GPIO[24]	AB17	IO	OV_{DD}	—
FEC1_TX_CLK/GTM1_TIN4/GPIO[25]	Y15	IO	OV_{DD}	—
FEC1_TX_EN/GTM1_TGATE[4]_B/GPIO[26]	Y16	IO	OV_{DD}	—

Table 46. MPC8306S Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
FEC3_TXD0/TSEC_TMR_PP2/GPIO[60]	R20	IO	OV_{DD}	—
FEC3_TXD1/TSEC_TMR_PP3/GPIO[61]	T22	IO	OV_{DD}	—
FEC3_TXD2/TSEC_TMR_ALARM1/GPIO[62]	T23	IO	OV_{DD}	—
FEC3_TXD3/TSEC_TMR_ALARM2/GPIO[63]	T20	IO	OV_{DD}	—
HDLC/GPIO/TDM				
HDLC1_RXCLK/TDM1_RCK/GPIO[1]	U23	IO	OV_{DD}	—
HDLC1_RXD/TDM1_RD/GPIO[3]	U22	IO	OV_{DD}	—
HDLC1_TXCLK/GPIO[0]/TDM1_TCK/ QE_BRG[5]	AC22	IO	OV_{DD}	—
HDLC1_TXD/GPIO[2]/TDM1_TD/ CFG_RESET_SOURCE[0]	W18	IO	OV_{DD}	—
HDLC1_CD_B/GPIO[4]/TDM1_TFS	W19	IO	OV_{DD}	—
HDLC1_CTS_B/GPIO[5]/TDM1_RFS	Y20	IO	OV_{DD}	—
HDLC1_RTS_B/GPIO[6]/TDM1_STROBE_B/ CFG_RESET_SOURCE[1]	AB22	IO	OV_{DD}	—
HDLC2_TXCLK/GPIO[16]/TDM2_TCK/ QE_BRG[7]	AB23	IO	OV_{DD}	—
HDLC2_RXCLK/GPIO[17]/TDM2_RCK/ QE_BRG[8]	AA23	IO	OV_{DD}	—
HDLC2_TXD/GPIO[18]/TDM2_TD/ CFG_RESET_SOURCE[2]	W20	IO	OV_{DD}	—
HDLC2_RXD/GPIO[19]/TDM2_RD	Y23	IO	OV_{DD}	—
HDLC2_CD_B/GPIO[20]/TDM2_TFS	Y22	IO	OV_{DD}	—
HDLC2_CTS_B/GPIO[21]/TDM2_RFS	W23	IO	OV_{DD}	—
HDLC2_RTS_B/GPIO[22]/TDM2_STROBE_B/ CFG_RESET_SOURCE[3]	W22	IO	OV_{DD}	—
Power				
AV_{DD1}	L16	—	—	—
AV_{DD2}	M16	—	—	—
AV_{DD3}	N8	—	—	—
GV_{DD}	G5, H5, J5, K5, L5, M5, N5, P5, R5, T5, U5	—	—	—
OV_{DD}	E7,E8,E9,E10,E11,E12, E13,E14, E15, E16,E17,G19,H19,J19,K 19,L19,M19, N19,P19,R19,T19,U19, W7,W8,W9, W10,W11, W12,W13, W14,W15, W16, W17	—	—	—

Table 46. MPC8306S Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
V_{DD}	H8,H9,H10,H11,H12,H13,H14,H15,H16,J8,J16,K8,K16,M8,N16,P8,P16,R8,R16,T8,T9,T10,T11,T12,T13,T14,T15,T16	—	—	—
VSS	A1,B4,B6,B9,B12,B15,B18,B21,C22,D2,D5,D18,D20,F2,F22,J2,J9,J10,J11,J12,J13,J14,J15,J22,K4,K9,K10,K11,K12,K13,K14,K15,L9,L10,L11,L12,L13,L14,L15,M2,M9,M10,M11,M12,M13,M14,M15,M22,N9,N10,N11,N12,N13,N14,N15,P9,P10,P11,P12,P13,P14,P15,R2,R9,R10,R11,R12,R13,R14,R15,R22,T4,V2,V19,V22,W4,Y19,AA2,AA22,AB4,AB6,AB9,AB12,AB15,AB18,AB21,AC1,AC23	—	—	—
NC	A23	—	—	—

Notes
1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OV_{DD}
2. This pin is an open drain signal. A weak pull-up resistor (2-10 kΩ) should be placed on this pin to OV_{DD}
3. This pin has weak pull-up that is always enabled.

Table 49. System PLL Multiplication Factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111–1111	Reserved

coherent system bus clock (*csb_clk*). The following table shows the expected frequency values for the CSB frequency for selected *csb_clk* to *SYS_CLK_IN* ratios.

Table 50. CSB Frequency Options

SPMF	csb_clk : sys_clk_in Ratio	SYS_CLK_IN(MHz)		
		25	33.33	66.67
		csb_clk Frequency (MHz)		
0010	2:1			133
0011	3:1			
0100	4:1		133	
0101	5:1	125	167	
0110	6:1			

20.3 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). The following table shows the encodings for RCWL[COREPLL]. COREPLL values not listed, and should be considered reserved.

Table 51. e300 Core PLL Configuration

RCWL[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO Divider
0-1	2-5	6		
nn	0000	n	PLL bypassed (PLL off, *csb_clk* clocks core directly)	PLL bypassed (PLL off, *csb_clk* clocks core directly)
00	0001	0	1:1	÷2
01	0001	0	1:1	÷4
10	0001	0	1:1	÷8
11	0001	0	1:1	÷8

Table 54. Suggested PLL Configurations

Conf No.	SPMF	Core PLL	CEPMF	CEDF	Input Clock Frequency (MHz)	CSB Frequency (MHz)	Core Frequency (MHz)	QUICC Engine Frequency (MHz)
1	0100	0000100	0111	0	33.33	133.33	266.66	233
2	0010	0000100	0111	1	66.67	133.33	266.66	233
3	0100	0000101	0111	0	33.33	133.33	333.33	233
4	0101	0000101	1001	0	25	125	312.5	225
5	0010	0000101	0111	1	66.67	133.33	333.33	233

22.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins. The voltage level at each $AV_{DD}n$ pin should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits as illustrated in Figure 41, one to each of the three AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

The following figure shows the PLL power supply filter circuit.

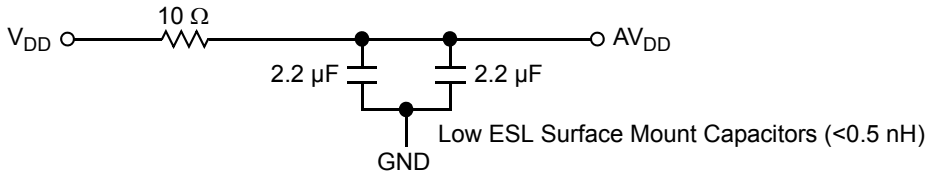


Figure 41. PLL Power Supply Filter Circuit

22.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the MPC8306S can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8306S system, and MPC8306S itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, and GV_{DD} pins of the MPC8306S. These decoupling capacitors should receive their power from separate V_{DD}, OV_{DD}, GV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, OV_{DD}, and GV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias

to minimize inductance. Suggested bulk capacitors—100 to 330 µF (AVX TPS tantalum or Sanyo OSCON).

22.4 Output Buffer DC Impedance

For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 42). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

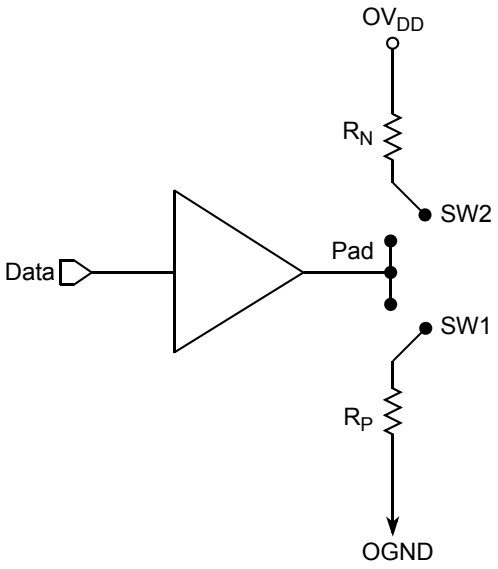


Figure 42. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

Table 57. Part Numbering Nomenclature

MPC	*nnnn*	*C*	*VM*	*AF*	*D*	*C*	*A*
Product Code	**Part Identifier**	**Temperature Range[1]**	**Package[2]**	**e300 Core Frequency[3]**	**DDR2 Frequency**	**QUICC Engine Frequency**	**Revision Level**
MPC	8306S	Blank = 0 to 105°C C = –40 to 105°C	VM = Pb-free	AB = 133MHz AC = 200 MHz AD = 266 MHz AF = 333 MHz	D = 266 MHz F = 333 MHz	C = 233 MHz	Contact local Freescale sales office

Notes:
1. Contact local Freescale office on availability of parts with C temperature range.
2. See Section 19, “Package and Pin Listings,” for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.

23.2 Part Marking

Parts are marked as in the example shown in the following figure.

MAPBGA

Notes:
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.

Figure 43. Freescale Part Marking for MAPBGA Devices

The following table shows the SVR Settings.

Table 58. SVR Settings

Device	Package	SVR (Rev 1.0)	SVR (Rev 1.1)
MPC8306S	MAPBGA	0x8110_0210	0x8110_0211
Note: PVR = 0x8085_0020			

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or
+1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

Document Number: MPC8306SEC
Rev. 1
09/2011

freescale™