**Welcome to E-XFL.COM**

## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PowerPC e300c3 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 333MHz |
| Co-Processors/DSP | Communications; QUICC Engine |
| RAM Controllers | DDR2 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100Mbps (3) |
| SATA | - |
| USB | USB 2.0 (1) |
| Voltage - I/O | 1.8V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 369-LFBGA |
| Supplier Device Package | 369-PBGA (19x19) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8306svmafdca |

In summary, the MPC8306S provides users with a highly integrated, fully programmable communications processor. This helps to ensure that a low-cost system solution can be quickly developed and offers flexibility to accommodate new standards and evolving system requirements.

## 1.1 Features

The major features of the device are as follows:

- e300c3 Power Architecture processor core
  - Enhanced version of the MPC603e core
  - High-performance, superscalar processor core with a four-stage pipeline and low interrupt latency times
  - Floating-point, dual integer units, load/store, system register, and branch processing units
  - 16-Kbyte instruction cache and 16-Kbyte data cache with lockable capabilities
  - Dynamic power management
  - Enhanced hardware program debug features
  - Software-compatible with Freescale processor families implementing Power Architecture technology
  - Separate PLL that is clocked by the system bus clock
  - Performance monitor
- QUICC Engine block
  - 32-bit RISC controller for flexible support of the communications peripherals with the following features:
    - One clock per instruction
    - Separate PLL for operating frequency that is independent of system's bus and e300 core frequency for power and performance optimization
    - 32-bit instruction object code
    - Executes code from internal IRAM
    - 32-bit arithmetic logic unit (ALU) data path
    - Modular architecture allowing for easy functional enhancements
    - Slave bus for CPU access of registers and multiuser RAM space
    - 48 Kbytes of instruction RAM
    - 16 Kbytes of multiuser data RAM
    - Serial DMA channel for receive and transmit on all serial channels
  - Five unified communication controllers (UCCs) supporting the following protocols and interfaces:
    - 10/100 Mbps Ethernet/IEEE Std. 802.3® through MII and RMII interfaces.
    - HDLC/Transparent (bit rate up to QUICC Engine operating frequency / 8)
    - HDLC Bus (bit rate up to 10 Mbps)
    - Asynchronous HDLC (bit rate up to 2 Mbps)

The following table shows the estimated typical I/O power dissipation for the device.

**Table 6. Typical I/O Power Dissipation**

| Interface | Parameter | $GV_{DD}$ (1.8 V) | $OV_{DD}$ (3.3 V) | Unit | Comments |
|---|---|---|---|---|---|
| DDR I/O<br>65% utilization<br>1.8 V<br>$R_s$ = 20 Ω<br>$R_t$ = 50 Ω<br>1 pair of clocks | 266 MHz, 1 × 16 bits | 0.141 | — | W | — |
| Local bus I/O load = 25 pF<br>1 pair of clocks | 66 MHz, 26 bits | — | 0.150 | W | 1 |
| QUICC Engine block and other I/Os | TDM serial, HDLC/TRAN serial, DUART, MII, RMII, Ethernet management, USB, SPI, Timer output, | | | | |

**Note:**
1. Typical I/O power is based on a nominal voltage of $V_{DD}$ = 3.3V, ambient temperature, and the core running a Dhrystone benchmark application. The measurements were taken on the evaluation board using WC process silicon.

# 4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8306S.

**NOTE**

The rise/fall time on QUICC Engine input pins should not exceed 5 ns. This should be enforced especially on clock signals. Rise time refers to signal transitions from 10% to 90% of $OV_{DD}$; fall time refers to transitions from 90% to 10% of $OV_{DD}$.

## 4.1 DC Electrical Characteristics

The following table provides the clock input (SYS_CLK_IN) DC specifications for the MPC8306S. These specifications are also applicable for QE_CLK_IN.

**Table 7. SYS_CLK_IN DC Electrical Characteristics**

| Parameter | Condition | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | — | $V_{IH}$ | 2.4 | $OV_{DD}$ + 0.3 | V |
| Input low voltage | — | $V_{IL}$ | –0.3 | 0.4 | V |
| SYS_CLK_IN input current | 0 V ≤ $V_{IN}$ ≤ $OV_{DD}$ | $I_{IN}$ | — | ±5 | μA |
| SYS_CLK_IN input current | 0 V ≤ $V_{IN}$ ≤ 0.5 V or<br>$OV_{DD}$ – 0.5 V ≤ $V_{IN}$ ≤ $OV_{DD}$ | $I_{IN}$ | — | ±5 | μA |
| SYS_CLK_IN input current | 0.5 V ≤ $V_{IN}$ ≤ $OV_{DD}$ – 0.5 V | $I_{IN}$ | — | ±50 | μA |

The following table provides the PLL lock times.

**Table 10. PLL Lock Times**

| Parameter/Condition | Min | Max | Unit | Note |
|---|---|---|---|---|
| PLL lock times | — | 100 | μs | — |

## 5.1 Reset Signals DC Electrical Characteristics

The following table provides the DC electrical characteristics for the MPC8306S reset signals mentioned in Table 9.

**Table 11. Reset Signals DC Electrical Characteristics**

| Characteristic | Symbol | Condition | Min | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –6.0 mA | 2.4 | — | V | 1 |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 6.0 mA | — | 0.5 | V | 1 |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.4 | V | 1 |
| Input high voltage | $V_{IH}$ | — | 2.0 | $OV_{DD}$ + 0.3 | V | 1 |
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V | — |
| Input current | $I_{IN}$ | 0 V ≤ $V_{IN}$ ≤ $OV_{DD}$ | — | ±5 | μA | — |

**Note:**
1. This specification applies when operating from 3.3 V supply.

# 6 DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR2 SDRAM interface of the MPC8306S. Note that DDR2 SDRAM is $GV_{DD}$(typ) = 1.8 V.

## 6.1 DDR2 SDRAM DC Electrical Characteristics

The following table provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8306S when $GV_{DD}$(typ) = 1.8 V.

**Table 12. DDR2 SDRAM DC Electrical Characteristics for $GV_{DD}$(typ) = 1.8 V**

| Parameter/Condition | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| I/O supply voltage | $GV_{DD}$ | 1.7 | 1.9 | V | 1 |
| I/O reference voltage | MVREF | 0.49 × $GV_{DD}$ | 0.51 × $GV_{DD}$ | V | 2 |
| I/O termination voltage | $V_{TT}$ | MVREF – 0.04 | MVREF + 0.04 | V | 3 |
| Input high voltage | $V_{IH}$ | MVREF+ 0.125 | $GV_{DD}$ + 0.3 | V | — |
| Input low voltage | $V_{IL}$ | –0.3 | MVREF – 0.125 | V | — |
| Output leakage current | $I_{OZ}$ | –9.9 | 9.9 | μA | 4 |

**Table 15. DDR2 SDRAM Input AC Timing Specifications (continued)**

At recommended operating conditions with $GV_{DD}$ of 1.8V ± 100mV.

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| 266 MHz | | –750 | 750 | | |

**Notes:**

1. $t_{CISKEW}$ represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called $t_{DISKEW}$. This can be determined by the equation: $t_{DISKEW} = \pm(T/4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of $t_{CISKEW}$.

The following figure shows the input timing diagram for the DDR controller.

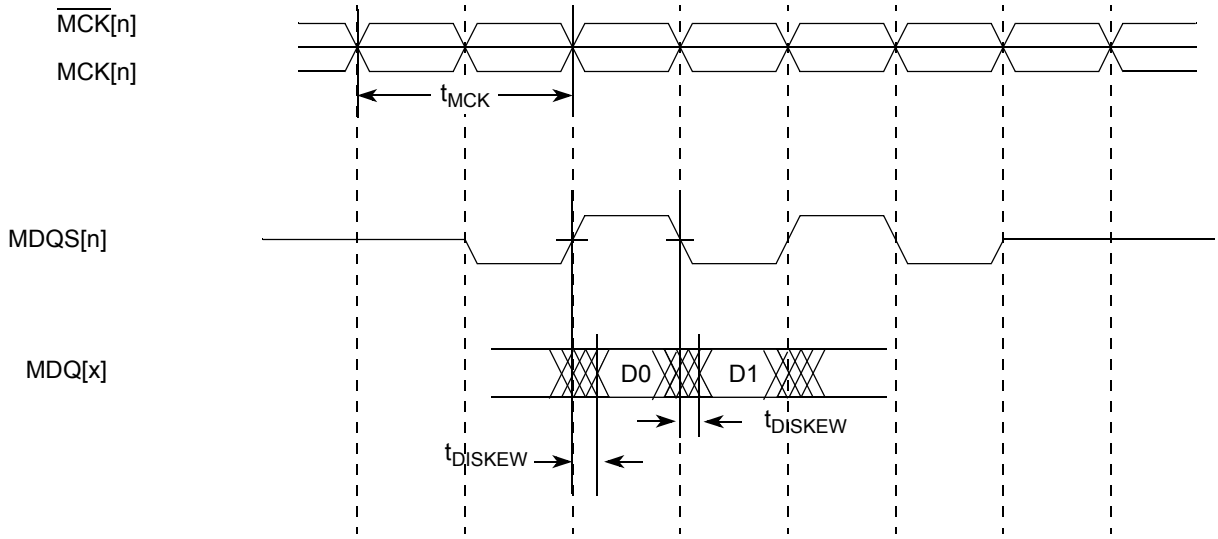



**Figure 4. DDR Input Timing Diagram**

## 6.2.2 DDR2 SDRAM Output AC Timing Specifications

The following table provides the output AC timing specifications for the DDR2 SDRAM interfaces.

**Table 16. DDR2 SDRAM Output AC Timing Specifications**

At recommended operating conditions with $GV_{DD}$ of 1.8V ± 100mV.

| Parameter | Symbol[1] | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| MCK cycle time, (MCK/$\overline{\text{MCK}}$ crossing) | $t_{MCK}$ | 5.988 | 8 | ns | 2 |
| ADDR/CMD output setup with respect to MCK<br>266 MHz | $t_{DDKHAS}$ | <br>2.5 | <br>— | ns | 3 |
| ADDR/CMD output hold with respect to MCK<br>266 MHz | $t_{DDKHAX}$ | <br>2.5 | <br>— | ns | 3 |
| $\overline{\text{MCS}}$ output setup with respect to MCK<br>266 MHz | $t_{DDKHCS}$ | <br>2.5 | <br>— | ns | 3 |

The following figure provides the AC test load for the local bus.

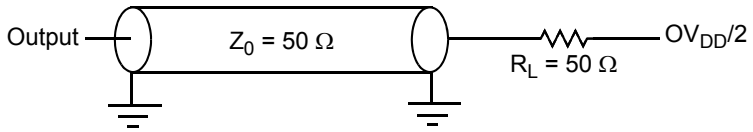



**Figure 7. Local Bus AC Test Load**

The following figures show the local bus signals. These figures has been given indicate timing parameters only and do not reflect actual functional operation of interface.

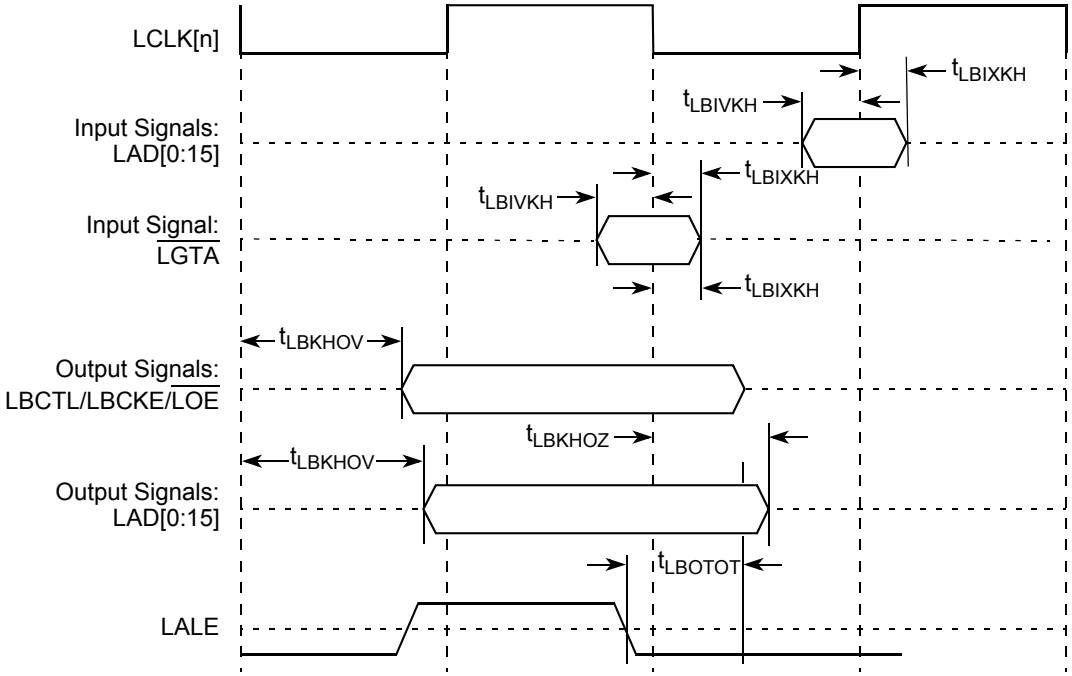



**Figure 8. Local Bus Signals**

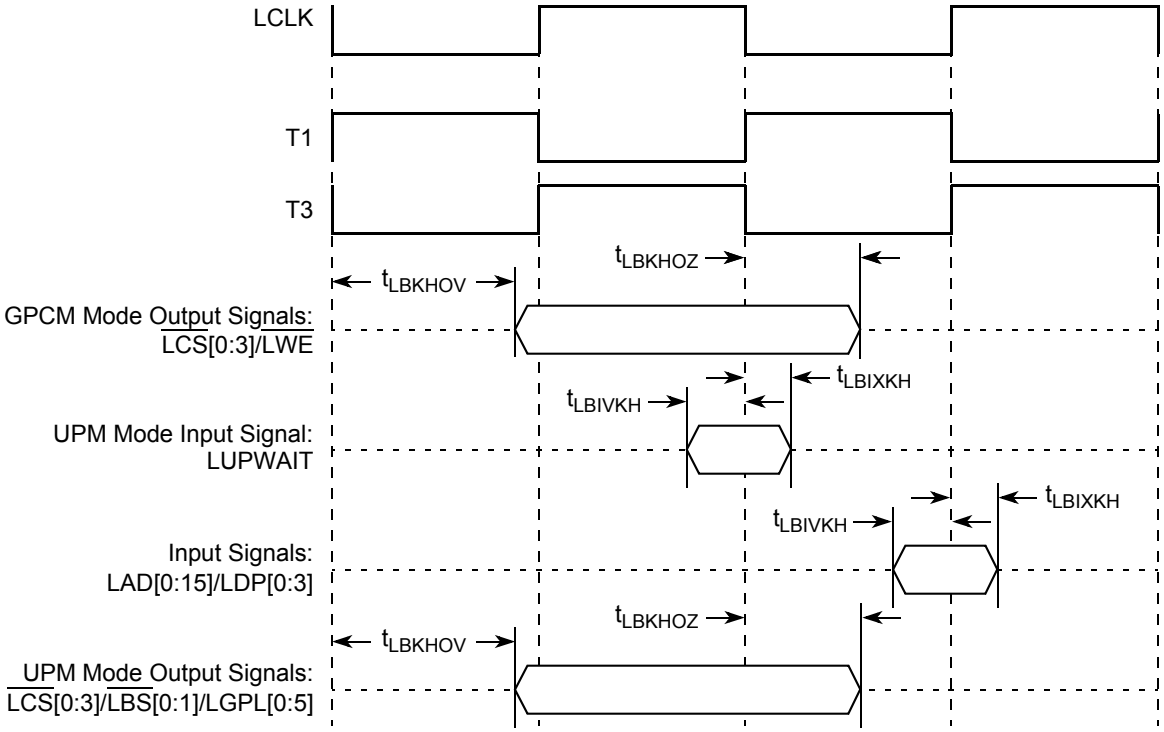



**Figure 9. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2**

The following figure provides the AC test load.

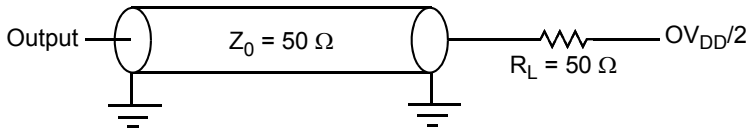



**Figure 11. AC Test Load**

The following figure shows the MII transmit AC timing diagram.

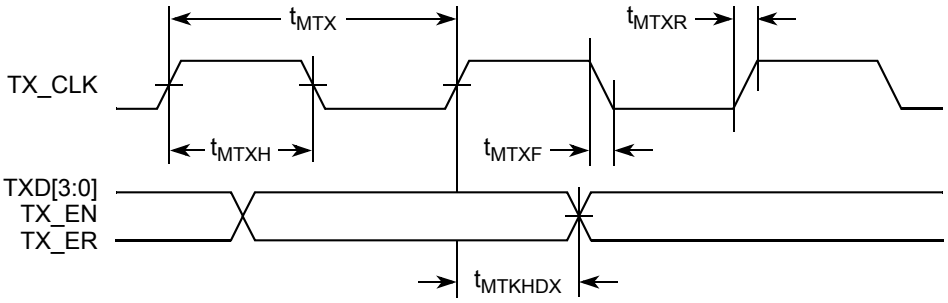



**Figure 12. MII Transmit AC Timing Diagram**

## 8.2.1.2 MII Receive AC Timing Specifications

The following table provides the MII receive AC timing specifications.

**Table 21. MII Receive AC Timing Specifications**

At recommended operating conditions with $OV_{DD}$ of 3.3 V ± 300mV.

| Parameter/Condition | Symbol[1] | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period 10 Mbps | $t_{MRX}$ | — | 400 | — | ns |
| RX_CLK clock period 100 Mbps | $t_{MRX}$ | — | 40 | — | ns |
| RX_CLK duty cycle | $t_{MRXH}/t_{MRX}$ | 35 | — | 65 | % |
| RXD[3:0], RX_DV, RX_ER setup time to RX_CLK | $t_{MRDVKH}$ | 10.0 | — | — | ns |
| RXD[3:0], RX_DV, RX_ER hold time to RX_CLK | $t_{MRDXKH}$ | 10.0 | — | — | ns |
| RX_CLK clock rise $V_{IL}$(min) to $V_{IH}$(max) | $t_{MRXR}$ | 1.0 | — | 4.0 | ns |
| RX_CLK clock fall time $V_{IH}$(max) to $V_{IL}$(min) | $t_{MRXF}$ | 1.0 | — | 4.0 | ns |

**Note:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MRDVKH}$ symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MRX}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{MRDXKL}$ symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{MRX}$ clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{MRX}$ represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure shows the MII receive AC timing diagram.

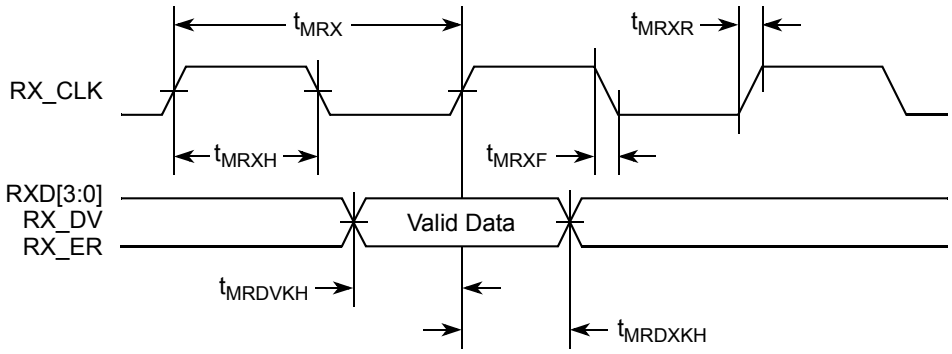



**Figure 13. MII Receive AC Timing Diagram**

## 8.2.2 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

### 8.2.2.1 RMII Transmit AC Timing Specifications

The following table provides the RMII transmit AC timing specifications.

**Table 22. RMII Transmit AC Timing Specifications**

At recommended operating conditions with $OV_{DD}$ of 3.3 V ± 300mV.

| Parameter/Condition | Symbol[1] | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| REF_CLK clock | $t_{RMX}$ | — | 20 | — | ns |
| REF_CLK duty cycle | $t_{RMXH}/t_{RMX}$ | 35 | — | 65 | % |
| REF_CLK to RMII data TXD[1:0], TX_EN delay | $t_{RMTKHDX}$ | 2 | — | 13 | ns |
| REF_CLK data clock rise $V_{IL}$(min) to $V_{IH}$(max) | $t_{RMXR}$ | 1.0 | — | 4.0 | ns |
| REF_CLK data clock fall $V_{IH}$(max) to $V_{IL}$(min) | $t_{RMXF}$ | 1.0 | — | 4.0 | ns |

**Note:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time $t_{RMX}$ clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of $t_{RMX}$ represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

The following figure provides the AC test load.

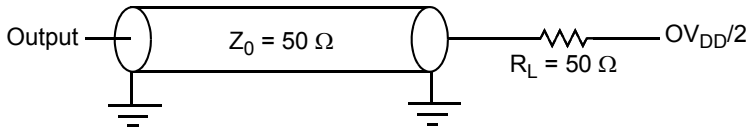



**Figure 14. AC Test Load**

# 9 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8306S.

## 9.1 TDM/SI DC Electrical Characteristics

The following table provides the DC electrical characteristics for the MPC8306S TDM/SI.

**Table 26. TDM/SI DC Electrical Characteristics**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –2.0 mA | 2.4 | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.5 | V |
| Input high voltage | $V_{IH}$ | — | 2.0 | $OV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | $0 V \le V_{IN} \le OV_{DD}$ | — | ±5 | μA |

## 9.2 TDM/SI AC Timing Specifications

The following table provides the TDM/SI input and output AC timing specifications.

**Table 27. TDM/SI AC Timing Specifications[1]**

| Characteristic | Symbol[2] | Min | Max | Unit |
|---|---|---|---|---|
| TDM/SI outputs—External clock delay | $t_{SEKHOV}$ | 2 | 14 | ns |
| TDM/SI outputs—External clock High Impedance | $t_{SEKHOX}$ | 2 | 10 | ns |
| TDM/SI inputs—External clock input setup time | $t_{SEIVKH}$ | 5 | — | ns |
| TDM/SI inputs—External clock input hold time | $t_{SEIXKH}$ | 2 | — | ns |

**Notes:**
1. Output specifications are measured from the 50% level of the rising edge of QE_CLK_IN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{SEKHOX}$ symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

The following figure provides the AC test load for the TDM/SI.

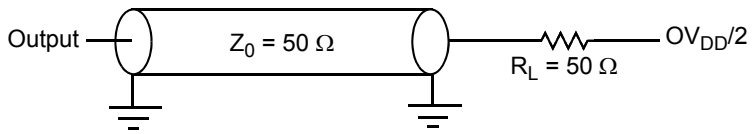



**Figure 18. TDM/SI AC Test Load**

**Table 29. HDLC AC Timing Specifications[1] (continued)**

| Characteristic | Symbol[2] | Min | Max | Unit |
|---|---|---|---|---|
| Outputs—External clock high impedance | $t_{HEKHOX}$ | 1 | 8 | ns |
| Inputs—Internal clock input setup time | $t_{HIIVKH}$ | 9 | — | ns |
| Inputs—External clock input setup time | $t_{HEIVKH}$ | 4 | — | ns |
| Inputs—Internal clock input hold time | $t_{HIIXKH}$ | 0 | — | ns |
| Inputs—External clock input hold time | $t_{HEIXKH}$ | 1 | — | ns |

**Notes:**
1. Output specifications are measured from the 50% level of the rising edge of QE_CLK_IN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{HIKHOX}$ symbolizes the outputs internal timing (HI) for the time $t_{serial}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

The following figure provides the AC test load.

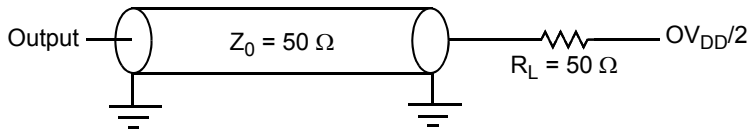
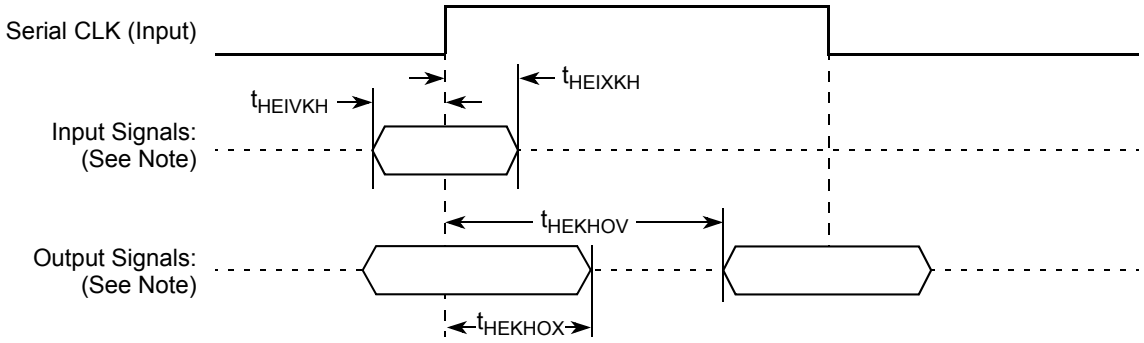



**Figure 20. AC Test Load**

Figure 21 and Figure 22 represent the AC timing from Table 29. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

The following figure shows the timing with external clock.




**Note:** The clock edge is selectable.

**Figure 21. AC Timing (External Clock) Diagram**

# 13 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8306S.

## 13.1 I²C DC Electrical Characteristics

The following table provides the DC electrical characteristics for the I²C interface of the MPC8306S.

**Table 34. I²C DC Electrical Characteristics**

At recommended operating conditions with $OV_{DD}$ of 3.3 V ± 300mV.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high voltage level | $V_{IH}$ | $0.7 \times OV_{DD}$ | $OV_{DD} + 0.3$ | V | — |
| Input low voltage level | $V_{IL}$ | –0.3 | $0.3 \times OV_{DD}$ | V | — |
| Low level output voltage | $V_{OL}$ | 0 | 0.4 | V | 1 |
| Output fall time from $V_{IH}$(min) to $V_{IL}$(max) with a bus capacitance from 10 to 400 pF | $t_{I2KLKV}$ | $20 + 0.1 \times C_B$ | 250 | ns | 2 |
| Pulse width of spikes which must be suppressed by the input filter | $t_{I2KHKL}$ | 0 | 50 | ns | 3 |
| Capacitance for each I/O pin | $C_I$ | — | 10 | pF | — |
| Input current ($0 V \le V_{IN} \le OV_{DD}$) | $I_{IN}$ | — | ±5 | μA | 4 |

**Notes:**
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. $C_B$ = capacitance of one bus line in pF.
3. Refer to the *MPC8306S PowerQUICC II Pro Integrated Communications Processor Family Reference Manual* for information on the digital filter used.
4. I/O pins obstructs the SDA and SCL lines if $OV_{DD}$ is switched off.

## 13.2 I²C AC Electrical Specifications

The following table provides the AC timing parameters for the I²C interface of the MPC8306S.

**Table 35. I²C AC Electrical Specifications**

All values refer to $V_{IH}$ (min) and $V_{IL}$ (max) levels (see Table 34).

| Parameter | Symbol[1] | Min | Max | Unit |
|---|---|---|---|---|
| SCL clock frequency | $f_{I2C}$ | 0 | 400 | kHz |
| Low period of the SCL clock | $t_{I2CL}$ | 1.3 | — | μs |
| High period of the SCL clock | $t_{I2CH}$ | 0.6 | — | μs |
| Setup time for a repeated START condition | $t_{I2SVKH}$ | 0.6 | — | μs |
| Hold time (repeated) START condition (after this period, the first clock pulse is generated) | $t_{I2SXKL}$ | 0.6 | — | μs |
| Data setup time | $t_{I2DVKH}$ | 100 | — | ns |
| Data hold time: I²C bus devices | $t_{I2DXKL}$ | 300 | 0.9[3] | μs |
| Rise time of both SDA and SCL signals | $t_{I2CR}$ | $20 + 0.1\ C_B$[4] | 300 | ns |

**Table 44. JTAG Interface DC Electrical Characteristics (continued)**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | — | 2.0 | $OV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | $0 V \le V_{IN} \le OV_{DD}$ | — | ±5 | μA |

## 18.2 JTAG AC Electrical Characteristics

This section describes the AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8306S. The following table provides the JTAG AC timing specifications as defined in Figure 33 through Figure 36.

**Table 45. JTAG AC Timing Specifications (Independent of SYS_CLK_IN)[1]**

At recommended operating conditions (see Table 2).

| Parameter | Symbol[2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| JTAG external clock frequency of operation | $f_{JTG}$ | 0 | 33.3 | MHz | — |
| JTAG external clock cycle time | $t_{JTG}$ | 30 | — | ns | — |
| JTAG external clock pulse width measured at 1.4 V | $t_{JTKHKL}$ | 11 | — | ns | — |
| JTAG external clock rise and fall times | $t_{JTGR}$, $t_{JTGF}$ | 0 | 2 | ns | — |
| $\overline{\text{TRST}}$ assert time | $t_{TRST}$ | 25 | — | ns | 3 |
| Input setup times:<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDVKH}$<br>$t_{JTIVKH}$ | <br>4<br>4 | <br>—<br>— | ns | 4 |
| Input hold times:<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDXKH}$<br>$t_{JTIXKH}$ | <br>10<br>10 | <br>—<br>— | ns | 4 |
| Valid times:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDV}$<br>$t_{JTKLOV}$ | <br>2<br>2 | <br>15<br>15 | ns | 5 |

# 19 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8306S is available in a thermally enhanced MAPBGA (mold array process-ball grid array); see Section 19.1, "Package Parameters for the MPC8306S," and Section 19.2, "Mechanical Dimensions of the MPC8306S MAPBGA," for information on the MAPBGA.

## 19.1 Package Parameters for the MPC8306S

The package parameters are as provided in the following list.

| | |
|---|---|
| Package outline | 19 mm × 19 mm |
| Package Type | MAPBGA |
| Interconnects | 369 |
| Pitch | 0.80 mm |
| Module height (typical) | 1.48 mm; Min = 1.31mm and Max 1.61mm |
| Solder Balls | 96 Sn / 3.5 Ag / 0.5 Cu (VM package) |
| Ball diameter (typical) | 0.40 mm |

## 19.2 Mechanical Dimensions of the MPC8306S MAPBGA

The following figure shows the mechanical dimensions and bottom surface nomenclature of the MPC8306S, 369-MAPBGA package.

**Table 46. MPC8306S Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| LA[17] | B14 | O | $OV_{DD}$ | — |
| LA[18] | A14 | O | $OV_{DD}$ | — |
| LA[19] | A15 | O | $OV_{DD}$ | — |
| LA[20] | A16 | O | $OV_{DD}$ | — |
| LA[21] | B16 | O | $OV_{DD}$ | — |
| LA[22] | A17 | O | $OV_{DD}$ | — |
| LA[23] | B17 | O | $OV_{DD}$ | — |
| LA[24] | A18 | O | $OV_{DD}$ | — |
| LA[25] | B19 | O | $OV_{DD}$ | — |
| LCS_B[0] | A19 | O | $OV_{DD}$ | 3 |
| LCS_B[1] | B20 | O | $OV_{DD}$ | 3 |
| LCS_B[2] | A20 | O | $OV_{DD}$ | 3 |
| LCS_B[3] | A21 | O | $OV_{DD}$ | 3 |
| LCLK[0] | D13 | O | $OV_{DD}$ | — |
| LGPL[0] | B22 | O | $OV_{DD}$ | — |
| LGPL[1] | D16 | O | $OV_{DD}$ | — |
| LGPL[2] | D19 | O | $OV_{DD}$ | — |
| LGPL[3] | D17 | O | $OV_{DD}$ | — |
| LGPL[4] | E18 | IO | $OV_{DD}$ | — |
| LGPL[5] | E19 | O | $OV_{DD}$ | — |
| LWE_B[0] | D15 | O | $OV_{DD}$ | — |
| LWE_B[1] | D14 | O | $OV_{DD}$ | — |
| LBCTL | A22 | O | $OV_{DD}$ | — |
| LALE | B23 | O | $OV_{DD}$ | — |
| **JTAG** | | | | |
| TCK | A3 | I | $OV_{DD}$ | — |
| TDI | B5 | I | $OV_{DD}$ | 3 |
| TDO | D7 | O | $OV_{DD}$ | — |
| TMS | A4 | I | $OV_{DD}$ | 3 |
| TRST_B | D8 | I | $OV_{DD}$ | 3 |
| **Test Interface** | | | | |
| TEST_MODE | A5 | I | $OV_{DD}$ | — |
| **System Control Signals** | | | | |
| HRESET_B | U20 | IO | $OV_{DD}$ | 1 |
| PORESET_B | V20 | I | $OV_{DD}$ | — |

**Table 46. MPC8306S Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **Clock Interface** | | | | |
| QE_CLK_IN | P23 | I | $OV_{DD}$ | — |
| SYS_CLK_IN | R23 | I | $OV_{DD}$ | — |
| RTC_PIT_CLOCK | V23 | I | $OV_{DD}$ | — |
| **Miscellaneous Signals** | | | | |
| QUIESCE_B | A2 | O | $OV_{DD}$ | — |
| THERM0 | D6 | I | $OV_{DD}$ | — |
| **GPIO** | | | | |
| GPIO[0]/MSRCID0 (DDR ID) | E5 | IO | $OV_{DD}$ | — |
| GPIO[1]/MSRCID1 (DDR ID) | E6 | IO | $OV_{DD}$ | — |
| GPIO[2]/MSRCID2 (DDR ID) | D4 | IO | $OV_{DD}$ | — |
| GPIO[3]/MSRCID3 (DDR ID) | C2 | IO | $OV_{DD}$ | — |
| GPIO[4]/MSRCID4 (DDR ID) | C1 | IO | $OV_{DD}$ | — |
| GPIO[5]/MDVAL (DDR ID) | B1 | IO | $OV_{DD}$ | — |
| GPIO[6]/QE_EXT_REQ_3 | B3 | IO | $OV_{DD}$ | — |
| GPIO[7]/QE_EXT_REQ_1 | B2 | IO | $OV_{DD}$ | — |
| **USB** | | | | |
| USBDR_PWRFAULT/IIC_SDA2/CE_PIO_1 | AC4 | IO | $OV_{DD}$ | 2 |
| USBDR_CLK/UART2_SIN[2]/UART2_CTS_B[1] | Y9 | I | $OV_{DD}$ | |
| USBDR_DIR/IIC_SCL2 | AC3 | IO | $OV_{DD}$ | 2 |
| USBDR_NXT/UART2_SIN[1]/QE_EXT_REQ_4 | AC2 | IO | $OV_{DD}$ | — |
| USBDR_PCTL[0]/UART2_SOUT[1]/ LB_POR_CFG_BOOT_ECC | AB3 | IO | $OV_{DD}$ | — |
| USBDR_PCTL[1]/UART2_SOUT[2]/ UART2_RTS_B1/LB_POR_BOOT_ERR | Y8 | O | $OV_{DD}$ | — |
| USBDR_STP/QE_EXT_REQ_2 | W6 | IO | $OV_{DD}$ | — |
| USBDR_TXDRXD[0]/UART1_SOUT[1]/ GPIO[32]/QE_TRB_O | AB7 | IO | $OV_{DD}$ | — |
| USBDR_TXDRXD[1]/UART1_SIN[1]/GPIO[33]/ QE_TRB_I | AB8 | IO | $OV_{DD}$ | — |
| USBDR_TXDRXD[2]/UART1_SOUT[2]/ UART1_RTS_B1/QE_BRG[1] | AC6 | IO | $OV_{DD}$ | — |
| USBDR_TXDRXD[3]/UART1_SIN[2]/ UART1_CTS_B1/QE_BRG[2] | AC5 | IO | $OV_{DD}$ | — |
| USBDR_TXDRXD[4]/GPIO[34]/QE_BRG[3] | AB5 | IO | $OV_{DD}$ | — |
| USBDR_TXDRXD[5]/GPIO[35]/QE_BRG[4] | Y7 | IO | $OV_{DD}$ | — |
| USBDR_TXDRXD[6]/GPIO[36]/QE_BRG[9] | Y6 | IO | $OV_{DD}$ | — |

**Table 46. MPC8306S Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| FEC3_TXD0/TSEC_TMR_PP2/GPIO[60] | R20 | IO | $OV_{DD}$ | — |
| FEC3_TXD1/TSEC_TMR_PP3/GPIO[61] | T22 | IO | $OV_{DD}$ | — |
| FEC3_TXD2/TSEC_TMR_ALARM1/GPIO[62] | T23 | IO | $OV_{DD}$ | — |
| FEC3_TXD3/TSEC_TMR_ALARM2/GPIO[63] | T20 | IO | $OV_{DD}$ | — |
| **HDLC/GPIO/TDM** | | | | |
| HDLC1_RXCLK/TDM1_RCK/GPIO[1] | U23 | IO | $OV_{DD}$ | — |
| HDLC1_RXD/TDM1_RD/GPIO[3] | U22 | IO | $OV_{DD}$ | — |
| HDLC1_TXCLK/GPIO[0]/TDM1_TCK/ QE_BRG[5] | AC22 | IO | $OV_{DD}$ | — |
| HDLC1_TXD/GPIO[2]/TDM1_TD/ CFG_RESET_SOURCE[0] | W18 | IO | $OV_{DD}$ | — |
| HDLC1_CD_B/GPIO[4]/TDM1_TFS | W19 | IO | $OV_{DD}$ | — |
| HDLC1_CTS_B/GPIO[5]/TDM1_RFS | Y20 | IO | $OV_{DD}$ | — |
| HDLC1_RTS_B/GPIO[6]/TDM1_STROBE_B/ CFG_RESET_SOURCE[1] | AB22 | IO | $OV_{DD}$ | — |
| HDLC2_TXCLK/GPIO[16]/TDM2_TCK/ QE_BRG[7] | AB23 | IO | $OV_{DD}$ | — |
| HDLC2_RXCLK/GPIO[17]/TDM2_RCK/ QE_BRG[8] | AA23 | IO | $OV_{DD}$ | — |
| HDLC2_TXD/GPIO[18]/TDM2_TD/ CFG_RESET_SOURCE[2] | W20 | IO | $OV_{DD}$ | — |
| HDLC2_RXD/GPIO[19]/TDM2_RD | Y23 | IO | $OV_{DD}$ | — |
| HDLC2_CD_B/GPIO[20]/TDM2_TFS | Y22 | IO | $OV_{DD}$ | — |
| HDLC2_CTS_B/GPIO[21]/TDM2_RFS | W23 | IO | $OV_{DD}$ | — |
| HDLC2_RTS_B/GPIO[22]/TDM2_STROBE_B/ CFG_RESET_SOURCE[3] | W22 | IO | $OV_{DD}$ | — |
| **Power** | | | | |
| $AV_{DD1}$ | L16 | — | — | — |
| $AV_{DD2}$ | M16 | — | — | — |
| $AV_{DD3}$ | N8 | — | — | — |
| $GV_{DD}$ | G5, H5, J5, K5, L5, M5, N5, P5, R5, T5, U5 | — | — | — |
| $OV_{DD}$ | E7,E8,E9,E10,E11,E12, E13,E14, E15, E16,E17,G19,H19,J19,K 19,L19,M19, N19,P19,R19,T19,U19, W7,W8,W9, W10,W11, W12,W13, W14,W15, W16, W17 | — | — | — |

**Table 51. e300 Core PLL Configuration (continued)**

| RCWL[COREPLL] | | | *core_clk* : *csb_clk* Ratio | VCO Divider |
|---|---|---|---|---|
| 0-1 | 2-5 | 6 | | |
| 00 | 0001 | 1 | 1.5:1 | ÷ 2 |
| 01 | 0001 | 1 | 1.5:1 | ÷ 4 |
| 10 | 0001 | 1 | 1.5:1 | ÷ 8 |
| 11 | 0001 | 1 | 1.5:1 | ÷ 8 |
| 00 | 0010 | 0 | 2:1 | ÷ 2 |
| 01 | 0010 | 0 | 2:1 | ÷ 4 |
| 10 | 0010 | 0 | 2:1 | ÷ 8 |
| 11 | 0010 | 0 | 2:1 | ÷ 8 |
| 00 | 0010 | 1 | 2.5:1 | ÷ 2 |
| 01 | 0010 | 1 | 2.5:1 | ÷ 4 |
| 10 | 0010 | 1 | 2.5:1 | ÷ 8 |
| 11 | 0010 | 1 | 2.5:1 | ÷ 8 |
| 00 | 0011 | 0 | 3:1 | ÷ 2 |
| 01 | 0011 | 0 | 3:1 | ÷ 4 |
| 10 | 0011 | 0 | 3:1 | ÷ 8 |
| 11 | 0011 | 0 | 3:1 | ÷ 8 |

**NOTE**

Core VCO frequency = core frequency × VCO divider. The VCO divider (RCWL[COREPLL[0:1]]), must be set properly so that the core VCO frequency is in the range of 400–800 MHz.

## 20.4 QUICC Engine PLL Configuration

The QUICC Engine PLL is controlled by the RCWL[CEPMF] and RCWL[CEPDF] parameters. The following table shows the multiplication factor encodings for the QUICC Engine PLL.

**Table 52. QUICC Engine PLL Multiplication Factors**

| RCWL[CEPMF] | RCWL[CEPDF] | QUICC Engine PLL Multiplication Factor = RCWL[CEPMF]/ (1 + RCWL[CEPDF]) |
|---|---|---|
| 00000–00001 | 0 | Reserved |
| 00010 | 0 | × 2 |
| 00011 | 0 | × 3 |
| 00100 | 0 | × 4 |
| 00101 | 0 | × 5 |
| 00110 | 0 | × 6 |

**Table 54. Suggested PLL Configurations**

| Conf No. | SPMF | Core PLL | CEPMF | CEDF | Input Clock Frequency (MHz) | CSB Frequency (MHz) | Core Frequency (MHz) | QUICC Engine Frequency (MHz) |
|---|---|---|---|---|---|---|---|---|
| 1 | 0100 | 0000100 | 0111 | 0 | 33.33 | 133.33 | 266.66 | 233 |
| 2 | 0010 | 0000100 | 0111 | 1 | 66.67 | 133.33 | 266.66 | 233 |
| 3 | 0100 | 0000101 | 0111 | 0 | 33.33 | 133.33 | 333.33 | 233 |
| 4 | 0101 | 0000101 | 1001 | 0 | 25 | 125 | 312.5 | 225 |
| 5 | 0010 | 0000101 | 0111 | 1 | 66.67 | 133.33 | 333.33 | 233 |

# 21 Thermal

This section describes the thermal specifications of the MPC8306S.

## 21.1 Thermal Characteristics

The following table provides the package thermal characteristics for the 369, 19 × 19 mm MAPBGA of the MPC8306S.

**Table 55. Package Thermal Characteristics for MAPBGA**

| Characteristic | Board type | Symbol | Value | Unit | Notes |
|---|---|---|---|---|---|
| Junction-to-ambient natural convection | Single-layer board (1s) | $R_{\theta JA}$ | 39 | °C/W | 1, 2 |
| Junction-to-ambient natural convection | Four-layer board (2s2p) | $R_{\theta JA}$ | 24 | °C/W | 1, 2, 3 |
| Junction-to-ambient (@200 ft/min) | Single-layer board (1s) | $R_{\theta JMA}$ | 32 | °C/W | 1, 3 |
| Junction-to-ambient (@200 ft/min) | Four-layer board (2s2p) | $R_{\theta JMA}$ | 21 | °C/W | 1, 3 |
| Junction-to-board | — | $R_{\theta JB}$ | 14 | °C/W | 4 |
| Junction-to-case | — | $R_{\theta JC}$ | 9 | °C/W | 5 |
| Junction-to-package top | Natural convection | $\Psi_{JT}$ | 2 | °C/W | 6 |

**Notes:**
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

### 21.1.1 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$, where $P_{I/O}$ is the power dissipation of the I/O drivers.

### 21.1.2 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, $T_J$, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \qquad \textit{Eqn. 1}$$

where:

$T_J$ = junction temperature (°C)

The following table summarizes the signal impedance targets. The driver impedance is targeted at minimum $V_{DD}$, nominal $OV_{DD}$, 105°C.

**Table 56. Impedance Characteristics**

| Impedance | Local Bus, Ethernet, DUART, Control, Configuration and Power Management | DDR DRAM | Symbol | Unit |
|---|---|---|---|---|
| $R_N$ | 42 Target | 20 Target | $Z_0$ | Ω |
| $R_P$ | 42 Target | 20 Target | $Z_0$ | Ω |
| Differential | NA | NA | $Z_{DIFF}$ | Ω |

**Note:** Nominal supply voltages. See Table 1, $T_j$ = 105°C.

## 22.5 Configuration Pin Multiplexing

The MPC8306S provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (Refer to the "Reset, Clocking and Initialization" of *MPC8306S PowerQUICC II Pro Integrated Communications Processor Family Reference Manual*). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

# 23 Ordering Information

This section presents ordering information for the devices discussed in this document, and it shows an example of how the parts are marked. Ordering information for the devices fully covered by this document is provided in Section 23.1, "Part Numbers Fully Addressed by This Document."

## 23.1 Part Numbers Fully Addressed by This Document

The following table provides the Freescale part numbering nomenclature for the MPC8306S family. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the maximum processor core frequency, the part numbering scheme also includes the maximum effective DDR memory speed and QUICC Engine bus frequency. Each part number also contains a revision code which refers to the die mask revision number.