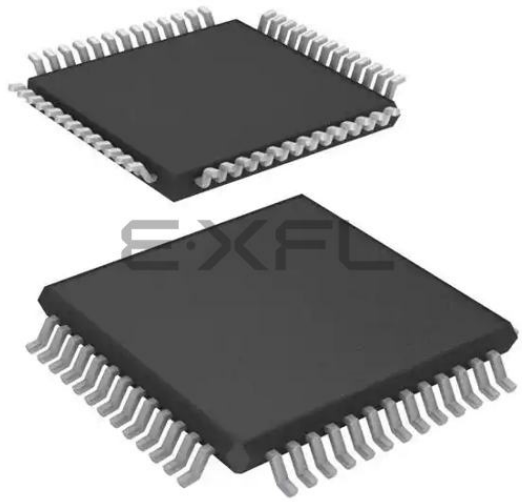
Analog Devices Inc./Maxim Integrated - DS87C530-ENL Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-TQFP
Supplier Device Package	52-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds87c530-enl

ORDERING INFORMATION

PART	TEMP RANGE	MAX CLOCK SPEED (MHz)	PIN-PACKAGE
DS87C530-QCL	0°C to +70°C	33	52 PLCC
DS87C530-QCL+	0°C to +70°C	33	52 PLCC
DS87C530-QNL	-40°C to +85°C	33	52 PLCC
DS87C530-QNL+	-40°C to +85°C	33	52 PLCC
DS87C530-KCL*	0°C to +70°C	33	52 Windowed CLCC
DS87C530-ECL	0°C to +70°C	33	52 TQFP
DS87C530-ECL+	0°C to +70°C	33	52 TQFP
DS87C530-ENL	-40°C to +85°C	33	52 TQFP
DS87C530-ENL+	-40°C to +85°C	33	52 TQFP
DS83C530-QCL	0°C to +70°C	33	52 PLCC
DS83C530-QCL+	0°C to +70°C	33	52 PLCC
DS83C530-QNL	-40°C to +85°C	33	52 PLCC
DS83C530-QNL+	-40°C to +85°C	33	52 PLCC
DS83C530-ECL	0°C to +70°C	33	52 TQFP
DS83C530-ECL+	0°C to +70°C	33	52 TQFP
DS83C530-ENL	-40°C to +85°C	33	52 TQFP
DS83C530-ENL+	-40°C to +85°C	33	52 TQFP

+ Denotes a lead(Pb)-free/RoHS-compliant device.

** The windowed ceramic LCC package is intrinsically lead(Pb) free.*

DETAILED DESCRIPTION

The DS87C530/DS83C530 EPROM/ROM microcontrollers with a real-time clock (RTC) are 8051-compatible microcontrollers based on the Dallas Semiconductor high-speed core. They use 4 clocks per instruction cycle instead of the 12 used by the standard 8051. They also provide a unique mix of peripherals not widely available on other processors. They include an on-chip RTC and battery backup support for an on-chip 1k x 8 SRAM. The new Power Management Mode allows software to select reduced power operation while still processing.

A combination of high-performance microcontroller core, RTC, battery-backed SRAM, and power management makes the DS87C530/DS83C530 ideal for instruments and portable applications. They also provide several peripherals found on other Dallas high-speed microcontrollers. These include two independent serial ports, two data pointers, on-chip power monitor with brownout detection and a watchdog timer.

Power Management Mode (PMM) allows software to select a slower CPU clock. While default operation uses four clocks per machine cycle, the PMM runs the processor at 64 or 1024 clocks per cycle. There is a corresponding drop in power consumption when the processor slows.

The EMI reduction feature allows software to select a reduced emission mode. This disables the ALE signal when it is unneeded.

The DS83C530 is a factory mask ROM version of the DS87C530 designed for high-volume, cost-sensitive applications. It is identical in all respects to the DS87C530, except that the 16kB of EPROM is replaced by a user-supplied application program. All references to features of the DS87C530 will apply to the DS83C530, with the exception of EPROM-specific features where noted. Please contact your local Dallas Semiconductor sales representative for ordering information.

Note: The DS87C530/DS83C530 are monolithic devices. A user must supply an external battery or super cap and a 32.768kHz timekeeping crystal to have permanently powered timekeeping or nonvolatile RAM. The DS87C530/DS83C530 provide all the support and switching circuitry needed to manage these resources.

PIN DESCRIPTION (continued)

PIN		NAME	FUNCTION
PLCC	TQFP		
30	23	P2.0 (AD8)	**Port 2 (A8–A15), I/O**. Port 2 is a bidirectional I/O port. The reset condition of Port 2 is logic high. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pullup. When software writes a 0 to any port pin, the device will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. As an alternate function Port 2 can function as MSB of the external address bus. This bus can be used to read external ROM and read/write external RAM memory or peripherals.
31	24	P2.1 (AD9)	
32	25	P2.2 (AD10)	
33	26	P2.3 (AD11)	
34	27	P2.4 (AD12)	
35	28	P2.5 (AD13)	
36	29	P2.6 (AD14)	
37	30	P2.7 (AD15)	
15	8	P3.0	**Port 3, I/O.** Port 3 functions as both an 8-bit, bi-directional I/O port and an alternate functional interface for external interrupts, Serial Port 0, Timer 0 and 1 Inputs, and $\overline{RD}$ and $\overline{WR}$ strobes. The reset condition of Port 3 is with all bits at a logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pullup. When software writes a 0 to any port pin, the device will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. The alternate modes of Port 3 are outlined below. **Port** **Alternate** **Function** P3.0 RXD0 Serial Port 0 Input P3.1 TXD0 Serial Port 0 Output P3.2 $\overline{INT0}$ External Interrupt 0 P3.3 $\overline{INT1}$ External Interrupt 1 P3.4 T0 Timer 0 External Input P3.5 T1 Timer 1 External Input P3.6 $\overline{WR}$ External Data Memory Write Strobe P3.7 $\overline{RD}$ External Data Memory Read Strobe
16	9	P3.1	
17	10	P3.2	
18	11	P3.3	
19	12	P3.4	
20	13	P3.5	
21	14	P3.6	
22	15	P3.7	
42	35	$\overline{EA}$	**External Access Input, Active Low.** Connect to ground to use an external ROM. Internal RAM is still accessible as determined by register settings. Connect to V_{CC} to use internal ROM.
51	44	V_{BAT}	**V_{BAT} Input.** Connect to the power source that maintains SRAM and RTC when $V_{CC} < V_{BAT}$. Can be connected to a 3V lithium battery or a super cap. Connect to GND if battery will not be used with device.
27	20	RTCX2	**Timekeeping Crystals**. A 32.768kHz crystal between these pins supplies the time base for the RTC. The devices support both 6pF and 12.5pF load capacitance crystals as selected by an SFR bit (described later). To prevent noise from affecting the RTC, the RTCX2 and RTCX1 pins should be guard-ringed with GND2.
28	21	RTCX1	
2, 11, 13, 14, 40, 41	4, 6, 7, 33, 34, 47	N.C.	**Not Connected.** These pins should not be connected. They are reserved for use with future devices in the family.

The relative time of two instructions might be different in the new architecture than it was previously. For example, in the original architecture, the “MOVX A, @DPTR” instruction and the “MOV direct, direct” instruction used two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS87C530/DS83C530, the MOVX instruction takes as little as two machine cycles or eight oscillator cycles but the “MOV direct, direct” uses three machine cycles or 12 oscillator cycles. While both are faster than their original counterparts, they now have different execution times. This is because the DS87C530/DS83C530 usually use one instruction cycle for each instruction byte. The user concerned with precise program timing should examine the timing of each instruction for familiarity with the changes. Note that a machine cycle now requires just 4 clocks, and provides one ALE pulse per cycle. Many instructions require only one cycle, but some require five. In the original architecture, all were one or two cycles except for MUL and DIV. Refer to the *High-Speed Microcontroller User’s Guide* for details and individual instruction timing.

SPECIAL FUNCTION REGISTERS

Special Function Registers (SFRs) control most special features of the DS87C530/DS83C530. This allows the device to incorporate new features but remain instruction-set compatible with the 8051. EQUATE statements can be used to define the new SFR to an assembler or compiler. All SFRs contained in the standard 80C52 are duplicated in this device. Table 1 shows the register addresses and bit locations. The *High-Speed Microcontroller User’s Guide* describes all SFRs.

Table 1. Special Function Register Locations

** Functions not present in the 80C52 are in bold.*

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
P0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	80h
SP									81h
DPL									82h
DPH									83h
DPL1									84h
DPH1									85h
DPS	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**SEL**	86h
PCON	SMOD_0	**SMOD0**	—	—	GF1	GF0	STOP	IDLE	87h
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h
TMOD	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	89h
TL0									8Ah
TL1									8Bh
TH0									8Ch
TH1									8Dh
CKCON	**WD1**	**WD0**	**T2M**	**T1M**	**T0M**	**MD2**	**MD1**	**MD0**	8Eh
P1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	90h
EXIF	**IE5**	**IE4**	**IE3**	**IE2**	**XT/RG**	**RGMD**	**RGSL**	**BGS**	91h
TRIM	**E4K**	**X12/$\overline{6}$**	**TRM2**	**$\overline{TRM2}$**	**TRM1**	**$\overline{TRM1}$**	**TRM0**	**$\overline{TRM0}$**	96h
SCON0	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	98h
SBUF0									99h
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	A0h
IE	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	A8h
SADDR0									A9h
SADDR1									AAh
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B0h
IP	—	PS1	PT2	PS0	PT1	PX1	PT0	PX0	B8h
SADEN0									B9h
SADEN1									BAh
SCON1	**SM0/FE_1**	**SM1_1**	**SM2_1**	**REN_1**	**TB8_1**	**RB8_1**	**TI_1**	**RI_1**	C0h
SBUF1									C1h
ROMSIZE	—	—	—	—	—	**RMS2**	**RMS1**	**RMS0**	C2h
PMR	**CD1**	**CD0**	**SWB**	**—**	**XTOFF**	**ALEOFF**	**DME1**	**DME0**	C4h
STATUS	**PIP**	**HIP**	**LIP**	**XTUP**	**SPTA1**	**SPRA1**	**SPTA0**	**SPRA0**	C5h
TA									C7h
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	C8h
T2MOD	—	—	—	—	—	—	T2OE	DCEN	C9h
RCAP2L									CAh
RCAP2H									CBh

Table 1. Special Function Register Locations (continued)

** Functions not present in the 80C52 are in bold.*

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
TL2									CCh
TH2									CDh
PSW	CY	AC	F0	RS1	RS0	OV	FL	P	D0h
WDCON	**SMOD_1**	**POR**	**EPFI**	**PFI**	**WDIF**	**WTRF**	**EWT**	**RWT**	D8h
ACC									E0h
EIE	—	—	**ERTCI**	**EWDI**	**EX5**	**EX4**	**EX3**	**EX2**	E8h
B									F0h
RTASS									F2h
RTAS	0	0							F3h
RTAM	0	0							F4h
RTAH	0	0	0						F5h
EIP	—	—	**PRTCI**	**PWDI**	**PX5**	**PX4**	**PX3**	**PX2**	F8h
RTCC	**SSCE**	**SCE**	**MCE**	**HCE**	**RTCRE**	**RTCWE**	**RTCIF**	**RTCE**	F9h
RTCSS									FAh
RTCS	0	0							FBh
RTCM	0	0							FCh
RTCH									FDh
RTCD0									FEh
RTCD1									FFh

NONVOLATILE FUNCTIONS

The DS87C530/DS83C530 provide two functions that are permanently powered if a user supplies an external energy source. These are an on-chip RTC and a nonvolatile SRAM. The chip contains all related functions and controls. The user must supply a backup source and a 32.768kHz timekeeping crystal.

REAL-TIME CLOCK

The on-chip RTC keeps time of day and calendar functions. Its time base is a 32.768kHz crystal between pins RTCX1 and RTCX2. The RTC maintains time to 1/256 of a second. It also allows a user to read (and write) seconds, minutes, hours, day of the week, and date. Figure 2 shows the clock organization.

Timekeeping registers allow easy access to commonly needed time values. For example, software can simply check the elapsed number of minutes by reading one register. Alternately, it can read the complete time of day, including subseconds, in only four registers. The calendar stores its data in binary form. While this requires software translation, it allows complete flexibility as to the exact value. A user can start the calendar with a variety of selections since it is simply a 16-bit binary number of days. This number allows a total range of 179 years beginning from 0000.

The RTC features a programmable alarm condition. A user selects the alarm time. When the RTC reaches the selected value, it sets a flag. This will cause an interrupt if enabled, even in Stop mode. The alarm consists of a comparator that matches the user value against the RTC actual value. A user can select a match for 1 or more of the sub-seconds, seconds, minutes, or hours. This allows an interrupt

CRYSTAL-LESS PMM

A major component of power consumption in PMM is the crystal amplifier circuit. The DS87C530/DS83C530 allow the user to switch CPU operation to an internal ring oscillator and turn off the crystal amplifier. The CPU would then have a clock source of approximately 2MHz to 4MHz, divided by either 4, 64, or 1024. The ring is not accurate, so software cannot perform precision timing. However, this mode allows an additional saving of between 0.5mA and 6.0mA, depending on the actual crystal frequency. While this saving is of little use when running at 4 clocks per instruction cycle, it makes a major contribution when running in PMM1 or PMM2.

PMM OPERATION

Software invokes the PMM by setting the appropriate bits in the SFR area. The basic choices are divider speed and clock source. There are three speeds (4, 64, and 1024) and two clock sources (crystal, ring). Both the decisions and the controls are separate. Software will typically select the clock speed first. Then, it will perform the switch to ring operation if desired. Lastly, software can disable the crystal amplifier if desired.

There are two ways of exiting PMM. Software can remove the condition by reversing the procedure that invoked PMM or hardware can (optionally) remove it. To resume operation at a divide-by-4 rate under software control, simply select 4 clocks per cycle, and then crystal-based operation if relevant. When disabling the crystal as the time base in favor of the ring oscillator, there are timing restrictions associated with restarting the crystal operation. Details are described below.

There are three registers containing bits that are concerned with PMM functions. They are Power Management Register (PMR; C4h), Status (STATUS; C5h), and External Interrupt Flag (EXIF; 91h)

Clock Divider

Software can select the instruction cycle rate by selecting bits CD1 (PMR.7) and CD0 (PMR.6) as follows:

CD1	CD0	CYCLE RATE
0	0	Reserved
0	1	4 clocks (default)
1	0	64 clocks
1	1	1024 clocks

The selection of instruction cycle rate will take effect after a delay of one instruction cycle. Note that the clock divider choice applies to all functions including timers. Since baud rates are altered, it will be difficult to conduct serial communication while in PMM. There are minor restrictions on accessing the clock selection bits. The processor must be running in a 4-clock state to select either 64 (PMM1) or 1024 (PMM2) clocks. This means software cannot go directly from PMM1 to PMM2 or visa versa. It must return to a 4-clock rate first.

Switchback

To return to a 4-clock rate from PMM, software can simply select the CD1 and CD0 clock control bits to the 4 clocks per cycle state. However, the DS87C530/DS83C530 provide several hardware alternatives for automatic Switchback. If Switchback is enabled, then the device will automatically return to a 4-clock per cycle speed when an interrupt occurs from an enabled, valid external interrupt source. A Switchback will also occur when a UART detects the beginning of a serial start bit if the serial receiver is enabled (REN = 1). Note the beginning of a start bit does not generate an interrupt; this occurs on reception of a complete serial word. The automatic Switchback on detection of a start bit allows hardware to correct baud rates in time for a proper serial reception. A Switchback will also occur when a byte is written to the SBUF0 or SBUF1 for transmission.

Switchback is enabled by setting the SWB bit (PMR.5) to a 1 in software. For an external interrupt, Switchback will occur only if the interrupt source could really generate the interrupt. For example, if $\overline{\text{INT0}}$ is enabled but has a low priority setting, then Switchback will not occur on $\overline{\text{INT0}}$ if the CPU is servicing a high priority interrupt.

Status

Information in the Status register assists decisions about switching into PMM. This register contains information about the level of active interrupts and the activity on the serial ports.

The DS87C530/DS83C530 support three levels of interrupt priority. These levels are Power-fail, High, and Low. Bits STATUS.7–5 indicate the service status of each level. If PIP (Power-fail Interrupt Priority; STATUS. 7) is 1, then the processor is servicing this level. If either HIP (High Interrupt Priority; STATUS.6) or LIP (Low Interrupt Priority; STATUS.5) is high, then the corresponding level is in service.

Software should not rely on a lower priority level interrupt source to remove PMM (Switchback) when a higher level is in service. Check the current priority service level before entering PMM. If the current service level locks out a desired Switchback source, then it would be advisable to wait until this condition clears before entering PMM.

Alternately, software can prevent an undesired exit from PMM by entering a low priority interrupt service level before entering PMM. This will prevent other low priority interrupts from causing a Switchback.

Status also contains information about the state of the serial ports. Serial Port Zero Receive Activity (SPRA0; STATUS.0) indicates a serial word is being received on Serial Port 0 when this bit is set to a 1. Serial Port 0 Transmit Activity (SPTA0; STATUS.1) indicates that the serial port is still shifting out a serial transmission. STATUS.2 and STATUS.3 provide the same information for Serial Port 1, respectively. These bits should be interrogated before entering PMM1 or PMM2 to ensure that no serial port operations are in progress. Changing the clock divisor rate during a serial transmission or reception will corrupt the operation.

Crystal/Ring Operation

The DS87C530/DS83C530 allow software to choose the clock source as an independent selection from the instruction cycle rate. The user can select crystal-based or ring oscillator-based operation under software control. Power-on reset default is the crystal (or external clock) source. The ring may save power depending on the actual crystal speed. To save still more power, software can then disable the crystal amplifier. This process requires two steps. Reversing the process also requires two steps.

The XT/$\overline{RG}$ bit (EXIF.3) selects the crystal or ring as the clock source. Setting XT/$\overline{RG}$ = 1 selects the crystal. Setting XT/$\overline{RG}$ = 0 selects the ring. The RGMD (EXIF.2) bit serves as a status bit by indicating the active clock source. RGMD = 0 indicates the CPU is running from the crystal. RGMD = 1 indicates it is running from the ring. When operating from the ring, disable the crystal amplifier by setting the XTOFF bit (PMR.3) to a 1. This can only be done when XT/$\overline{RG}$ = 0.

When changing the clock source, the selection will take effect after a one-instruction-cycle delay. This applies to changes from crystal to ring and vise versa. However, this assumes that the crystal amplifier is running. In most cases, when the ring is active, software previously disabled the crystal to save power. If ring operation is being used and the system must switch to crystal operation, the crystal must first be enabled. Set the XTOFF bit to 0. At this time, the crystal oscillation will begin. The DS87C530/DS83C530 then provide a warm-up delay to make certain that the frequency is stable. Hardware will set the XTUP bit (STATUS.4) to 1 when the crystal is ready for use. Then software should write XT/$\overline{RG}$ to 1 to begin operating from the crystal. Hardware prevents writing XT/$\overline{RG}$ to 1 before XTUP = 1. The delay between XTOFF = 0 and XTUP = 1 will be 65,536 crystal clocks in addition to the crystal cycle startup time.

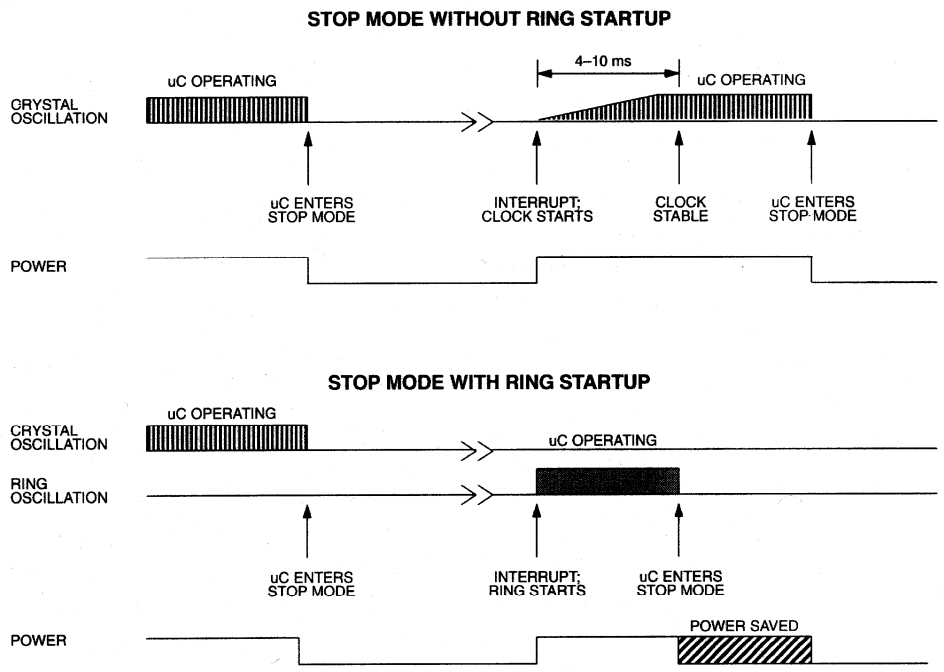
Switchback has no affect on the clock source. If software selects a reduced clock divider and enables the ring, a Switchback will only restore the divider speed. The ring will remain as the time base until altered by software. If there is serial activity, Switchback usually occurs with enough time to create proper baud rates. This is not true if the crystal is off and the CPU is running from the ring. If sending a serial character that wakes the system from crystal-less PMM, then it should be a dummy character of no importance with a subsequent delay for crystal startup.

Table 6 is a summary of the bits relating to PMM and its operation. The flow chart below illustrates a typical decision set associated with PMM.

The ring oscillator runs at approximately 2MHz to 4MHz but will not be a precise value. Do not conduct real-time precision operations (including serial communication) during this ring period. Figure 6 shows how the operation would compare when using the ring, and when starting up normally. The default state is to exit Stop mode without using the ring oscillator.

The RGSL ring-select bit at EXIF.1 (EXIF; 91h) controls this function. When RGSL = 1, the CPU will use the ring oscillator to exit Stop mode quickly. As mentioned above, the processor will automatically switch from the ring to the crystal after a delay of 65,536 crystal clocks. For a 3.57MHz crystal, this is approximately 18ms. The processor sets a flag called RGMD- Ring Mode, located at EXIF.2, that tells software that the ring is being used. The bit will be a logic 1 when the ring is in use. Attempt no serial communication or precision timing while this bit is set, since the operating frequency is not precise.

Figure 6. Ring Oscillator Exit from Stop Mode



NOTE: DIAGRAM ASSUMES THAT THE OPERATION FOLLOWING STOP REQUIRES LESS THAN 18ms TO COMPLETE.

EMI REDUCTION

One of the major contributors to radiated noise in an 8051-based system is the toggling of ALE. The DS87C530/DS83C530 allow software to disable ALE when not used by setting the ALEOFF (PMR.2) bit to 1. When ALEOFF = 1, ALE will still toggle during an off-chip MOVX. However, ALE will remain in a static when performing on-chip memory access. The default state of ALEOFF = 0 so ALE toggles with every instruction cycle.

PERIPHERAL OVERVIEW

The DS87C530/DS83C530 provide several of the most commonly needed peripheral functions in microcomputer-based systems. These new functions include a second serial port, power-fail reset, Power-fail interrupt, and a programmable watchdog timer. These are described below, and more details are available in the *High-Speed Microcontroller User's Guide*.

SERIAL PORTS

The DS87C530/DS83C530 provide a serial port (UART) that is identical to the 80C52. In addition it includes a second hardware serial port that is a full duplicate of the standard one. This port optionally uses pins P1.2 (RXD1) and P1.3 (TXD1). It has duplicate control functions included in new SFR locations.

Both ports can operate simultaneously but can be at different baud rates or even in different modes. The second serial port has similar control registers (SCON1; C0h, SBUF1; C1h) to the original. The new serial port can only use Timer 1 for timer-generated baud rates.

TIMER RATE CONTROL

There is one important difference between the DS87C530/DS83C530 and 8051 regarding timers. The original 8051 used 12 clocks per cycle for timers as well as for machine cycles. The DS87C530/DS83C530 architecture normally uses 4 clocks per machine cycle. However, in the area of timers and serial ports, the DS87C530/DS83C530 will default to 12 clocks per cycle on reset. This allows existing code with real-time dependencies such as baud rates to operate properly.

If an application needs higher speed timers or serial baud rates, the user can select individual timers to run at the 4-clock rate. The Clock Control register (CKCON; 8Eh) determines these timer speeds. When the relevant CKCON bit is logic 1, the DS87C530/DS83C530 use 4 clocks per cycle to generate timer speeds. When the bit is a 0, the DS87C530 uses 12 clocks for timer speeds. The reset condition is a 0. CKCON.5 selects the speed of Timer 2. CKCON.4 selects Timer 1 and CKCON.3 selects Timer 0. Unless a user desires very fast timing, it is unnecessary to alter these bits. Note that the timer controls are independent.

POWER-FAIL RESET

The DS87C530/DS83C530 use a precision bandgap voltage reference to decide if V_{CC} is out of tolerance. While powering up, the internal monitor circuit maintains a reset state until V_{CC} rises above the V_{RST} level. Once above this level, the monitor enables the crystal oscillator and counts 65,536 clocks. It then exits the reset state. This power-on reset (POR) interval allows time for the oscillator to stabilize.

A system needs no external components to generate a power-related reset. Anytime V_{CC} drops below V_{RST}, as in power failure or a power drop, the monitor will generate and hold a reset. It occurs automatically, needing no action from the software. Refer to the *Electrical Specifications* section for the exact value of V_{RST}.

POWER-FAIL INTERRUPT

The voltage reference that sets a precise reset threshold also generates an optional early warning power-fail interrupt (PFI). When enabled by software, the processor will vector to program memory address 0033h if V_{CC} drops below V_{PFW}. PFI has the highest priority. The PFI enable is in the Watchdog Control SFR (WDCON–D8h). Setting WDCON.5 to logic 1 will enable the PFI. Application software can also

TIMED-ACCESS PROTECTION

It is useful to protect certain SFR bits from an accidental write operation. The Timed-Access procedure stops an errant CPU from accidentally changing these bits. It requires that the following instructions precede a write of a protected bit.

```
MOV     0C7h, #0AAh
MOV     0C7h, #55h
```

Writing an AAh and then a 55h to the Timed-Access register (location C7h) opens a three-cycle window for write access. The window allows software to modify a protected bit(s). If these instructions do not immediately precede the write operation, then the write will not take effect. The protected bits are:

EXIF.0	BGS	Bandgap Select
WDCON.6	POR	Power-On Reset flag
WDCON.1	EWT	Enable Watchdog Reset
WDCON.0	RWT	Restart Watchdog
WDCON.3	WDIF	Watchdog Interrupt Flag
ROMSIZE.2	RMS2	ROM Size Select 2
ROMSIZE.1	RMS1	ROM Size Select 1
ROMSIZE.0	RMS0	ROM Size Select 0
TRIM.7–0	—	All RTC Trim Functions
RTCC.2	RTCWE	RTC Write Enable
RTCC.0	RTCE	RTC Oscillator Enable

EPROM PROGRAMMING

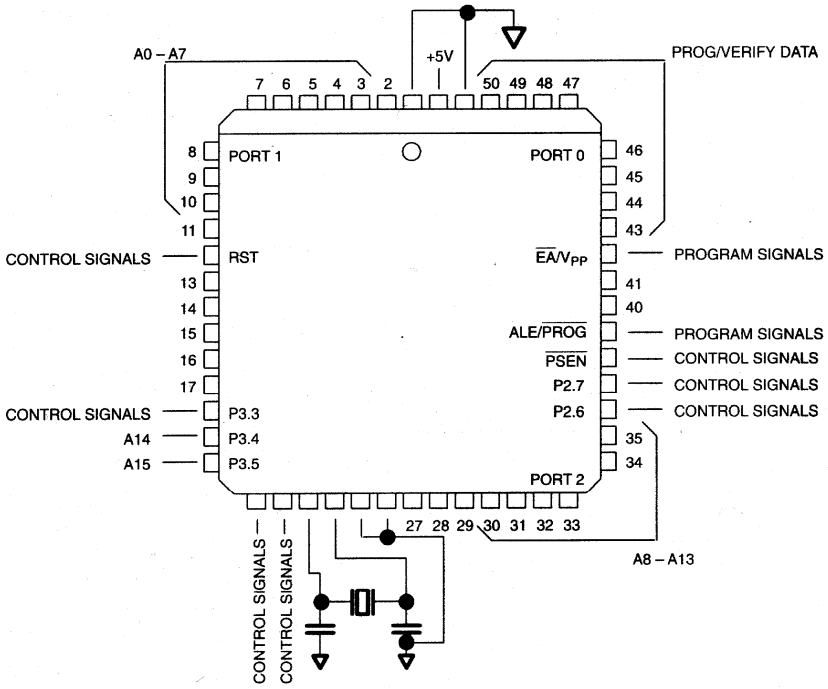
The DS87C530 follows standards for a 16kB EPROM version in the 8051 family. It is available in a UV erasable, ceramic windowed package and in plastic packages for one-time user-programmable versions. The part has unique signature information so programmers can support its specific EPROM options.

PROGRAMMING PROCEDURE

The DS87C530 should run from a clock speed between 4MHz and 6MHz when programmed. The programming fixture should apply address information for each byte to the address lines and the data value to the data lines. The control signals must be manipulated as shown in Table 9. The diagram in Figure 5 shows the expected electrical connection for programming. Note that the programmer must apply addresses in demultiplexed fashion to Ports 1 and 2 with data on Port 0. Waveforms and timing are provided in the *Electrical Specifications* section. Program the DS87C530 as follows:

1) Apply the address value,
2) Apply the data value,
3) Select the programming option from Table 9 using the control signals,
4) Increase the voltage on V_{PP} from 5V to 12.75V if writing to the EPROM,
5) Pulse the $\overline{PROG}$ signal five times for EPROM array and 25 times for encryption table, lock bits, and other EPROM bits,
6) Repeat as many times as necessary.

Figure 7. EPROM Programming Configuration



ROM-SPECIFIC FEATURES (DS83C530)

The DS83C530 supports a subset of the EPROM features found on the DS87C530.

SECURITY OPTIONS

Lock Bits

The DS83C530 employs a lock that restricts viewing of the ROM contents. When set, the lock will prevent MOVC instructions in external memory from reading program bytes in internal memory. When locked, the $\overline{EA}$ pin is sampled and latched on reset. The lock setting is enabled or disabled when the devices are manufactured according to customer specifications. The lock bit cannot be read in software, and its status can only be determined by observing the operation of the device.

Encryption Array

The DS83C530 Encryption Array allows an authorized user to verify ROM without allowing the true memory contents to be dumped. During a verify, each byte is Exclusive NORed (XNOR) with a byte in the Encryption Array. This results in a true representation of the ROM while the Encryption is unprogrammed (FFh). Once the Encryption Array is programmed in a non-FFh state, the Encryption Array is programmed (or optionally left unprogrammed) when the devices are manufactured according to customer specifications.

DS83C530 ROM Verification

The DS83C530 memory contents can be verified using a standard EPROM programmer. The memory address to be verified is placed on the pins shown in Figure 7, and the programming control pins are set to the levels shown in Table 9. The data at that location is then asserted on port 0.

DS83C530 Signature

The Signature bytes identify the DS83C530 to EPROM programmers. This information is at programming addresses 30h, 31h, and 60h. Because Mask ROM devices are not programmed in device programmers, most designers will find little use for the feature, and it is included only for compatibility.

ADDRESS	VALUE	MEANING
30h	DAh	Manufacturer
31h	31h	Model
60h	01h	Extension

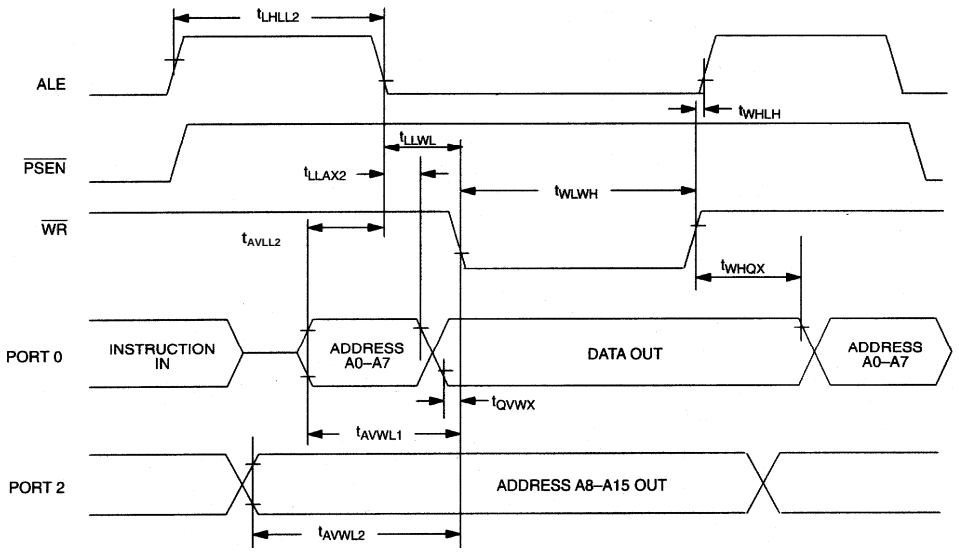
AC ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER		SYMBOL	33MHz		VARIABLE CLOCK		UNITS
			MIN	MAX	MIN	MAX	
Oscillator Frequency	External Oscillator	$1/t_{CLCL}$	0	33	0	33	MHz
	External Crystal		1	33	1	33	
ALE Pulse Width		t_{LHLL}	40		$1.5t_{CLCL}$-5		ns
Port 0 Address Valid to ALE Low		t_{AVLL}	10		$0.5t_{CLCL}$-5		ns
Address Hold after ALE Low		t_{LLAX1}	(Note 2)		(Note 2)		ns
ALE low to Valid Instruction In		t_{LLIV}		43		$2.5t_{CLCL}$-33	ns
ALE Low to $\overline{\text{PSEN}}$ Low		t_{LLPL}	4		$0.5t_{CLCL}$-11		ns
$\overline{\text{PSEN}}$ Pulse Width		t_{PLPH}	55		$2t_{CLCL}$-5		ns
$\overline{\text{PSEN}}$ Low to Valid Instruction In		t_{PLIV}		37		$2t_{CLCL}$-24	ns
Input Instruction Hold after $\overline{\text{PSEN}}$		t_{PXIX}	0		0		ns
Input Instruction Float after $\overline{\text{PSEN}}$		t_{PXIZ}		26		t_{CLCL}-5	ns
Port 0 Address to Valid Instruction In		t_{AVIV1}		59		$3t_{CLCL}$-32	ns
Port 2 Address to Valid Instruction In		t_{AVIV2}		68		$3.5t_{CLCL}$-38	ns
$\overline{\text{PSEN}}$ Low to Address Float		t_{PLAZ}		(Note 2)		(Note 2)	ns

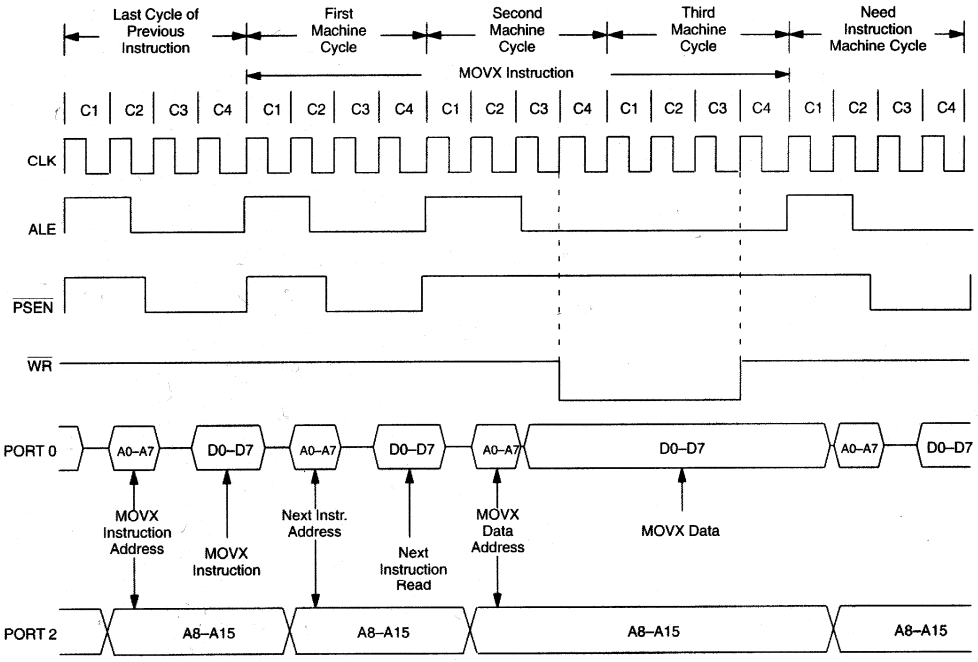
Note 1: All parameters apply to both commercial and industrial temperature range operation unless otherwise noted. Specifications to -40°C are guaranteed by design and are not production tested. AC electrical characteristics are not 100% tested, but are characterized and guaranteed by design. All signals are characterized with load capacitance of 80pF except Port 0, ALE, $\overline{\text{PSEN}}$, $\overline{\text{RD}}$ and $\overline{\text{WR}}$ with 100pF. Interfacing to memory devices with float times (turn off times) over 25ns may cause contention. This will not damage the parts, but will cause an increase in operating current. Specifications assume a 50% duty cycle for the oscillator. Port 2 and ALE timing will change in relation to duty cycle variation.

Note 2: Address is driven strongly until ALE falls, and is then held in a weak latch until overdriven externally.

DATA MEMORY WRITE CYCLE

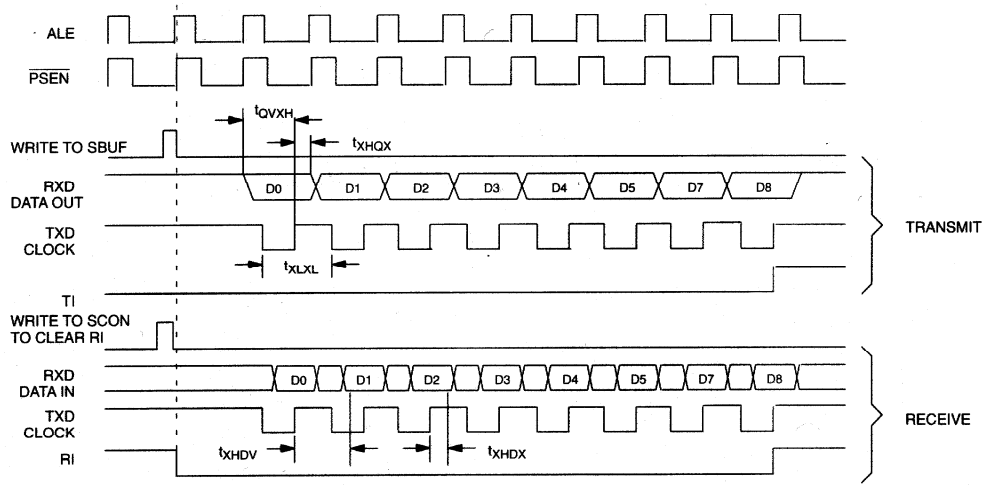


DATA MEMORY WRITE WITH STRETCH = 1

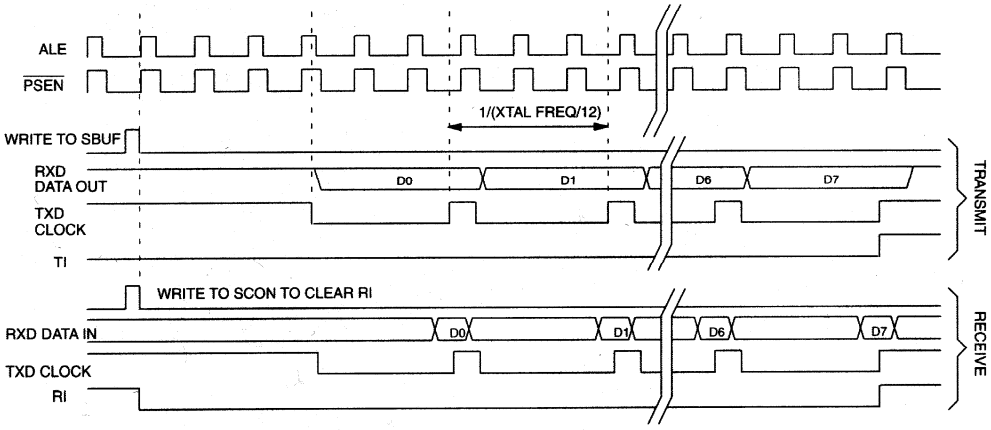


SERIAL PORT MODE 0 TIMING

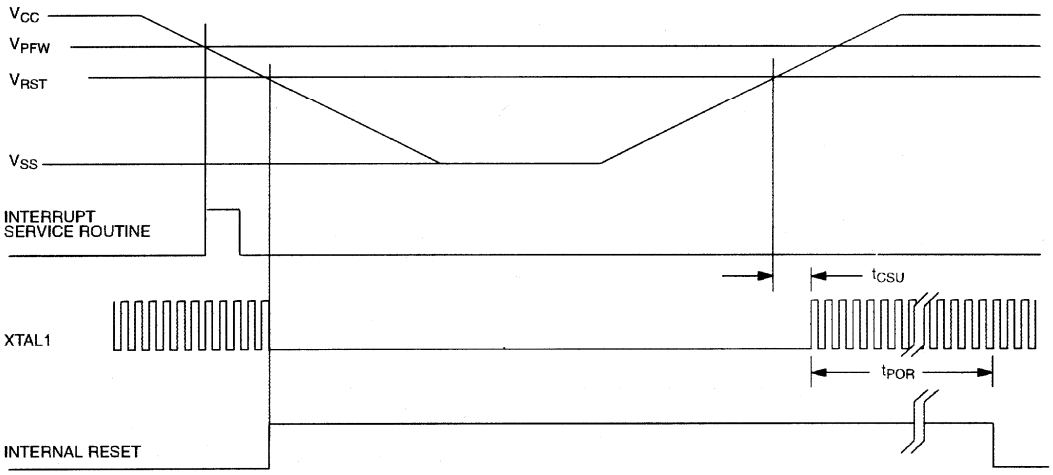
SERIAL PORT 0 (SYNCHRONOUS MODE)
HIGH SPEED OPERATION SM2=1=>TXD CLOCK=XTAL/4



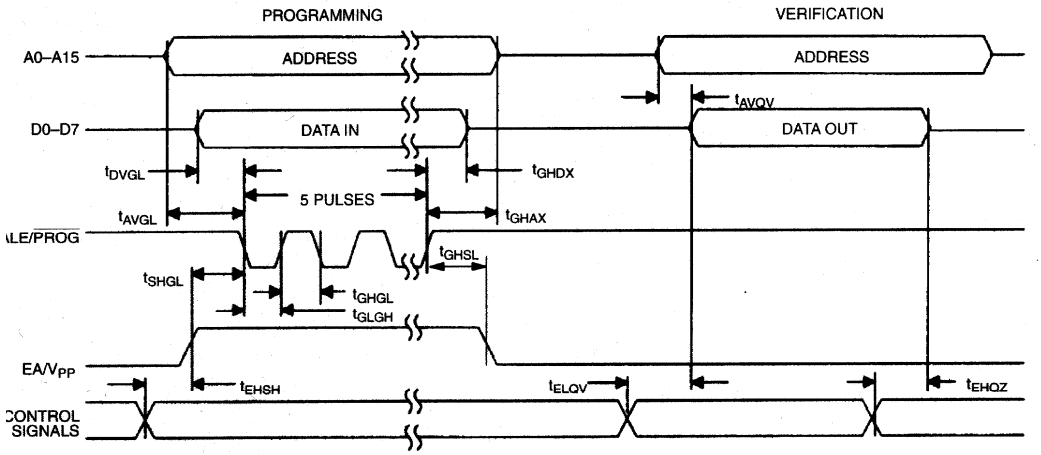
SERIAL PORT 0 (SYNCHRONOUS MODE)
SM2=0=>TXD CLOCK=XTAL/12



POWER-CYCLE TIMING



EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



PACKAGE INFORMATION

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
52 TQFP	C52+2	**21-0295**
52 CQUAD	K52-1	**21-0383**
52 PLCC	Q52+1	**21-0049**

DATA SHEET REVISION SUMMARY

REVISION	DESCRIPTION
071107	1) Corrected P1.5 pin for TQFP package from 4 to 1 (page 5).
070505	2) Added Pb-free/RoHS-compliant part numbers to Ordering Information table. 3) Deleted the "A" from the IPC/JEDEC J-STD-020 specification in the Absolute Maximum Ratings.
040104	4) Removed "Preliminary" status. 5) Soldering temperature parameter now references JEDEC specification. 6) Added note to absolute maximums clarifying voltages referenced to ground and storage temperature. 7) Updated I_{CC}, I_{IDLE}, I_{STOP}, I_{SPBG}, I_{IL}, and I_{TL} to incorporate errata conditions. 8) Added note clarifying DC electrical test conditions. 9) Added note clarifying V_{OH3} specification applies to first clock cycle following the transition. 10) Updated AC and MOVX electrical characteristics with final characterization values. 11) Added t_{AVLL2} specification and corrected MOVX timing diagrams to show t_{AVLL2} instead of t_{AVLL}. 12) Updated I_{BAT} to incorporate errata conditions.
112299	Contact factory for details.
070798	1) Added DS83C530 to data sheet. 2) Updated PMM operating current estimates. 3) Added note to clarify I_{IL} specification. 4) Added note to prevent accidental corruption of Watchdog Timer count while changing counter length. 5) Changed I_{BAT} specification to 1µA over extended temperature range. 6) Changed minimum oscillator frequency to 1MHz when using external crystal. 7) Changed RST pulldown resistance from 170kΩ to 200kΩ maximum. 8) Corrected "Data memory write with stretch" diagrams to show falling edge of ALE coincident with rising edge of C3 clock.
022097	1) Updated ALE pin description. 2) Added note pertaining to erasure window. 3) Added note pertaining to internal MOVX SRAM. 4) Changed Note 6 from RST=5.5V to RST=V_{CC}. 5) Changed Note 10 from RST=5.5V to RST=V_{CC}. 6) Changed serial port mode 0 timing diagram label from t_{QVXL} to t_{QVXH}. 7) Added information pertaining to 52-pin TQFP package.
060895	Initial release.

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