Analog Devices Inc./Maxim Integrated - DS87C530-KCL Datasheet

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	EPROM, UV
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	52-CLCC, Window (J Lead)
Supplier Device Package	52-CLCC (19.2x19.2)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds87c530-kcl

PIN DESCRIPTION (continued)

PIN		NAME	FUNCTION
PLCC	TQFP		
30	23	P2.0 (AD8)	**Port 2 (A8–A15), I/O**. Port 2 is a bidirectional I/O port. The reset condition of Port 2 is logic high. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pullup. When software writes a 0 to any port pin, the device will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. As an alternate function Port 2 can function as MSB of the external address bus. This bus can be used to read external ROM and read/write external RAM memory or peripherals.
31	24	P2.1 (AD9)	
32	25	P2.2 (AD10)	
33	26	P2.3 (AD11)	
34	27	P2.4 (AD12)	
35	28	P2.5 (AD13)	
36	29	P2.6 (AD14)	
37	30	P2.7 (AD15)	
15	8	P3.0	**Port 3, I/O.** Port 3 functions as both an 8-bit, bi-directional I/O port and an alternate functional interface for external interrupts, Serial Port 0, Timer 0 and 1 Inputs, and $\overline{\text{RD}}$ and $\overline{\text{WR}}$ strobes. The reset condition of Port 3 is with all bits at a logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pullup. When software writes a 0 to any port pin, the device will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. The alternate modes of Port 3 are outlined below. **Port** **Alternate** **Function** P3.0 RXD0 Serial Port 0 Input P3.1 TXD0 Serial Port 0 Output P3.2 $\overline{\text{INT0}}$ External Interrupt 0 P3.3 $\overline{\text{INT1}}$ External Interrupt 1 P3.4 T0 Timer 0 External Input P3.5 T1 Timer 1 External Input P3.6 $\overline{\text{WR}}$ External Data Memory Write Strobe P3.7 $\overline{\text{RD}}$ External Data Memory Read Strobe
16	9	P3.1	
17	10	P3.2	
18	11	P3.3	
19	12	P3.4	
20	13	P3.5	
21	14	P3.6	
22	15	P3.7	
42	35	$\overline{\text{EA}}$	**External Access Input, Active Low.** Connect to ground to use an external ROM. Internal RAM is still accessible as determined by register settings. Connect to V_{CC} to use internal ROM.
51	44	V_{BAT}	**V_{BAT} Input.** Connect to the power source that maintains SRAM and RTC when $V_{CC} < V_{BAT}$. Can be connected to a 3V lithium battery or a super cap. Connect to GND if battery will not be used with device.
27	20	RTCX2	**Timekeeping Crystals**. A 32.768kHz crystal between these pins supplies the time base for the RTC. The devices support both 6pF and 12.5pF load capacitance crystals as selected by an SFR bit (described later). To prevent noise from affecting the RTC, the RTCX2 and RTCX1 pins should be guard-ringed with GND2.
28	21	RTCX1	
2, 11, 13, 14, 40, 41	4, 6, 7, 33, 34, 47	N.C.	**Not Connected.** These pins should not be connected. They are reserved for use with future devices in the family.

The relative time of two instructions might be different in the new architecture than it was previously. For example, in the original architecture, the "MOVX A, @DPTR" instruction and the "MOV direct, direct" instruction used two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS87C530/DS83C530, the MOVX instruction takes as little as two machine cycles or eight oscillator cycles but the "MOV direct, direct" uses three machine cycles or 12 oscillator cycles. While both are faster than their original counterparts, they now have different execution times. This is because the DS87C530/DS83C530 usually use one instruction cycle for each instruction byte. The user concerned with precise program timing should examine the timing of each instruction for familiarity with the changes. Note that a machine cycle now requires just 4 clocks, and provides one ALE pulse per cycle. Many instructions require only one cycle, but some require five. In the original architecture, all were one or two cycles except for MUL and DIV. Refer to the *High-Speed Microcontroller User's Guide* for details and individual instruction timing.

SPECIAL FUNCTION REGISTERS

Special Function Registers (SFRs) control most special features of the DS87C530/DS83C530. This allows the device to incorporate new features but remain instruction-set compatible with the 8051. EQUATE statements can be used to define the new SFR to an assembler or compiler. All SFRs contained in the standard 80C52 are duplicated in this device. Table 1 shows the register addresses and bit locations. The *High-Speed Microcontroller User's Guide* describes all SFRs.

Table 1. Special Function Register Locations

** Functions not present in the 80C52 are in bold.*

REGISTER	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**	**ADDRESS**
P0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	80h
SP									81h
DPL									82h
DPH									83h
DPL1									84h
DPH1									85h
DPS	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**SEL**	86h
PCON	SMOD_0	**SMOD0**	—	—	GF1	GF0	STOP	IDLE	87h
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h
TMOD	GATE	C/$\overline{\text{T}}$	M1	M0	GATE	C/$\overline{\text{T}}$	M1	M0	89h
TL0									8Ah
TL1									8Bh
TH0									8Ch
TH1									8Dh
CKCON	**WD1**	**WD0**	**T2M**	**T1M**	**T0M**	**MD2**	**MD1**	**MD0**	8Eh
P1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	90h
EXIF	**IE5**	**IE4**	**IE3**	**IE2**	**XT/RG**	**RGMD**	**RGSL**	**BGS**	91h
TRIM	**E4K**	**X12/$\overline{6}$**	**TRM2**	**$\overline{\text{TRM2}}$**	**TRM1**	**$\overline{\text{TRM1}}$**	**TRM0**	**$\overline{\text{TRM0}}$**	96h
SCON0	SM0/FE_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	98h
SBUF0									99h
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	A0h
IE	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	A8h
SADDR0									A9h
SADDR1									AAh
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B0h
IP	—	PS1	PT2	PS0	PT1	PX1	PT0	PX0	B8h
SADEN0									B9h
SADEN1									BAh
SCON1	**SM0/FE_1**	**SM1_1**	**SM2_1**	**REN_1**	**TB8_1**	**RB8_1**	**TI_1**	**RI_1**	C0h
SBUF1									C1h
ROMSIZE	—	—	—	—	—	**RMS2**	**RMS1**	**RMS0**	C2h
PMR	**CD1**	**CD0**	**SWB**	**—**	**XTOFF**	**ALEOFF**	**DME1**	**DME0**	C4h
STATUS	**PIP**	**HIP**	**LIP**	**XTUP**	**SPTA1**	**SPRA1**	**SPTA0**	**SPRA0**	C5h
TA									C7h
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{\text{T2}}$	CP/$\overline{\text{RL2}}$	C8h
T2MOD	—	—	—	—	—	—	T2OE	DCEN	C9h
RCAP2L									CAh
RCAP2H									CBh

Table 1. Special Function Register Locations (continued)

** Functions not present in the 80C52 are in bold.*

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
TL2									CCh
TH2									CDh
PSW	CY	AC	F0	RS1	RS0	OV	FL	P	D0h
WDCON	**SMOD_1**	**POR**	**EPFI**	**PFI**	**WDIF**	**WTRF**	**EWT**	**RWT**	D8h
ACC									E0h
EIE	—	—	**ERTCI**	**EWDI**	**EX5**	**EX4**	**EX3**	**EX2**	E8h
B									F0h
RTASS									F2h
RTAS	0	0							F3h
RTAM	0	0							F4h
RTAH	0	0	0						F5h
EIP	—	—	**PRTCI**	**PWDI**	**PX5**	**PX4**	**PX3**	**PX2**	F8h
RTCC	**SSCE**	**SCE**	**MCE**	**HCE**	**RTCRE**	**RTCWE**	**RTCIF**	**RTCE**	F9h
RTCSS									FAh
RTCS	0	0							FBh
RTCM	0	0							FCh
RTCH									FDh
RTCD0									FEh
RTCD1									FFh

NONVOLATILE FUNCTIONS

The DS87C530/DS83C530 provide two functions that are permanently powered if a user supplies an external energy source. These are an on-chip RTC and a nonvolatile SRAM. The chip contains all related functions and controls. The user must supply a backup source and a 32.768kHz timekeeping crystal.

REAL-TIME CLOCK

The on-chip RTC keeps time of day and calendar functions. Its time base is a 32.768kHz crystal between pins RTCX1 and RTCX2. The RTC maintains time to 1/256 of a second. It also allows a user to read (and write) seconds, minutes, hours, day of the week, and date. Figure 2 shows the clock organization.

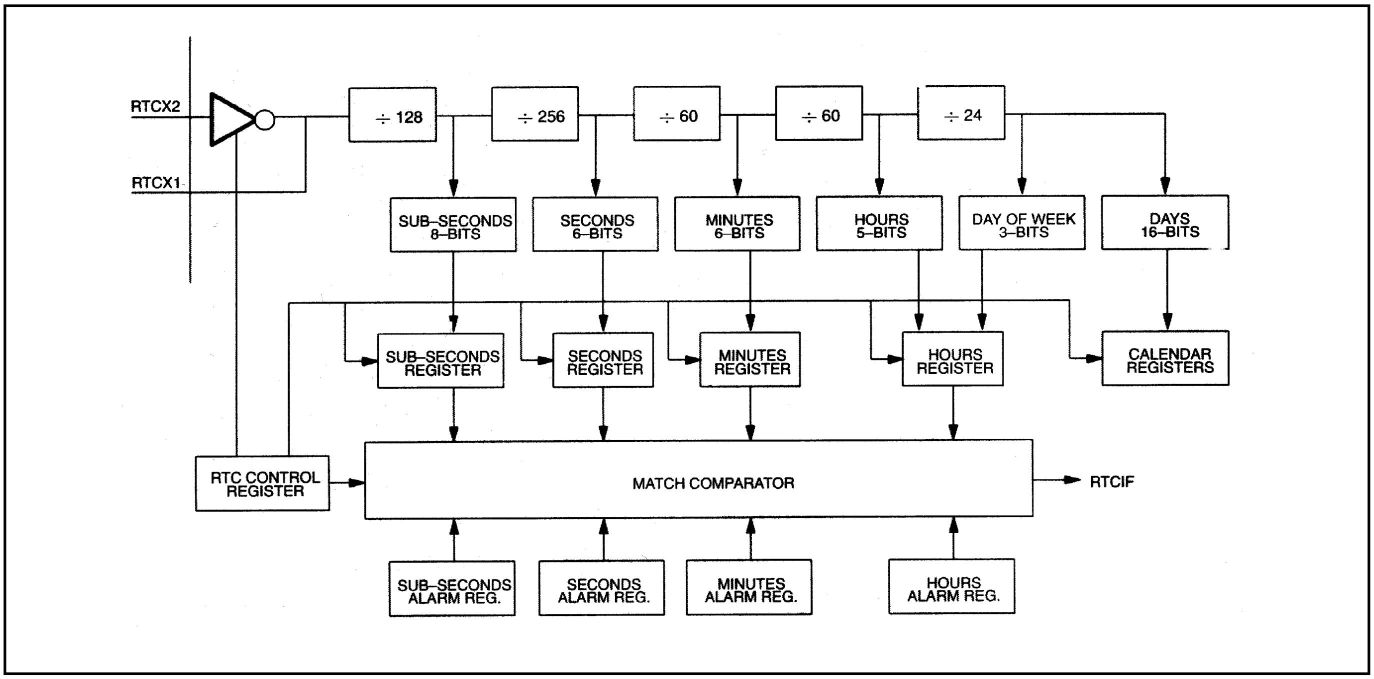
Timekeeping registers allow easy access to commonly needed time values. For example, software can simply check the elapsed number of minutes by reading one register. Alternately, it can read the complete time of day, including subseconds, in only four registers. The calendar stores its data in binary form. While this requires software translation, it allows complete flexibility as to the exact value. A user can start the calendar with a variety of selections since it is simply a 16-bit binary number of days. This number allows a total range of 179 years beginning from 0000.

The RTC features a programmable alarm condition. A user selects the alarm time. When the RTC reaches the selected value, it sets a flag. This will cause an interrupt if enabled, even in Stop mode. The alarm consists of a comparator that matches the user value against the RTC actual value. A user can select a match for 1 or more of the sub-seconds, seconds, minutes, or hours. This allows an interrupt automatically to occur once per second, once per minute, once per hour, or once per day. Enabling interrupts with no match will generate an interrupt 256 times per second.

Software enables the timekeeper oscillator using the RTC enable bit in the RTC Control register (F9h). This starts the clock. It can disable the oscillator to preserve the life of the backup energy-source if unneeded. Values in the RTC Control register are maintained by the backup source through power failure. Once enabled, the RTC maintains time for the life of the backup source even when V_{CC} is removed.

The RTC will maintain an accuracy of ±2 minutes per month at 25°C. Under no circumstances are negative voltages, of any amplitude, allowed on any pin while the device is in data retention mode ($V_{CC} < V_{BAT}$). Negative voltages will shorten battery life, possibly corrupting the contents of internal SRAM and the RTC.

Figure 2. Real-Time Clock



NONVOLATILE RAM

The 1k x 8 on-chip SRAM can be nonvolatile if an external backup energy source is used. This allows the device to log data or to store configuration settings. Internal switching circuits will detect the loss of V_{CC} and switch SRAM power to the backup source on the V_{BAT} pin. The 256 bytes of direct RAM are not affected by this circuit and are volatile.

CRYSTAL AND BACKUP SOURCES

To use the unique functions of the DS87C530/DS83C530, a 32.768kHz timekeeping crystal and a backup energy source are needed. The following describes guidelines for choosing these devices.

Timekeeping Crystal

The DS87C530/DS83C530 can use a standard 32.768kHz crystal as the RTC time base. There are two versions of standard crystals available, with 6pF and 12.5pF load capacitance. The tradeoff is that the 6pF uses less power, giving longer life while V_{CC} is off, but is more sensitive to noise and board layout. The

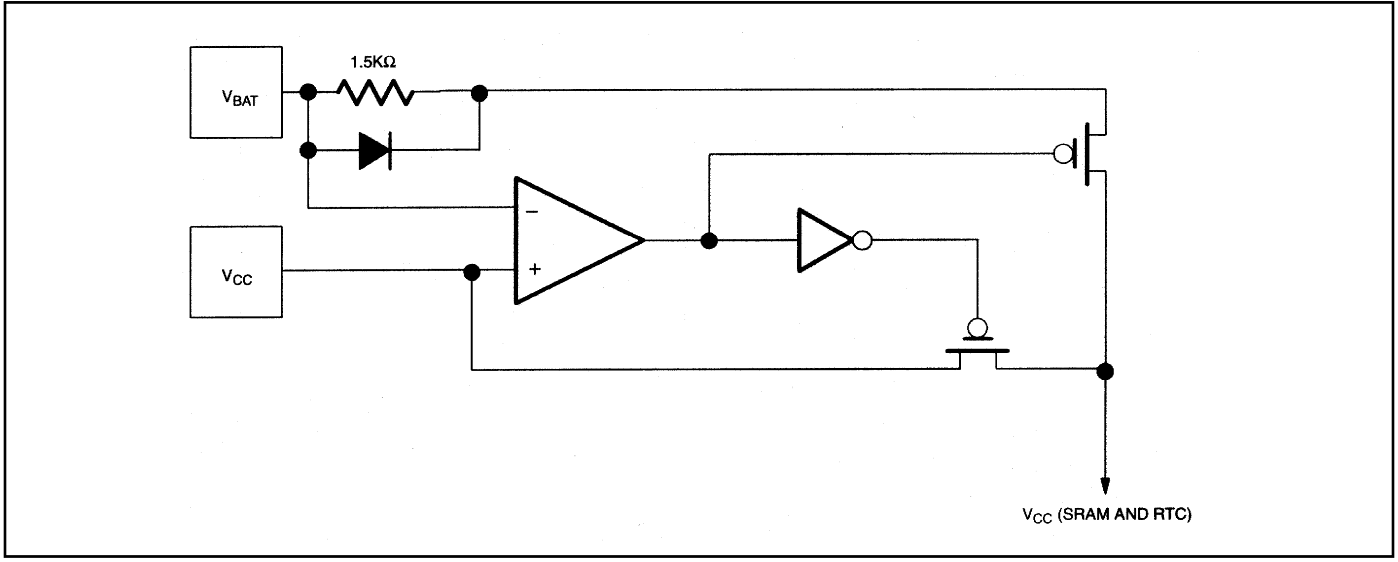
12.5pF crystal uses more power, giving a shorter battery backed life, but produces a more robust oscillator. Bit 6 in the RTC Trim register (TRIM; 96h) must be programmed to specify the crystal type for the oscillator. When TRIM.6 = 1, the circuit expects a 12.5pF crystal. When TRIM.6 = 0, it expects a 6pF crystal. This bit will be nonvolatile so these choices will remain while the backup source is present. A guard ring (connected to the RTC ground) should encircle the RTCX1 and RTCX2 pins.

Backup Energy Source

The DS87C530/DS83C530 use an external energy source to maintain timekeeping and SRAM data without V_{CC}. This source can be either a battery or 0.47F super cap and should be connected to the V_{BAT} pin. The nominal battery voltage is 3V. The V_{BAT} pin will not source current. Therefore, a super cap requires an external resistor and diode to supply charge.

The backup lifetime is a function of the battery capacity and the data retention current drain. This drain is specified in the electrical specifications. The circuit loads the V_{BAT} only when V_{CC} has fallen below V_{BAT}. Thus the actual lifetime depends not only on the current and battery capacity, but also on the portion of time without power. A very small lithium cell provides a lifetime of more than 10 years.

Figure 3. Internal Backup Circuit



IMPORTANT APPLICATION NOTE

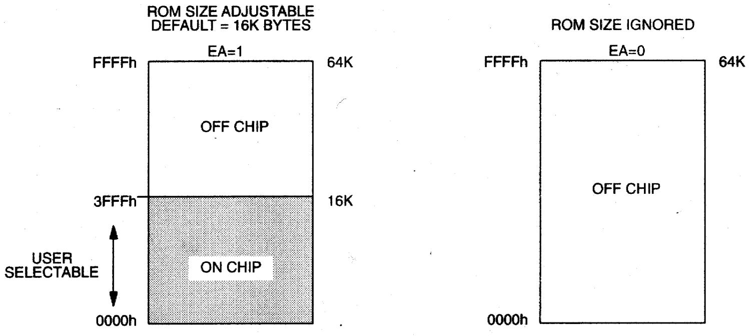
The pins on the DS87C530/DS83C530 are generally as resilient as other CMOS circuits. They have no unusual susceptibility to electrostatic discharge (ESD) or other electrical transients. **However, no pin on the DS87C530/DS83C530 should ever be taken to a voltage below ground.** Negative voltages on any pin can turn on internal parasitic diodes that draw current directly from the battery. If a device pin is connected to the "outside world" where it may be handled or come in contact with electrical noise, protection should be added to prevent the device pin from going below -0.3V. Some power supplies can give a small undershoot on power-up, which should be prevented. *Application Note 93: Design Guidelines for Microcontrollers Incorporating NV RAM* discusses how to protect the DS87C530/DS83C530 against these conditions.

MEMORY RESOURCES

Like the 8051, the DS87C530/DS83C530 use three memory areas. The total memory configuration of the device is 16kB of ROM, 1kB of data SRAM and 256 bytes of scratchpad or direct RAM. The 1kB of data device will immediately jump to external program execution because program code from 4kB to 16kB (1000h–3FFFh) is no longer located on-chip. This could result in code misalignment and execution of an invalid instruction. The recommended method is to modify the ROMSIZE register from a location in memory that will be internal (or external) both before and after the operation. In the above example, the instruction which modifies the ROMSIZE register should be located below the 4kB (1000h) boundary, so that it will be unaffected by the memory modification. The same precaution should be applied if the internal program memory size is modified while executing from external program memory.

Off-chip memory is accessed using the multiplexed address/data bus on P0 and the MSB address on P2. While serving as a memory bus, these pins are not I/O ports. This convention follows the standard 8051 method of expanding on-chip memory. Off-chip ROM access also occurs if the $\overline{\text{EA}}$ pin is a logic 0. $\overline{\text{EA}}$ overrides all bit settings. The $\overline{\text{PSEN}}$ signal will go active (low) to serve as a chip enable or output enable when Ports 0 and 2 fetch from external ROM.

Figure 4. ROM Memory Map



DATA MEMORY ACCESS

Unlike many 8051 derivatives, the DS87C530/DS83C530 contain on-chip data memory. The devices also contain the standard 256 bytes of RAM accessed by direct instructions. These areas are separate. The MOVX instruction accesses the on-chip data memory. Although physically on-chip, software treats this area as though it was located off-chip. The 1kB of SRAM is between address 0000h and 03FFh.

Access to the on-chip data RAM is optional under software control. When enabled by software, the data SRAM is between 0000h and 03FFh. Any MOVX instruction that uses this area will go to the on-chip RAM while enabled. MOVX addresses greater than 03FFh automatically go to external memory through Ports 0 and 2.

When disabled, the 1kB memory area is transparent to the system memory map. Any MOVX directed to the space between 0000h and FFFFh goes to the expanded bus on Ports 0 and 2. This also is the default condition. This default allows the DS87C530/DS83C530 to drop into an existing system that uses these addresses for other hardware and still have full compatibility.

The on-chip data area is software selectable using 2 bits in the Power Management Register at location C4h. This selection is dynamically programmable. Thus access to the on-chip area becomes transparent to reach off-chip devices at the same addresses. The control bits are DME1 (PMR.1) and DME0 (PMR.0). They have the following operation:

Table 2. Data Memory Access Control

DME1	DME0	DATA MEMORY ADDRESS	MEMORY FUNCTION
0	0	0000h–FFFFh	External Data Memory (*default condition)*
0	1	0000h–03FFh	Internal SRAM Data Memory
		0400h–FFFFh	External Data Memory
1	0	Reserved	Reserved
1	1	0000h–03FFh	Internal SRAM Data Memory
		0400h–FFFBh	Reserved—no external access
		FFFCh	Read access to the status of lock bits
		FFFDh–FFFh	Reserved—no external access

Notes on the status byte read at FFFCh with DME1, 0 = 1, 1: Bits 2-0 reflect the programmed status of the security lock bits LB2–LB0. They are individually set to a logic 1 to correspond to a security lock bit that has been programmed. These status bits allow software to verify that the part has been locked before running if desired. The bits are read-only.

Note: After internal MOVX SRAM has been initialized, changing bits DEM0/1 has no effect on the contents of the SRAM.

STRETCH MEMORY CYCLE

The DS87C530/DS83C530 allow software to adjust the speed of off-chip data memory access. The microcontrollers can perform the MOVX in as few as two instruction cycles. The on-chip SRAM uses this speed and any MOVX instruction directed internally uses two cycles. However, the time can be stretched for interface to external devices. This allows access to both fast memory and slow memory or peripherals with no glue logic. Even in high-speed systems, it may not be necessary or desirable to perform off-chip data memory access at full speed. In addition, there are a variety of memory-mapped peripherals such as LCDs or UARTs that are slow.

The Stretch MOVX is controlled by the Clock Control Register at SFR location 8Eh as described below. It allows the user to select a Stretch value between 0 and 7. A Stretch of 0 will result in a two-machine cycle MOVX. A Stretch of 7 will result in a MOVX of nine machine cycles. Software can dynamically change this value depending on the particular memory or peripheral.

On reset, the Stretch value will default to a 1, resulting in a three-cycle MOVX for any external access. Therefore, off-chip RAM access is not at full speed. This is a convenience to existing designs that may not have fast RAM in place. Internal SRAM access is always at full speed regardless of the Stretch setting. When desiring maximum speed, software should select a Stretch value of 0. When using very slow RAM or peripherals, select a larger Stretch value. Note that this affects data memory only and the only way to slow program memory (ROM) access is to use a slower crystal.

Using a Stretch value between 1 and 7 causes the microcontroller to stretch the read/write strobe and all related timing. Also, setup and hold times are increased by 1 clock when using any Stretch greater than 0. This results in a wider read/write strobe and relaxed interface timing, allowing more time for memory/peripherals to respond. The timing of the variable speed MOVX is in the *Electrical Specifications* section. Table 3 shows the resulting strobe widths for each Stretch value. The memory Stretch uses the Clock Control Special Function Register at SFR location 8Eh. The Stretch value is selected using bits CKCON.2–0. In the table, these bits are referred to as M2 through M0. The first Stretch (default) allows the use of common 120ns RAMs without dramatically lengthening the memory access.

Table 3. Data Memory Cycle Stretch Values

CKCON.2–0			MEMORY CYCLES	$\overline{\text{RD}}$ OR $\overline{\text{WR}}$ STROBE WIDTH IN CLOCKS	STROBE WIDTH TIME AT 33MHz (ns)
M2	**M1**	**M0**			
0	0	0	2 (forced internal)	2	60
0	0	1	3 (default external)	4	121
0	1	0	4	8	242
0	1	1	5	12	364
1	0	0	6	16	485
1	0	1	7	20	606
1	1	0	8	24	727
1	1	1	9	28	848

DUAL DATA POINTER

The timing of block moves of data memory is faster using the Dual Data Pointer (DPTR). The standard 8051 DPTR is a 16-bit value that is used to address off-chip data RAM or peripherals. In the DS87C530/DS83C530, the standard data pointer is called DPTR, located at SFR addresses 82h and 83h. These are the standard locations. Using DPTR requires no modification of standard code. The new DPTR at SFR 84h and 85h is called DPTR1. The DPTR Select bit (DPS) chooses the active pointer. Its location is the lsb of the SFR location 86h. No other bits in register 86h have any effect and are 0. The user switches between data pointers by toggling the lsb of register 86h. The increment (INC) instruction is the fastest way to accomplish this. All DPTR-related instructions use the currently selected DPTR for any activity. Therefore it takes only one instruction to switch from a source to a destination address. Using the Dual Data Pointer saves code from needing to save source and destination addresses when doing a block move. The software simply switches between DPTR and 1 once software loads them. The relevant register locations are as follows.

DPL	82h	Low byte original DPTR
DPH	83h	High byte original DPTR
DPL1	84h	Low byte new DPTR
DPH1	85h	High byte new DPTR
DPS	86h	DPTR Select (lsb)

POWER MANAGEMENT

Along with the standard Idle and power-down (Stop) modes of the standard 80C52, the DS87C530/DS83C530 provide a new Power Management Mode. This mode allows the processor to continue functioning, yet to save power compared with full operation. The DS87C530/DS83C530 also feature several enhancements to Stop mode that make it more useful.

POWER MANAGEMENT MODE (PMM)

Power Management Mode offers a complete scheme of reduced internal clock speeds that allow the CPU to run software but to use substantially less power. During default operation, the DS87C530/DS83C530 use four clocks per machine cycle. Thus the instruction cycle rate is (Clock/4). At 33MHz crystal speed, the instruction cycle speed is 8.25MHz (33/4). In PMM, the microcontroller continues to operate but uses an internally divided version of the clock source. This creates a lower power state without external components. It offers a choice of two reduced instruction cycle speeds (and two clock sources - discussed below). The speeds are (Clock/64) and (Clock/1024).

Software is the only mechanism to invoke the PMM. Table 4 illustrates the instruction cycle rate in PMM for several common crystal frequencies. Since power consumption is a direct function of operating speed, PMM 1 eliminates most of the power consumption while still allowing a reasonable speed of processing. PMM 2 runs very slowly and provides the lowest power consumption without stopping the CPU. This is illustrated in Table 5.

Note that PMM provides a lower power condition than Idle mode. This is because in Idle, all clocked functions such as timers run at a rate of crystal divided by 4. Since wake-up from PMM is as fast as or faster than from Idle and PMM allows the CPU to operate (even if doing NOPs), there is little reason to use Idle mode in new designs.

Table 4. Machine Cycle Rate

CRYSTAL SPEED (MHz)	FULL OPERATION (4 CLOCKS) (MHz)	PMM1 (64 CLOCKS) (kHz)	PMM2 (1024 CLOCKS) (kHz)
11.0592	2.765	172.8	10.8
16	4.00	250.0	15.6
25	6.25	390.6	24.4
33	8.25	515.6	32.2

Table 5. Typical Operating Current in PMM

CRYSTAL SPEED (MHz)	FULL OPERATION (4 CLOCKS) (mA)	PMM1 (64 CLOCKS) (mA)	PMM2 (1024 CLOCKS) (mA)
11.0592	13.1	5.3	4.8
16	17.2	6.4	5.6
25	25.7	8.1	7.0
33	32.8	9.8	8.2

Table 6. PMM Control and Status Bit Summary

NAME	LOCATION	FUNCTION	RESET	WRITE ACCESS
XT/$\overline{\text{RG}}$	EXIF.3	Control. XT/$\overline{\text{RG}}$ =1, runs from crystal or external clock; XT/$\overline{\text{RG}}$ =0, runs from internal ring oscillator.	X	0 to 1 only when XTUP = 1 and XTOFF= 0
RGMD	EXIF.2	Status. RGMD=1, CPU clock = ring; RGMD = 0, CPU clock = crystal.	0	None
CD1, CD0	PMR7, PMR.6	Control. CD1, 0 = 01, 4 clocks; CS1, 0 = 10, PMM1; CD1, 0 = 11, PMM2.	0, 1	Write CD1, 0 = 10 or 11 only from CD1, 0 = 01
SWB	PMR.5	Control. SWB = 1, hardware invokes switchback to 4 clocks, SWB = 0, no hardware switchback.	0	Unrestricted
XTOFF	PMR.3	Control. Disables crystal operation after ring is selected.	0	1 only when XT/$\overline{\text{RG}}$ = 0
PIP	STATUS.7	Status. 1 indicates a power-fail interrupt in service.	0	None
HIP	STATUS.6	Status. 1 indicates high priority interrupt in service.	0	None
LIP	STATUS.5	Status. 1 indicates low priority interrupt in service.	0	None
XTUP	STATUS.4	Status. 1 indicates that the crystal has stabilized.	1	None
SPTA1	STATUS.3	Status. Serial transmission on serial port 1.	0	None
SPRA1	STATUS.2	Status. Serial word reception on serial port 1.	0	None
SPTA0	STATUS.1	Status. Serial transmission on serial port 0.	0	None
SPRA0	STATUS.0	Status. Serial word reception on serial port 0.	0	None

IDLE MODE

Setting the lsb of the Power Control register (PCON; 87h) invokes the Idle mode. Idle will leave internal clocks, serial ports and timers running. Power consumption drops because the CPU is not active. Since clocks are running, the Idle power consumption is a function of crystal frequency. It should be approximately one-half the operational power at a given frequency. The CPU can exit the Idle state with any interrupt or a reset. Idle is available for backward software compatibility. The system can now reduce power consumption to below Idle levels by using PMM1 or PMM2 and running NOPs.

STOP MODE ENHANCEMENTS

Setting bit 1 of the Power Control register (PCON; 87h) invokes the Stop mode. Stop mode is the lowest power state since it turns off all internal clocking. The I_{CC} of a standard Stop mode is approximately 1 μA but is specified in the Electrical Specifications. The CPU will exit Stop mode from an external interrupt or a reset condition. Internally generated interrupts (timer, serial port, watchdog) are not useful since they require clocking activity. One exception is that a RTC interrupt can cause the device to exit Stop mode. This provides a very power efficient way of performing infrequent yet periodic tasks.

The DS87C530/DS83C530 provide two enhancements to the Stop mode. As documented below, the device provides a bandgap reference to determine Power-fail Interrupt and Reset thresholds. The default state is that the bandgap reference is off while in Stop mode. This allows the extremely low-power state mentioned above. A user can optionally choose to have the bandgap enabled during Stop mode. With the bandgap reference enabled, PFI and Power-fail Reset are functional and are a valid means for leaving Stop mode. This allows software to detect and compensate for a brownout or power supply sag, even when in Stop mode.

In Stop mode with the bandgap enabled, I_{CC} will be approximately 50μA compared with 1μA with the bandgap off. If a user does not require a Power-fail Reset or Interrupt while in Stop mode, the bandgap can remain disabled. Only the most power sensitive applications should turn off the bandgap, as this results in an uncontrolled power-down condition.

The control of the bandgap reference is located in the Extended Interrupt Flag register (EXIF; 91h). Setting BGS (EXIF.0) to a 1 will keep the bandgap reference enabled during Stop mode. The default or reset condition is with the bit at a logic 0. This results in the bandgap being off during Stop mode. Note that this bit has no control of the reference during full power, PMM, or Idle modes.

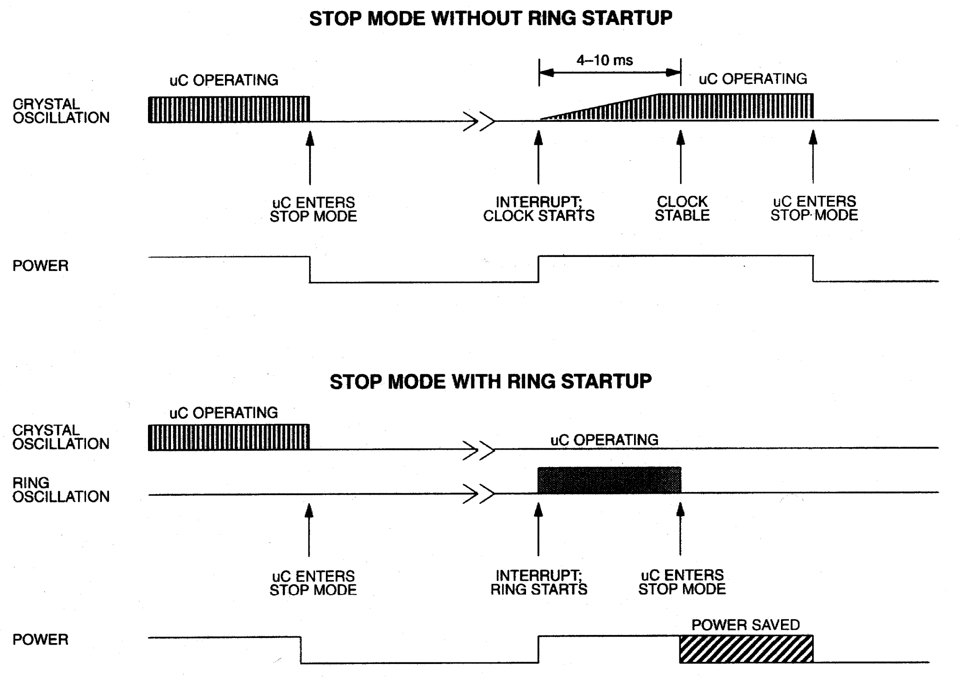
The second feature allows an additional power saving option while also making Stop easier to use. This is the ability to start instantly when exiting Stop mode. It is the internal ring oscillator that provides this feature. This ring can be a clock source when exiting Stop mode in response to an interrupt. The benefit of the ring oscillator is as follows.

Using Stop mode turns off the crystal oscillator and all internal clocks to save power. This requires that the oscillator be restarted when exiting Stop mode. Actual startup time is crystal-dependent, but is normally at least 4ms. A common recommendation is 10ms. In an application that will wake up, perform a short operation, then return to sleep, the crystal startup can be longer than the real transaction. However, the ring oscillator will start instantly. Running from the ring, the user can perform a simple operation and return to sleep before the crystal has even started. If a user selects the ring to provide the startup clock and the processor remains running, hardware will automatically switch to the crystal once a power-on reset interval (65,536 clocks) has expired. Hardware uses this value to assure proper crystal start even though power is not being cycled.

The ring oscillator runs at approximately 2MHz to 4MHz but will not be a precise value. Do not conduct real-time precision operations (including serial communication) during this ring period. Figure 6 shows how the operation would compare when using the ring, and when starting up normally. The default state is to exit Stop mode without using the ring oscillator.

The RGSL ring-select bit at EXIF.1 (EXIF; 91h) controls this function. When RGSL = 1, the CPU will use the ring oscillator to exit Stop mode quickly. As mentioned above, the processor will automatically switch from the ring to the crystal after a delay of 65,536 crystal clocks. For a 3.57MHz crystal, this is approximately 18ms. The processor sets a flag called RGMD- Ring Mode, located at EXIF.2, that tells software that the ring is being used. The bit will be a logic 1 when the ring is in use. Attempt no serial communication or precision timing while this bit is set, since the operating frequency is not precise.

Figure 6. Ring Oscillator Exit from Stop Mode



NOTE: DIAGRAM ASSUMES THAT THE OPERATION FOLLOWING STOP REQUIRES LESS THAN 18ms TO COMPLETE.

EMI REDUCTION

One of the major contributors to radiated noise in an 8051-based system is the toggling of ALE. The DS87C530/DS83C530 allow software to disable ALE when not used by setting the ALEOFF (PMR.2) bit to 1. When ALEOFF = 1, ALE will still toggle during an off-chip MOVX. However, ALE will remain in a static when performing on-chip memory access. The default state of ALEOFF = 0 so ALE toggles with every instruction cycle.

PERIPHERAL OVERVIEW

The DS87C530/DS83C530 provide several of the most commonly needed peripheral functions in microcomputer-based systems. These new functions include a second serial port, power-fail reset, Power-fail interrupt, and a programmable watchdog timer. These are described below, and more details are available in the *High-Speed Microcontroller User's Guide*.

SERIAL PORTS

The DS87C530/DS83C530 provide a serial port (UART) that is identical to the 80C52. In addition it includes a second hardware serial port that is a full duplicate of the standard one. This port optionally uses pins P1.2 (RXD1) and P1.3 (TXD1). It has duplicate control functions included in new SFR locations.

Both ports can operate simultaneously but can be at different baud rates or even in different modes. The second serial port has similar control registers (SCON1; C0h, SBUF1; C1h) to the original. The new serial port can only use Timer 1 for timer-generated baud rates.

TIMER RATE CONTROL

There is one important difference between the DS87C530/DS83C530 and 8051 regarding timers. The original 8051 used 12 clocks per cycle for timers as well as for machine cycles. The DS87C530/DS83C530 architecture normally uses 4 clocks per machine cycle. However, in the area of timers and serial ports, the DS87C530/DS83C530 will default to 12 clocks per cycle on reset. This allows existing code with real-time dependencies such as baud rates to operate properly.

If an application needs higher speed timers or serial baud rates, the user can select individual timers to run at the 4-clock rate. The Clock Control register (CKCON; 8Eh) determines these timer speeds. When the relevant CKCON bit is logic 1, the DS87C530/DS83C530 use 4 clocks per cycle to generate timer speeds. When the bit is a 0, the DS87C530 uses 12 clocks for timer speeds. The reset condition is a 0. CKCON.5 selects the speed of Timer 2. CKCON.4 selects Timer 1 and CKCON.3 selects Timer 0. Unless a user desires very fast timing, it is unnecessary to alter these bits. Note that the timer controls are independent.

POWER-FAIL RESET

The DS87C530/DS83C530 use a precision bandgap voltage reference to decide if V_{CC} is out of tolerance. While powering up, the internal monitor circuit maintains a reset state until V_{CC} rises above the V_{RST} level. Once above this level, the monitor enables the crystal oscillator and counts 65,536 clocks. It then exits the reset state. This power-on reset (POR) interval allows time for the oscillator to stabilize.

A system needs no external components to generate a power-related reset. Anytime V_{CC} drops below V_{RST}, as in power failure or a power drop, the monitor will generate and hold a reset. It occurs automatically, needing no action from the software. Refer to the *Electrical Specifications* section for the exact value of V_{RST}.

POWER-FAIL INTERRUPT

The voltage reference that sets a precise reset threshold also generates an optional early warning power-fail interrupt (PFI). When enabled by software, the processor will vector to program memory address 0033h if V_{CC} drops below V_{PFW}. PFI has the highest priority. The PFI enable is in the Watchdog Control SFR (WDCON–D8h). Setting WDCON.5 to logic 1 will enable the PFI. Application software can also

DS83C530 ROM Verification

The DS83C530 memory contents can be verified using a standard EPROM programmer. The memory address to be verified is placed on the pins shown in Figure 7, and the programming control pins are set to the levels shown in Table 9. The data at that location is then asserted on port 0.

DS83C530 Signature

The Signature bytes identify the DS83C530 to EPROM programmers. This information is at programming addresses 30h, 31h, and 60h. Because Mask ROM devices are not programmed in device programmers, most designers will find little use for the feature, and it is included only for compatibility.

ADDRESS	VALUE	MEANING
30h	DAh	Manufacturer
31h	31h	Model
60h	01h	Extension

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……………………………………………………….-0.3V to (V_{CC} + 0.5V)
Voltage Range on V_{CC} Relative to Ground……………………………………………………………….-0.3V to +6.0V
Operating Temperature Range……………………………………………………………………………0°C to +70°C
Storage Temperature Range…………………………………………………………………...-55°C to +125°C (Note 1)
Soldering Temperature.…………………………………………………………See IPD/JEDEC J-STD-020 Specification

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, T_A = -40°C to +85°C.) (Note 2)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	3
Power-Fail Warning	V_{PFW}	4.25	4.38	4.5	V	3
Minimum Operating Voltage	V_{RST}	4.0	4.13	4.25	V	3
Backup Battery Voltage	V_{BAT}	2.5	3.0	V_{CC}-0.7	V	
Supply Current Active Mode at 33MHz	I_{CC}		30	46	mA	4
Supply Current Idle Mode at 33MHz	I_{Idle}		15	25	mA	5
Supply Current Stop Mode, Bandgap Disabled (0°C to +70°C)	I_{Stop}		1	100	µA	6
Supply Current Stop Mode, Bandgap Disabled (-40°C to +85°C)			1	150	µA	6
Supply Current Stop Mode, Bandgap Enabled (0°C to +70°C)	I_{SPBG}		50	170	µA	6
Supply Current Stop Mode, Bandgap Enabled (-40°C to +85°C)			50	195	µA	6
Backup Supply Current, Data-Retention Mode (0°C to +70°C)	I_{BAT}	0		0.5	µA	7
Backup Supply Current, Data-Retention Mode (-40°C to +85°C)		0		1	µA	7
Input Low Level	V_{IL}	-0.3		+0.8	V	3
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	3
Input High Level XTAL1 and RST	V_{IH2}	3.5		V_{CC}+0.3	V	3
Output Low Voltage at I_{OL} = 1.6mA	V_{OL1}		0.15	0.45	V	3
Output Low Voltage Ports 0, 2, ALE, and $\overline{PSEN}$ at I_{OL} = 3.2mA	V_{OL2}		0.15	0.45	V	3
Output High Voltage Ports 1, 2, 3, ALE, $\overline{PSEN}$ at I_{OH} = -50µA	V_{OH1}	2.4			V	3, 8
Output High Voltage Ports 1, 2, 3 at I_{OH} = -1.5mA	V_{OH2}	2.4			V	3, 9
Output High Voltage Port 0 in Bus Mode I_{OH} = -8mA	V_{OH3}	2.4			V	3, 10
Input Low Current Ports 1, 2, 3 at 0.45V	I_{IL}			-70	µA	11
Transition Current from 1 to 0 Ports 1, 2, 3 at 2V	I_{TL}			-800	µA	12

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.5V to 5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Port 0, $\overline{EA}$, Pins, I/O Mode	I_L	-10		+10	μA	13
Input Leakage Port 0, Bus Mode	I_L	-300		+300	μA	14
RST Pulldown Resistance	R_{RST}	50		200	kΩ	

Note 1: Storage temperature is defined as the temperature of the device when V_{CC} = 0V and V_{BAT} = 0V. In this state, the contents of SRAM are not battery backed and are undefined.

Note 2: All parameters apply to both commercial and industrial temperature operation unless otherwise noted.

Note 3: All voltages are referenced to ground.

Note 4: Active current measured with 33MHz clock source on XTAL1, V_{CC} = RST = 5.5V, other pins disconnected.

Note 5: Idle mode current measured with 33MHz clock source on XTAL1, V_{CC} = 5.5V, RST at ground, other pins disconnected.

Note 6: Stop mode current measured with XTAL1 and RST grounded, V_{CC} = 5.5V, all other pins disconnected.

Note 7: V_{CC} = 0V, V_{BAT} = 3.3V. 32.768kHz crystal with 12.5pF load capacitance between RTCX1 and RTCX2 pins. RTCE bit set to 1.

Note 8: RST = V_{CC}. This condition mimics operation of pins in I/O mode. Port 0 is tri-stated in reset and when at a logic high state during I/O mode.

Note 9: During a 0-to-1 transition, a one-shot drives the ports hard for two clock cycles. This measurement reflects port in transition mode.

Note 10: When addressing external memory. This specification only applies to the first clock cycle following the transition.

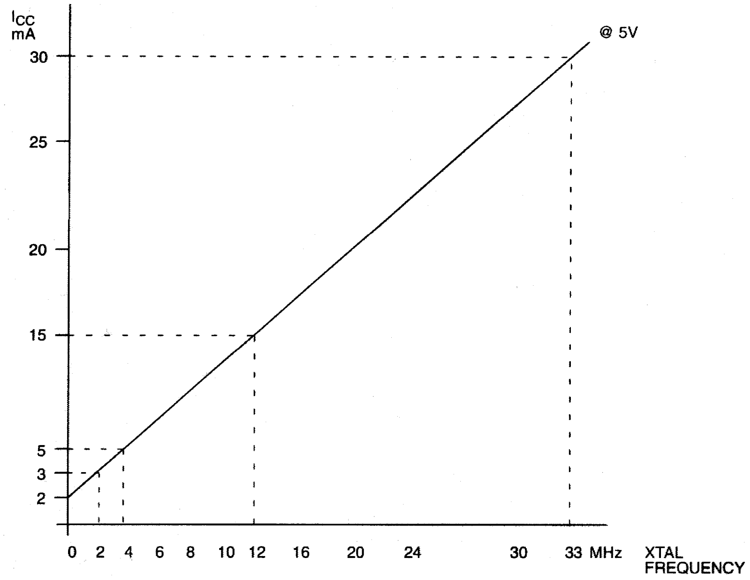
Note 11: This is the current required from an external circuit to hold a logic low level on an I/O pin while the corresponding port latch bit is set to 1. This is only the current required to *hold* the low level; transitions from 1 to 0 on an I/O pin will also have to overcome the transition current.

Note 12: Ports 1, 2, and 3 source transition current when being pulled down externally. It reaches its maximum at approximately 2V.

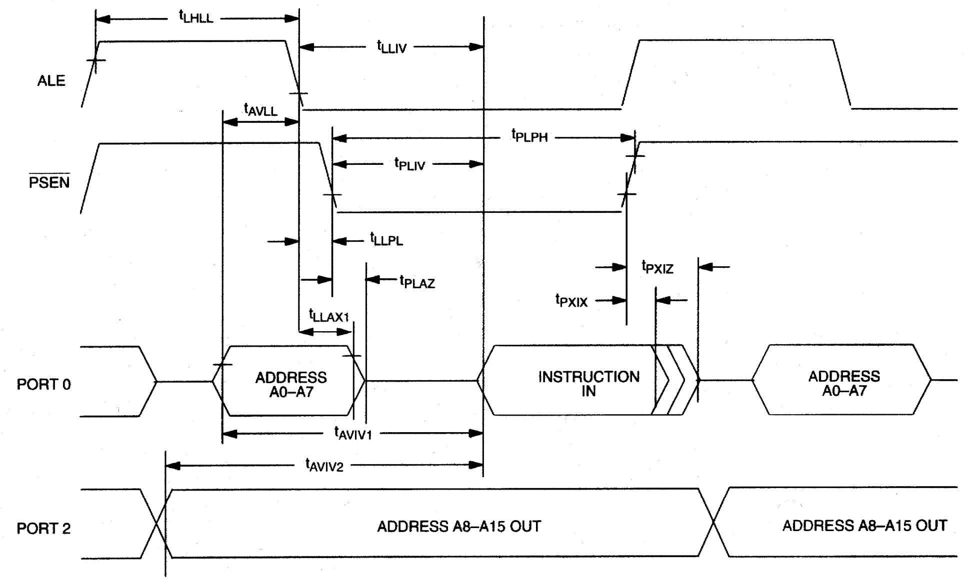
Note 13: 0.45 < V_{IN} < V_{CC}. RST = V_{CC}. This condition mimics operation of pins in I/O mode.

Note 14: 0.45 < V_{IN} < V_{CC}. Not a high-impedance input. This port is a weak address holding latch in Bus Mode. Peak current occurs near the input transition point of the latch, approximately 2V.

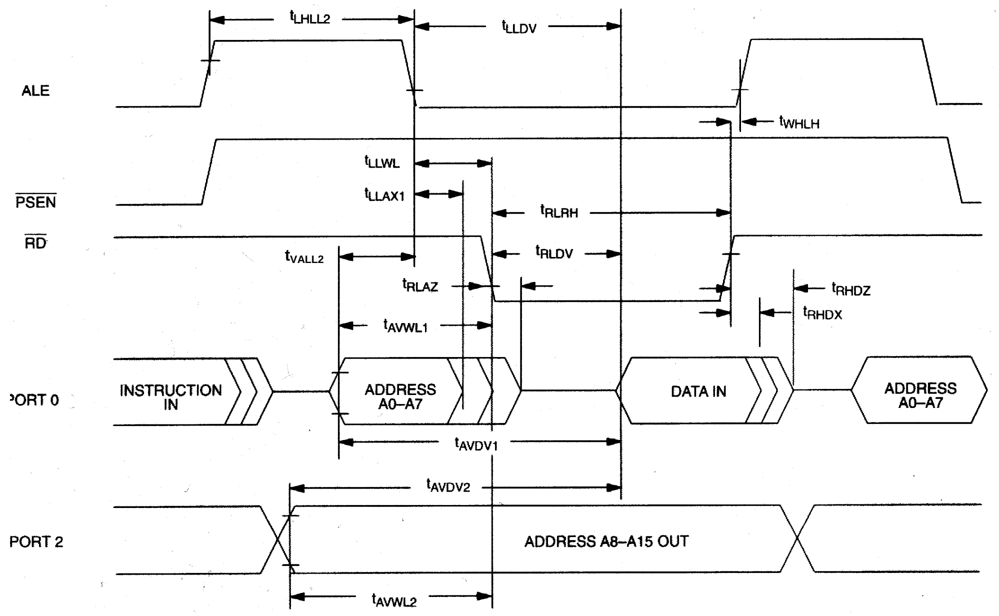
TYPICAL I_{CC} vs. FREQUENCY



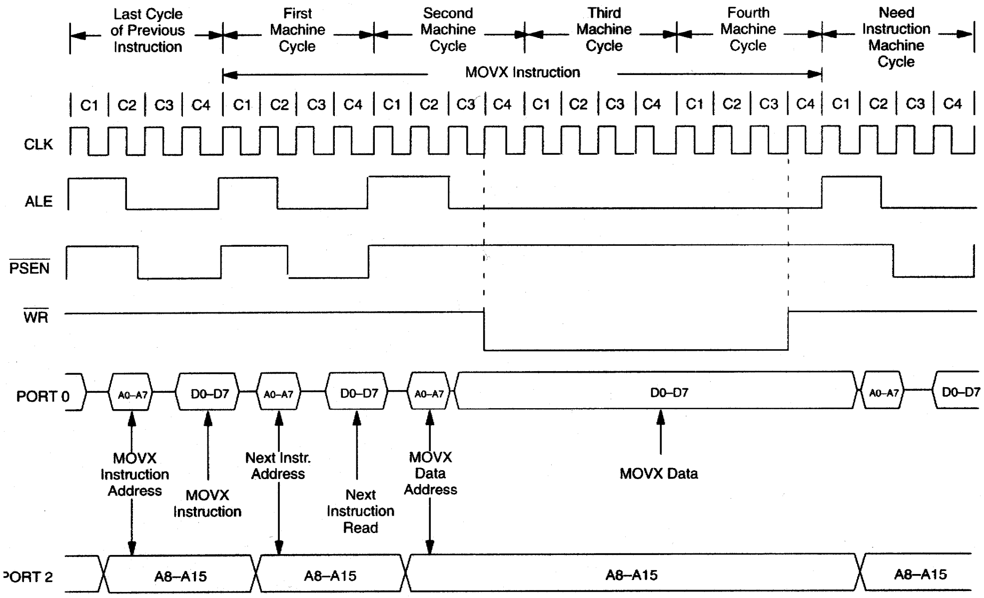
EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE

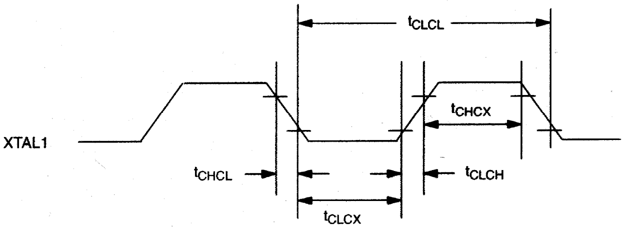


DATA MEMORY WRITE WITH STRETCH = 2



FOUR CYCLE DATA MEMORY WRITE
STRETCH VALUE=2

EXTERNAL CLOCK DRIVE



PACKAGE INFORMATION

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
52 TQFP	C52+2	**21-0295**
52 CQUAD	K52-1	**21-0383**
52 PLCC	Q52+1	**21-0049**