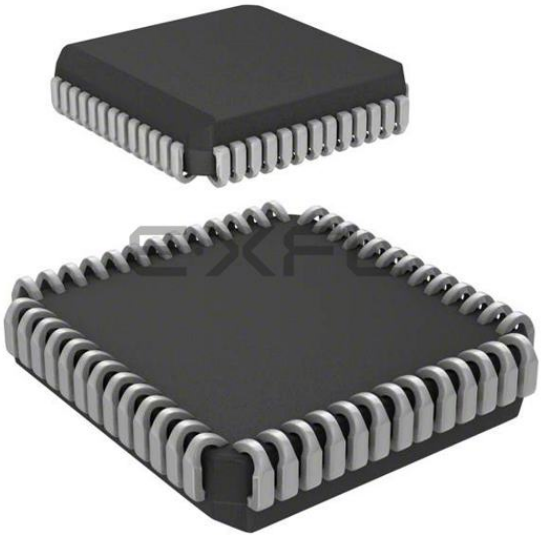
Analog Devices Inc./Maxim Integrated - DS87C530-QCL+ Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	33MHz
Connectivity	EBI/EMI, SIO, UART/USART
Peripherals	Power-Fail Reset, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LCC (J-Lead)
Supplier Device Package	52-PLCC (19.13x19.13)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds87c530-qcl

DETAILED DESCRIPTION

The DS87C530/DS83C530 EPROM/ROM microcontrollers with a real-time clock (RTC) are 8051-compatible microcontrollers based on the Dallas Semiconductor high-speed core. They use 4 clocks per instruction cycle instead of the 12 used by the standard 8051. They also provide a unique mix of peripherals not widely available on other processors. They include an on-chip RTC and battery backup support for an on-chip 1k x 8 SRAM. The new Power Management Mode allows software to select reduced power operation while still processing.

A combination of high-performance microcontroller core, RTC, battery-backed SRAM, and power management makes the DS87C530/DS83C530 ideal for instruments and portable applications. They also provide several peripherals found on other Dallas high-speed microcontrollers. These include two independent serial ports, two data pointers, on-chip power monitor with brownout detection and a watchdog timer.

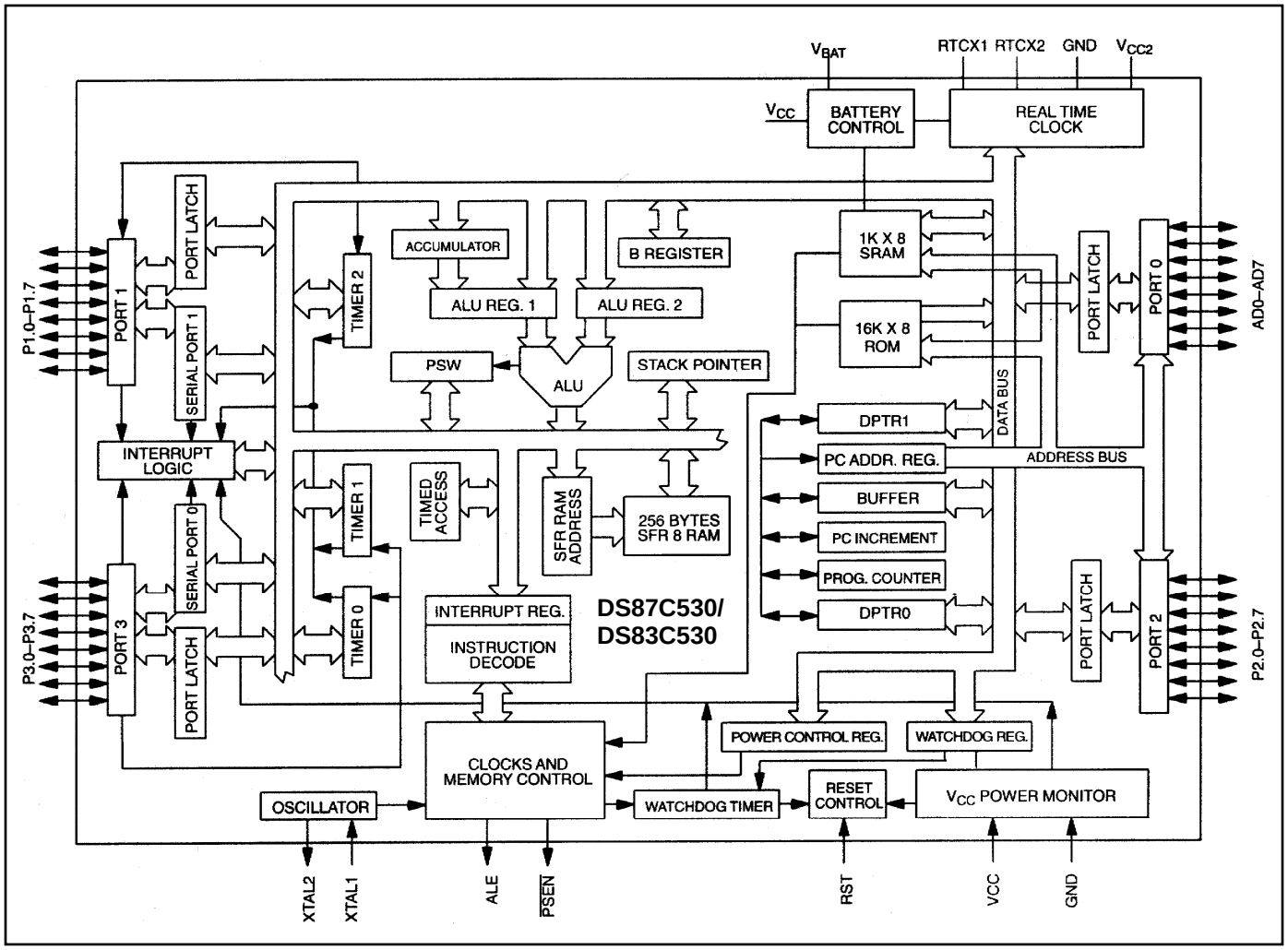
Power Management Mode (PMM) allows software to select a slower CPU clock. While default operation uses four clocks per machine cycle, the PMM runs the processor at 64 or 1024 clocks per cycle. There is a corresponding drop in power consumption when the processor slows.

The EMI reduction feature allows software to select a reduced emission mode. This disables the ALE signal when it is unneeded.

The DS83C530 is a factory mask ROM version of the DS87C530 designed for high-volume, cost-sensitive applications. It is identical in all respects to the DS87C530, except that the 16kB of EPROM is replaced by a user-supplied application program. All references to features of the DS87C530 will apply to the DS83C530, with the exception of EPROM-specific features where noted. Please contact your local Dallas Semiconductor sales representative for ordering information.

Note: The DS87C530/DS83C530 are monolithic devices. A user must supply an external battery or super cap and a 32.768kHz timekeeping crystal to have permanently powered timekeeping or nonvolatile RAM. The DS87C530/DS83C530 provide all the support and switching circuitry needed to manage these resources.

Figure 1. Block Diagram



PIN DESCRIPTION

PIN		NAME	FUNCTION
PLCC	TQFP		
52	45	V_{CC}	**+5V Processor Power Supply**
1, 25	18, 46	GND	**Processor Digital Circuit Ground**
29	22	V_{CC2}	**+5V RTC Supply.** V_{CC2} is isolated from V_{CC} to isolate the RTC from digital noise.
26	19	GND2	**RTC Circuit Ground**
12	5	RST	**Reset Input.** This pin contains a Schmitt voltage input to recognize external active high reset inputs. The pin also employs an internal pulldown resistor to allow for a combination of wired OR external reset sources. An RC is not required for power-up, as the device provides this function internally.
23	16	XTAL2	**Crystal Oscillator Pins.** XTAL1 and XTAL2 provide support for parallel-resonant, AT-cut crystals. XTAL1 acts also as an input if there is an external clock source in place of a crystal. XTAL2 is the output of the crystal amplifier.
24	17	XTAL1	

PIN DESCRIPTION (continued)

<table>
<tr><th colspan="2">PIN</th><th rowspan="2">NAME</th><th rowspan="2">FUNCTION</th></tr>
<tr><th>PLCC</th><th>TQFP</th></tr>
<tr><td>38</td><td>31</td><td>$\overline{\text{PSEN}}$</td><td>Program Store-Enable Output. This active-low signal is a chip enable for optional external ROM memory. $\overline{\text{PSEN}}$ provides an active-low pulse and is driven high when external ROM is not being accessed.</td></tr>
<tr><td>39</td><td>32</td><td>ALE</td><td>Address Latch-Enable Output. This pin latches the external address LSB from the multiplexed address/data bus on Port 0. This signal is commonly connected to the latch enable of an external 373 family transparent latch. ALE has a pulse width of 1.5 XTAL1 cycles and a period of four XTAL1 cycles. ALE is forced high when the device is in a Reset condition. ALE can be disabled and forced high by writing ALEOFF = 1 (PMR.2). ALE operates independently of ALEOFF during external memory accesses.</td></tr>
<tr><td>50</td><td>43</td><td>P0.0 (AD0)</td><td rowspan="8">Port 0 (AD0–AD7), I/O. Port 0 is an open-drain, 8-bit, bidirectional I/O port. As an alternate function Port 0 can function as the multiplexed address/data bus to access off-chip memory. During the time when ALE is high, the LSB of a memory address is presented. When ALE falls to a logic 0, the port transitions to a bidirectional data bus. This bus is used to read external ROM and read/ write external RAM memory or peripherals. When used as a memory bus, the port provides active high drivers. The reset condition of Port 0 is tri-state. Pullup resistors are required when using Port 0 as an I/O port.</td></tr>
<tr><td>49</td><td>42</td><td>P0.1 (AD1)</td></tr>
<tr><td>48</td><td>41</td><td>P0.2 (AD2)</td></tr>
<tr><td>47</td><td>40</td><td>P0.3 (AD3)</td></tr>
<tr><td>46</td><td>39</td><td>P0.4 (AD4)</td></tr>
<tr><td>45</td><td>38</td><td>P0.5 (AD5)</td></tr>
<tr><td>44</td><td>37</td><td>P0.6 (AD6)</td></tr>
<tr><td>43</td><td>36</td><td>P0.7 (AD7)</td></tr>
<tr><td>3</td><td>48</td><td>P1.0</td><td rowspan="9">Port 1, I/O. Port 1 functions as both an 8-bit, bidirectional I/O port and an alternate functional interface for Timer 2 I/O, new External Interrupts, and new Serial Port 1. The reset condition of Port 1 is with all bits at a logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pullup. When software writes a 0 to any port pin, the device will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes the output high (and input) state. The alternate modes of Port 1 are outlined as follows.

Port Alternate Function
P1.0 T2 External I/O for Timer/Counter 2
P1.1 T2EX Timer/Counter 2 Capture/Reload Trigger
P1.2 RXD1 Serial Port 1 Input
P1.3 TXD1 Serial Port 1 Output
P1.4 $\overline{\text{INT2}}$ External Interrupt 2 (Positive Edge Detect)
P1.5 $\overline{\text{INT3}}$ External Interrupt 3 (Negative Edge Detect)
P1.6 $\overline{\text{INT4}}$ External Interrupt 4 (Positive Edge Detect)
P1.7 $\overline{\text{INT5}}$ External Interrupt 5 (Negative Edge Detect)</td></tr>
<tr><td>4</td><td>49</td><td>P1.1</td></tr>
<tr><td>5</td><td>50</td><td>P1.2</td></tr>
<tr><td>6</td><td>51</td><td>P1.3</td></tr>
<tr><td>7</td><td>52</td><td>P1.4</td></tr>
<tr><td>8</td><td>1</td><td>P1.5</td></tr>
<tr><td>9</td><td>2</td><td>P1.6</td></tr>
<tr><td>10</td><td>3</td><td>P1.7</td></tr>
</table>

PIN DESCRIPTION (continued)

PIN		NAME	FUNCTION
PLCC	TQFP		
30	23	P2.0 (AD8)	**Port 2 (A8–A15), I/O**. Port 2 is a bidirectional I/O port. The reset condition of Port 2 is logic high. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pullup. When software writes a 0 to any port pin, the device will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. As an alternate function Port 2 can function as MSB of the external address bus. This bus can be used to read external ROM and read/write external RAM memory or peripherals.
31	24	P2.1 (AD9)	
32	25	P2.2 (AD10)	
33	26	P2.3 (AD11)	
34	27	P2.4 (AD12)	
35	28	P2.5 (AD13)	
36	29	P2.6 (AD14)	
37	30	P2.7 (AD15)	
15	8	P3.0	**Port 3, I/O.** Port 3 functions as both an 8-bit, bi-directional I/O port and an alternate functional interface for external interrupts, Serial Port 0, Timer 0 and 1 Inputs, and $\overline{RD}$ and $\overline{WR}$ strobes. The reset condition of Port 3 is with all bits at a logic 1. In this state, a weak pullup holds the port high. This condition also serves as an input mode, since any external circuit that writes to the port will overcome the weak pullup. When software writes a 0 to any port pin, the device will activate a strong pulldown that remains on until either a 1 is written or a reset occurs. Writing a 1 after the port has been at 0 will cause a strong transition driver to turn on, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port again becomes both the output high and input state. The alternate modes of Port 3 are outlined below. **Port** **Alternate** **Function** P3.0 RXD0 Serial Port 0 Input P3.1 TXD0 Serial Port 0 Output P3.2 $\overline{INT0}$ External Interrupt 0 P3.3 $\overline{INT1}$ External Interrupt 1 P3.4 T0 Timer 0 External Input P3.5 T1 Timer 1 External Input P3.6 $\overline{WR}$ External Data Memory Write Strobe P3.7 $\overline{RD}$ External Data Memory Read Strobe
16	9	P3.1	
17	10	P3.2	
18	11	P3.3	
19	12	P3.4	
20	13	P3.5	
21	14	P3.6	
22	15	P3.7	
42	35	$\overline{EA}$	**External Access Input, Active Low.** Connect to ground to use an external ROM. Internal RAM is still accessible as determined by register settings. Connect to V_{CC} to use internal ROM.
51	44	V_{BAT}	**V_{BAT} Input.** Connect to the power source that maintains SRAM and RTC when $V_{CC} < V_{BAT}$. Can be connected to a 3V lithium battery or a super cap. Connect to GND if battery will not be used with device.
27	20	RTCX2	**Timekeeping Crystals**. A 32.768kHz crystal between these pins supplies the time base for the RTC. The devices support both 6pF and 12.5pF load capacitance crystals as selected by an SFR bit (described later). To prevent noise from affecting the RTC, the RTCX2 and RTCX1 pins should be guard-ringed with GND2.
28	21	RTCX1	
2, 11, 13, 14, 40, 41	4, 6, 7, 33, 34, 47	N.C.	**Not Connected.** These pins should not be connected. They are reserved for use with future devices in the family.

The relative time of two instructions might be different in the new architecture than it was previously. For example, in the original architecture, the “MOVX A, @DPTR” instruction and the “MOV direct, direct” instruction used two machine cycles or 24 oscillator cycles. Therefore, they required the same amount of time. In the DS87C530/DS83C530, the MOVX instruction takes as little as two machine cycles or eight oscillator cycles but the “MOV direct, direct” uses three machine cycles or 12 oscillator cycles. While both are faster than their original counterparts, they now have different execution times. This is because the DS87C530/DS83C530 usually use one instruction cycle for each instruction byte. The user concerned with precise program timing should examine the timing of each instruction for familiarity with the changes. Note that a machine cycle now requires just 4 clocks, and provides one ALE pulse per cycle. Many instructions require only one cycle, but some require five. In the original architecture, all were one or two cycles except for MUL and DIV. Refer to the *High-Speed Microcontroller User’s Guide* for details and individual instruction timing.

SPECIAL FUNCTION REGISTERS

Special Function Registers (SFRs) control most special features of the DS87C530/DS83C530. This allows the device to incorporate new features but remain instruction-set compatible with the 8051. EQUATE statements can be used to define the new SFR to an assembler or compiler. All SFRs contained in the standard 80C52 are duplicated in this device. Table 1 shows the register addresses and bit locations. The *High-Speed Microcontroller User’s Guide* describes all SFRs.

Table 1. Special Function Register Locations (continued)

** Functions not present in the 80C52 are in bold.*

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
TL2									CCh
TH2									CDh
PSW	CY	AC	F0	RS1	RS0	OV	FL	P	D0h
WDCON	**SMOD_1**	**POR**	**EPFI**	**PFI**	**WDIF**	**WTRF**	**EWT**	**RWT**	D8h
ACC									E0h
EIE	—	—	**ERTCI**	**EWDI**	**EX5**	**EX4**	**EX3**	**EX2**	E8h
B									F0h
RTASS									F2h
RTAS	0	0							F3h
RTAM	0	0							F4h
RTAH	0	0	0						F5h
EIP	—	—	**PRTCI**	**PWDI**	**PX5**	**PX4**	**PX3**	**PX2**	F8h
RTCC	**SSCE**	**SCE**	**MCE**	**HCE**	**RTCRE**	**RTCWE**	**RTCIF**	**RTCE**	F9h
RTCSS									FAh
RTCS	0	0							FBh
RTCM	0	0							FCh
RTCH									FDh
RTCD0									FEh
RTCD1									FFh

NONVOLATILE FUNCTIONS

The DS87C530/DS83C530 provide two functions that are permanently powered if a user supplies an external energy source. These are an on-chip RTC and a nonvolatile SRAM. The chip contains all related functions and controls. The user must supply a backup source and a 32.768kHz timekeeping crystal.

REAL-TIME CLOCK

The on-chip RTC keeps time of day and calendar functions. Its time base is a 32.768kHz crystal between pins RTCX1 and RTCX2. The RTC maintains time to 1/256 of a second. It also allows a user to read (and write) seconds, minutes, hours, day of the week, and date. Figure 2 shows the clock organization.

Timekeeping registers allow easy access to commonly needed time values. For example, software can simply check the elapsed number of minutes by reading one register. Alternately, it can read the complete time of day, including subseconds, in only four registers. The calendar stores its data in binary form. While this requires software translation, it allows complete flexibility as to the exact value. A user can start the calendar with a variety of selections since it is simply a 16-bit binary number of days. This number allows a total range of 179 years beginning from 0000.

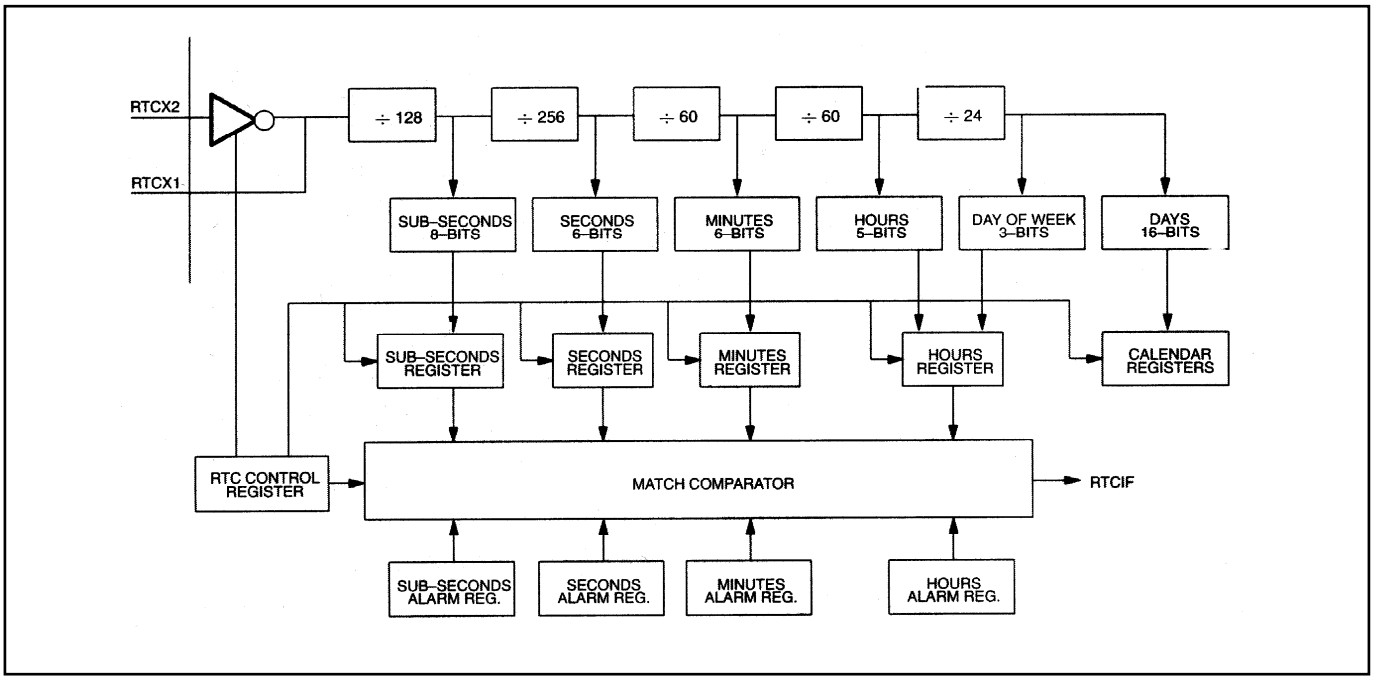
The RTC features a programmable alarm condition. A user selects the alarm time. When the RTC reaches the selected value, it sets a flag. This will cause an interrupt if enabled, even in Stop mode. The alarm consists of a comparator that matches the user value against the RTC actual value. A user can select a match for 1 or more of the sub-seconds, seconds, minutes, or hours. This allows an interrupt

automatically to occur once per second, once per minute, once per hour, or once per day. Enabling interrupts with no match will generate an interrupt 256 times per second.

Software enables the timekeeper oscillator using the RTC enable bit in the RTC Control register (F9h). This starts the clock. It can disable the oscillator to preserve the life of the backup energy-source if unneeded. Values in the RTC Control register are maintained by the backup source through power failure. Once enabled, the RTC maintains time for the life of the backup source even when V_{CC} is removed.

The RTC will maintain an accuracy of ±2 minutes per month at 25°C. Under no circumstances are negative voltages, of any amplitude, allowed on any pin while the device is in data retention mode ($V_{CC} < V_{BAT}$). Negative voltages will shorten battery life, possibly corrupting the contents of internal SRAM and the RTC.

Figure 2. Real-Time Clock



NONVOLATILE RAM

The 1k x 8 on-chip SRAM can be nonvolatile if an external backup energy source is used. This allows the device to log data or to store configuration settings. Internal switching circuits will detect the loss of V_{CC} and switch SRAM power to the backup source on the V_{BAT} pin. The 256 bytes of direct RAM are not affected by this circuit and are volatile.

CRYSTAL AND BACKUP SOURCES

To use the unique functions of the DS87C530/DS83C530, a 32.768kHz timekeeping crystal and a backup energy source are needed. The following describes guidelines for choosing these devices.

Timekeeping Crystal

The DS87C530/DS83C530 can use a standard 32.768kHz crystal as the RTC time base. There are two versions of standard crystals available, with 6pF and 12.5pF load capacitance. The tradeoff is that the 6pF uses less power, giving longer life while V_{CC} is off, but is more sensitive to noise and board layout. The

The on-chip data area is software selectable using 2 bits in the Power Management Register at location C4h. This selection is dynamically programmable. Thus access to the on-chip area becomes transparent to reach off-chip devices at the same addresses. The control bits are DME1 (PMR.1) and DME0 (PMR.0). They have the following operation:

Table 2. Data Memory Access Control

DME1	DME0	DATA MEMORY ADDRESS	MEMORY FUNCTION
0	0	0000h–FFFFh	External Data Memory (*default condition)*
0	1	0000h–03FFh	Internal SRAM Data Memory
		0400h–FFFFh	External Data Memory
1	0	Reserved	Reserved
1	1	0000h–03FFh	Internal SRAM Data Memory
		0400h–FFFBh	Reserved—no external access
		FFFCh	Read access to the status of lock bits
		FFFDh–FFFh	Reserved—no external access

Notes on the status byte read at FFFCh with DME1, 0 = 1, 1: Bits 2-0 reflect the programmed status of the security lock bits LB2–LB0. They are individually set to a logic 1 to correspond to a security lock bit that has been programmed. These status bits allow software to verify that the part has been locked before running if desired. The bits are read-only.

Note: After internal MOVX SRAM has been initialized, changing bits DEM0/1 has no effect on the contents of the SRAM.

STRETCH MEMORY CYCLE

The DS87C530/DS83C530 allow software to adjust the speed of off-chip data memory access. The microcontrollers can perform the MOVX in as few as two instruction cycles. The on-chip SRAM uses this speed and any MOVX instruction directed internally uses two cycles. However, the time can be stretched for interface to external devices. This allows access to both fast memory and slow memory or peripherals with no glue logic. Even in high-speed systems, it may not be necessary or desirable to perform off-chip data memory access at full speed. In addition, there are a variety of memory-mapped peripherals such as LCDs or UARTs that are slow.

The Stretch MOVX is controlled by the Clock Control Register at SFR location 8Eh as described below. It allows the user to select a Stretch value between 0 and 7. A Stretch of 0 will result in a two-machine cycle MOVX. A Stretch of 7 will result in a MOVX of nine machine cycles. Software can dynamically change this value depending on the particular memory or peripheral.

On reset, the Stretch value will default to a 1, resulting in a three-cycle MOVX for any external access. Therefore, off-chip RAM access is not at full speed. This is a convenience to existing designs that may not have fast RAM in place. Internal SRAM access is always at full speed regardless of the Stretch setting. When desiring maximum speed, software should select a Stretch value of 0. When using very slow RAM or peripherals, select a larger Stretch value. Note that this affects data memory only and the only way to slow program memory (ROM) access is to use a slower crystal.

POWER MANAGEMENT

Along with the standard Idle and power-down (Stop) modes of the standard 80C52, the DS87C530/DS83C530 provide a new Power Management Mode. This mode allows the processor to continue functioning, yet to save power compared with full operation. The DS87C530/DS83C530 also feature several enhancements to Stop mode that make it more useful.

POWER MANAGEMENT MODE (PMM)

Power Management Mode offers a complete scheme of reduced internal clock speeds that allow the CPU to run software but to use substantially less power. During default operation, the DS87C530/DS83C530 use four clocks per machine cycle. Thus the instruction cycle rate is (Clock/4). At 33MHz crystal speed, the instruction cycle speed is 8.25MHz (33/4). In PMM, the microcontroller continues to operate but uses an internally divided version of the clock source. This creates a lower power state without external components. It offers a choice of two reduced instruction cycle speeds (and two clock sources - discussed below). The speeds are (Clock/64) and (Clock/1024).

Software is the only mechanism to invoke the PMM. Table 4 illustrates the instruction cycle rate in PMM for several common crystal frequencies. Since power consumption is a direct function of operating speed, PMM 1 eliminates most of the power consumption while still allowing a reasonable speed of processing. PMM 2 runs very slowly and provides the lowest power consumption without stopping the CPU. This is illustrated in Table 5.

Note that PMM provides a lower power condition than Idle mode. This is because in Idle, all clocked functions such as timers run at a rate of crystal divided by 4. Since wake-up from PMM is as fast as or faster than from Idle and PMM allows the CPU to operate (even if doing NOPs), there is little reason to use Idle mode in new designs.

Table 4. Machine Cycle Rate

CRYSTAL SPEED (MHz)	FULL OPERATION (4 CLOCKS) (MHz)	PMM1 (64 CLOCKS) (kHz)	PMM2 (1024 CLOCKS) (kHz)
11.0592	2.765	172.8	10.8
16	4.00	250.0	15.6
25	6.25	390.6	24.4
33	8.25	515.6	32.2

Table 5. Typical Operating Current in PMM

CRYSTAL SPEED (MHz)	FULL OPERATION (4 CLOCKS) (mA)	PMM1 (64 CLOCKS) (mA)	PMM2 (1024 CLOCKS) (mA)
11.0592	13.1	5.3	4.8
16	17.2	6.4	5.6
25	25.7	8.1	7.0
33	32.8	9.8	8.2

CRYSTAL-LESS PMM

A major component of power consumption in PMM is the crystal amplifier circuit. The DS87C530/DS83C530 allow the user to switch CPU operation to an internal ring oscillator and turn off the crystal amplifier. The CPU would then have a clock source of approximately 2MHz to 4MHz, divided by either 4, 64, or 1024. The ring is not accurate, so software cannot perform precision timing. However, this mode allows an additional saving of between 0.5mA and 6.0mA, depending on the actual crystal frequency. While this saving is of little use when running at 4 clocks per instruction cycle, it makes a major contribution when running in PMM1 or PMM2.

PMM OPERATION

Software invokes the PMM by setting the appropriate bits in the SFR area. The basic choices are divider speed and clock source. There are three speeds (4, 64, and 1024) and two clock sources (crystal, ring). Both the decisions and the controls are separate. Software will typically select the clock speed first. Then, it will perform the switch to ring operation if desired. Lastly, software can disable the crystal amplifier if desired.

There are two ways of exiting PMM. Software can remove the condition by reversing the procedure that invoked PMM or hardware can (optionally) remove it. To resume operation at a divide-by-4 rate under software control, simply select 4 clocks per cycle, and then crystal-based operation if relevant. When disabling the crystal as the time base in favor of the ring oscillator, there are timing restrictions associated with restarting the crystal operation. Details are described below.

There are three registers containing bits that are concerned with PMM functions. They are Power Management Register (PMR; C4h), Status (STATUS; C5h), and External Interrupt Flag (EXIF; 91h)

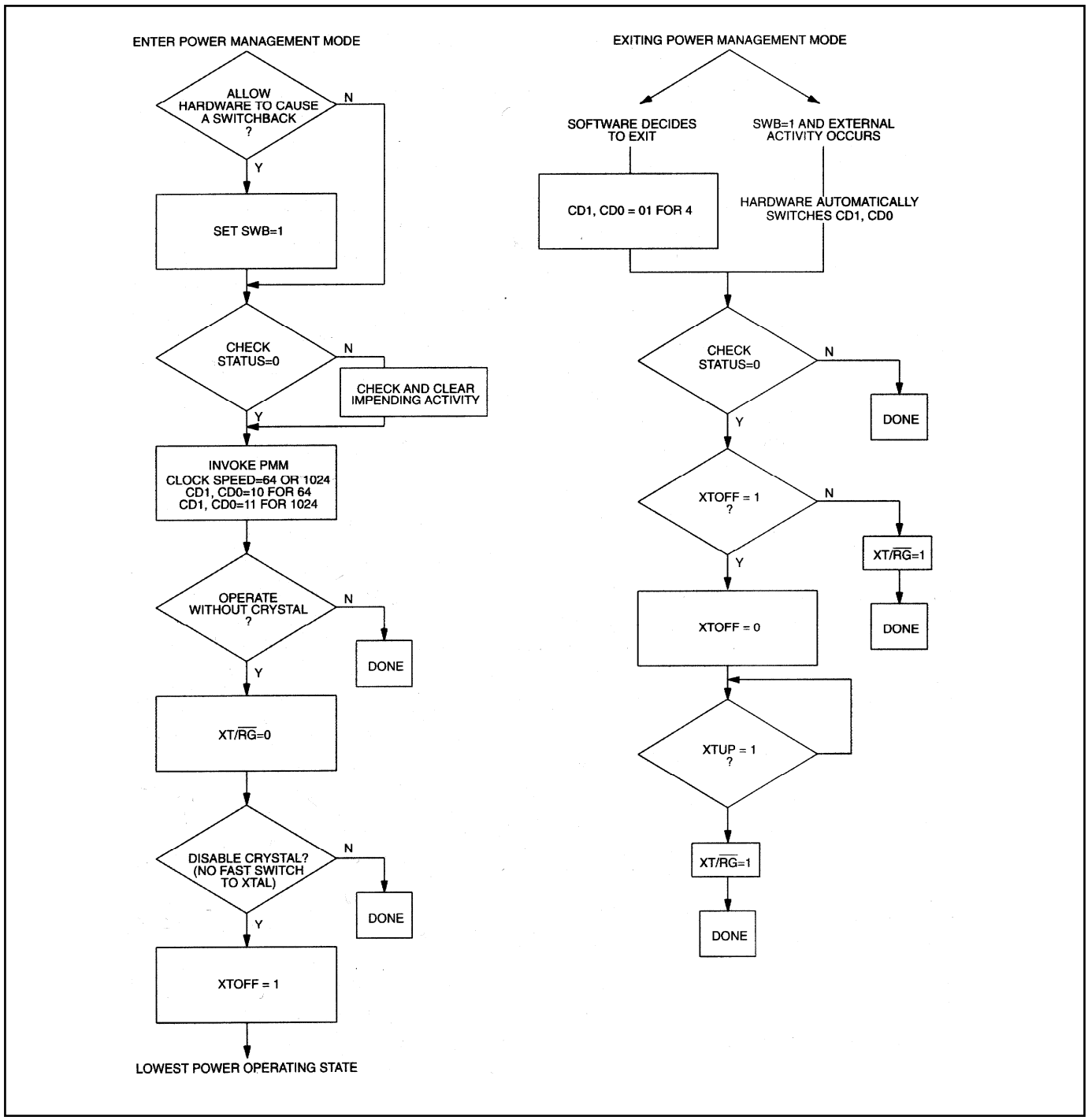
Clock Divider

Software can select the instruction cycle rate by selecting bits CD1 (PMR.7) and CD0 (PMR.6) as follows:

CD1	CD0	CYCLE RATE
0	0	Reserved
0	1	4 clocks (default)
1	0	64 clocks
1	1	1024 clocks

The selection of instruction cycle rate will take effect after a delay of one instruction cycle. Note that the clock divider choice applies to all functions including timers. Since baud rates are altered, it will be difficult to conduct serial communication while in PMM. There are minor restrictions on accessing the clock selection bits. The processor must be running in a 4-clock state to select either 64 (PMM1) or 1024 (PMM2) clocks. This means software cannot go directly from PMM1 to PMM2 or visa versa. It must return to a 4-clock rate first.

Figure 5. Invoking and Clearing PMM



PERIPHERAL OVERVIEW

The DS87C530/DS83C530 provide several of the most commonly needed peripheral functions in microcomputer-based systems. These new functions include a second serial port, power-fail reset, Power-fail interrupt, and a programmable watchdog timer. These are described below, and more details are available in the *High-Speed Microcontroller User's Guide*.

SERIAL PORTS

The DS87C530/DS83C530 provide a serial port (UART) that is identical to the 80C52. In addition it includes a second hardware serial port that is a full duplicate of the standard one. This port optionally uses pins P1.2 (RXD1) and P1.3 (TXD1). It has duplicate control functions included in new SFR locations.

Both ports can operate simultaneously but can be at different baud rates or even in different modes. The second serial port has similar control registers (SCON1; C0h, SBUF1; C1h) to the original. The new serial port can only use Timer 1 for timer-generated baud rates.

TIMER RATE CONTROL

There is one important difference between the DS87C530/DS83C530 and 8051 regarding timers. The original 8051 used 12 clocks per cycle for timers as well as for machine cycles. The DS87C530/DS83C530 architecture normally uses 4 clocks per machine cycle. However, in the area of timers and serial ports, the DS87C530/DS83C530 will default to 12 clocks per cycle on reset. This allows existing code with real-time dependencies such as baud rates to operate properly.

If an application needs higher speed timers or serial baud rates, the user can select individual timers to run at the 4-clock rate. The Clock Control register (CKCON; 8Eh) determines these timer speeds. When the relevant CKCON bit is logic 1, the DS87C530/DS83C530 use 4 clocks per cycle to generate timer speeds. When the bit is a 0, the DS87C530 uses 12 clocks for timer speeds. The reset condition is a 0. CKCON.5 selects the speed of Timer 2. CKCON.4 selects Timer 1 and CKCON.3 selects Timer 0. Unless a user desires very fast timing, it is unnecessary to alter these bits. Note that the timer controls are independent.

POWER-FAIL RESET

The DS87C530/DS83C530 use a precision bandgap voltage reference to decide if V_{CC} is out of tolerance. While powering up, the internal monitor circuit maintains a reset state until V_{CC} rises above the V_{RST} level. Once above this level, the monitor enables the crystal oscillator and counts 65,536 clocks. It then exits the reset state. This power-on reset (POR) interval allows time for the oscillator to stabilize.

A system needs no external components to generate a power-related reset. Anytime V_{CC} drops below V_{RST}, as in power failure or a power drop, the monitor will generate and hold a reset. It occurs automatically, needing no action from the software. Refer to the *Electrical Specifications* section for the exact value of V_{RST}.

POWER-FAIL INTERRUPT

The voltage reference that sets a precise reset threshold also generates an optional early warning power-fail interrupt (PFI). When enabled by software, the processor will vector to program memory address 0033h if V_{CC} drops below V_{PFW}. PFI has the highest priority. The PFI enable is in the Watchdog Control SFR (WDCON–D8h). Setting WDCON.5 to logic 1 will enable the PFI. Application software can also

There are five control bits in special function registers that affect the Watchdog Timer and two status flags that report to the user. WDIF (WDCON.3) is the interrupt flag that is set at timer termination when there are 512 clocks remaining until the reset flag is set. WTRF (WDCON.2) is the flag that is set when the timer has completely timed out. This flag is normally associated with a CPU reset and allows software to determine the reset source. EWT (WDCON.1) is the enable for the Watchdog Timer reset function. RWT (WDCON.0) is the bit that software uses to restart the Watchdog Timer. Setting this bit restarts the timer for another full interval. Application software must set this bit before the timeout. Both of these bits are protected by Timed Access discussed below. As mentioned previously, WD1 and 0 (CKCON .7 and 6) select the timeout. The Reset Watchdog Timer bit (WDCON.0) should be asserted prior to modifying the Watchdog Timer Mode Select bits (WD1, WD0) to avoid corruption of the watchdog count. Finally, the user can enable the Watchdog Interrupt using EWDI (EIE.4).

INTERRUPTS

The DS87C530/DS83C530 provide 14 interrupt sources with three priority levels. The Power-Fail Interrupt (PFI) has the highest priority. Software can assign high or low priority to other sources. All interrupts that are new to the 8051 family, except for the PFI, have a lower natural priority than the originals.

Table 8. Interrupt Sources and Priorities

NAME	FUNCTION	VECTOR	NATURAL PRIORITY	8051/DALLAS
PFI	Power-Fail Interrupt	33h	1	DALLAS
$\overline{\text{INT0}}$	External Interrupt 0	03h	2	8051
TF0	Timer 0	0Bh	3	8051
$\overline{\text{INT1}}$	External Interrupt 1	13h	4	8051
TF1	Timer 1	1Bh	5	8051
SCON0	TI0 or RI0 from Serial Port 0	23h	6	8051
TF2	Timer 2	2Bh	7	8051
SCON1	TI1 or RI1 from Serial Port 1	3Bh	8	DALLAS
INT2	External Interrupt 2	43h	9	DALLAS
$\overline{\text{INT3}}$	External Interrupt 3	4Bh	10	DALLAS
INT4	External Interrupt 4	53h	11	DALLAS
$\overline{\text{INT5}}$	External Interrupt 5	5Bh	12	DALLAS
WDTI	Watchdog Timeout Interrupt	63h	13	DALLAS
RTCI	RTC Interrupt	6Bh	14	DALLAS

Table 9. EPROM Programming Modes

MODE		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/VPP	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code Data		H	L	PL	12.75V	L	H	H	H	H
Verify Code Data		H	L	H	H	L	L	L	H	H
Program Encryption Array Address 0-3Fh		H	L	PL	12.75V	L	H	H	L	H
Program Lock Bits	LB1	H	L	PL	12.75V	H	H	H	H	H
	LB2	H	L	PL	12.75V	H	H	H	L	L
	LB3	H	L	PL	12.75V	H	L	H	H	L
Program Option Register Address FCh		H	L	PL	12.75V	L	H	H	L	L
Read Signature or Option Registers 30, 31, 60, FCh		H	L	H	H	L	L	L	L	L

* *PL indicates pulse to a logic low.*

Table 10. EPROM Lock Bits

LEVEL	LOCK BITS			PROTECTION
	LB1	LB2	LB3	
1	U	U	U	No program lock. Encrypted verify if encryption table was programmed.
2	P	U	U	Prevent MOVC instructions in external memory from reading program bytes in internal memory. $\overline{EA}$ is sampled and latched on reset. Allow no further programming of EPROM.
3	P	P	U	Level 2 plus no verify operation. Also, prevent MOVX instructions in external memory from reading SRAM (MOVX) in internal memory.
4	P	P	P	Level 3 plus no external execution.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……-0.3V to (V_{CC} + 0.5V)
Voltage Range on V_{CC} Relative to Ground……-0.3V to +6.0V
Operating Temperature Range……0°C to +70°C
Storage Temperature Range……-55°C to +125°C (Note 1)
Soldering Temperature……See IPD/JEDEC J-STD-020 Specification

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, T_A = -40°C to +85°C.) (Note 2)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	3
Power-Fail Warning	V_{PFW}	4.25	4.38	4.5	V	3
Minimum Operating Voltage	V_{RST}	4.0	4.13	4.25	V	3
Backup Battery Voltage	V_{BAT}	2.5	3.0	V_{CC}-0.7	V	
Supply Current Active Mode at 33MHz	I_{CC}		30	46	mA	4
Supply Current Idle Mode at 33MHz	I_{Idle}		15	25	mA	5
Supply Current Stop Mode, Bandgap Disabled (0°C to +70°C)	I_{Stop}		1	100	µA	6
Supply Current Stop Mode, Bandgap Disabled (-40°C to +85°C)			1	150	µA	6
Supply Current Stop Mode, Bandgap Enabled (0°C to +70°C)	I_{SPBG}		50	170	µA	6
Supply Current Stop Mode, Bandgap Enabled (-40°C to +85°C)			50	195	µA	6
Backup Supply Current, Data-Retention Mode (0°C to +70°C)	I_{BAT}	0		0.5	µA	7
Backup Supply Current, Data-Retention Mode (-40°C to +85°C)		0		1	µA	7
Input Low Level	V_{IL}	-0.3		+0.8	V	3
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V	3
Input High Level XTAL1 and RST	V_{IH2}	3.5		V_{CC}+0.3	V	3
Output Low Voltage at I_{OL} = 1.6mA	V_{OL1}		0.15	0.45	V	3
Output Low Voltage Ports 0, 2, ALE, and $\overline{PSEN}$ at I_{OL} = 3.2mA	V_{OL2}		0.15	0.45	V	3
Output High Voltage Ports 1, 2, 3, ALE, $\overline{PSEN}$ at I_{OH} = -50µA	V_{OH1}	2.4			V	3, 8
Output High Voltage Ports 1, 2, 3 at I_{OH} = -1.5mA	V_{OH2}	2.4			V	3, 9
Output High Voltage Port 0 in Bus Mode I_{OH} = -8mA	V_{OH3}	2.4			V	3, 10
Input Low Current Ports 1, 2, 3 at 0.45V	I_{IL}			-70	µA	11
Transition Current from 1 to 0 Ports 1, 2, 3 at 2V	I_{TL}			-800	µA	12

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.5V to 5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Port 0, $\overline{EA}$, Pins, I/O Mode	I_L	-10		+10	µA	13
Input Leakage Port 0, Bus Mode	I_L	-300		+300	µA	14
RST Pulldown Resistance	R_{RST}	50		200	kΩ	

Note 1: Storage temperature is defined as the temperature of the device when V_{CC} = 0V and V_{BAT} = 0V. In this state, the contents of SRAM are not battery backed and are undefined.

Note 2: All parameters apply to both commercial and industrial temperature operation unless otherwise noted.

Note 3: All voltages are referenced to ground.

Note 4: Active current measured with 33MHz clock source on XTAL1, V_{CC} = RST = 5.5V, other pins disconnected.

Note 5: Idle mode current measured with 33MHz clock source on XTAL1, V_{CC} = 5.5V, RST at ground, other pins disconnected.

Note 6: Stop mode current measured with XTAL1 and RST grounded, V_{CC} = 5.5V, all other pins disconnected.

Note 7: V_{CC} = 0V, V_{BAT} = 3.3V. 32.768kHz crystal with 12.5pF load capacitance between RTCX1 and RTCX2 pins. RTCE bit set to 1.

Note 8: RST = V_{CC}. This condition mimics operation of pins in I/O mode. Port 0 is tri-stated in reset and when at a logic high state during I/O mode.

Note 9: During a 0-to-1 transition, a one-shot drives the ports hard for two clock cycles. This measurement reflects port in transition mode.

Note 10: When addressing external memory. This specification only applies to the first clock cycle following the transition.

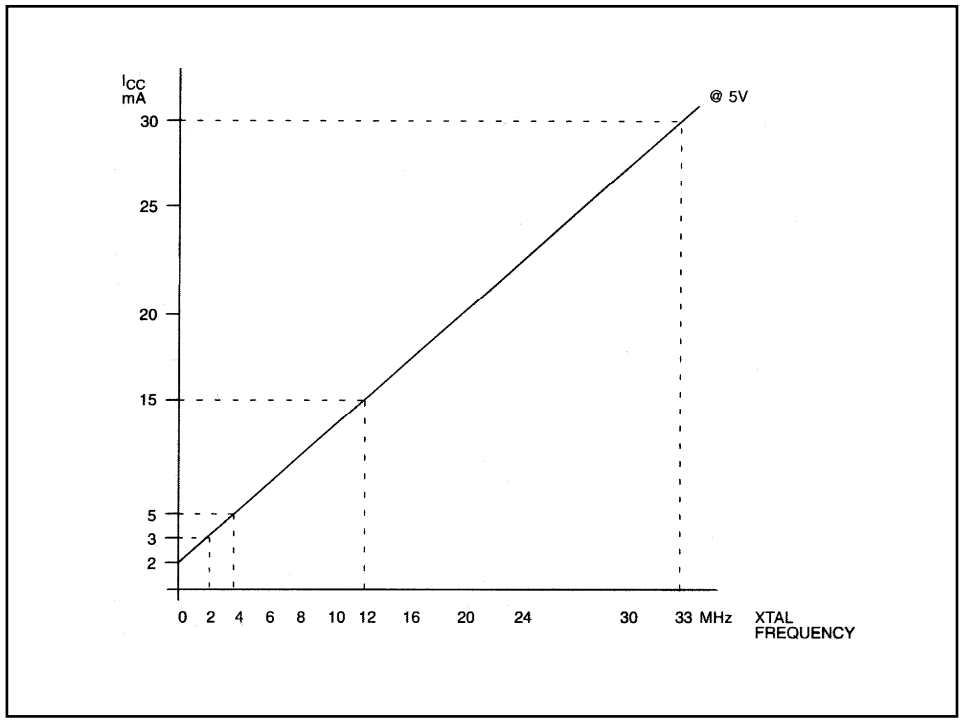
Note 11: This is the current required from an external circuit to hold a logic low level on an I/O pin while the corresponding port latch bit is set to 1. This is only the current required to *hold* the low level; transitions from 1 to 0 on an I/O pin will also have to overcome the transition current.

Note 12: Ports 1, 2, and 3 source transition current when being pulled down externally. It reaches its maximum at approximately 2V.

Note 13: 0.45 < V_{IN} < V_{CC}. RST = V_{CC}. This condition mimics operation of pins in I/O mode.

Note 14: 0.45 < V_{IN} < V_{CC}. Not a high-impedance input. This port is a weak address holding latch in Bus Mode. Peak current occurs near the input transition point of the latch, approximately 2V.

TYPICAL I_{CC} vs. FREQUENCY



MOVX CHARACTERISTICS USING STRETCH MEMORY CYCLES (continued)

M2	M1	M0	MOVX CYCLES	t_{MCS}
0	0	0	2 machine cycles	0
0	0	1	3 machine cycles (default)	4 t_{CLCL}
0	1	0	4 machine cycles	8 t_{CLCL}
0	1	1	5 machine cycles	12 t_{CLCL}
1	0	0	6 machine cycles	16 t_{CLCL}
1	0	1	7 machine cycles	20 t_{CLCL}
1	1	0	8 machine cycles	24 t_{CLCL}
1	1	1	9 machine cycles	28 t_{CLCL}

EXTERNAL CLOCK CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Clock High Time	t_{CHCX}	10			ns
Clock Low Time	t_{CLCX}	10			ns
Clock Rise Time	t_{CLCL}			5	ns
Clock Fall Time	t_{CHCL}			5	ns

SERIAL PORT MODE 0 TIMING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Port Clock Cycle Time	t_{XLXL}	SM2 = 0, 12 clocks per cycle		$12t_{CLCL}$		ns
		SM2 = 1, 4 clocks per cycle		$4t_{CLCL}$		
Output Data Setup to Clock Rising	t_{QVXH}	SM2 = 0, 12 clocks per cycle		$10t_{CLCL}$		ns
		SM2 = 1, 4 clocks per cycle		$3t_{CLCL}$		
Output Data Hold from Clock Rising	t_{XHQX}	SM2 = 0, 12 clocks per cycle		$2t_{CLCL}$		ns
		SM2 = 1, 4 clocks per cycle		t_{CLCL}		
Input Data Hold after Clock Rising	t_{XHDX}	SM2 = 0, 12 clocks per cycle		t_{CLCL}		ns
		SM2 = 1, 4 clocks per cycle		t_{CLCL}		
Clock Rising Edge to Input Data Valid	t_{XHDV}	SM2 = 0, 12 clocks per cycle		$11t_{CLCL}$		ns
		SM2 = 1, 4 clocks per cycle		$3t_{CLCL}$		

EXPLANATION OF AC SYMBOLS

In an effort to remain compatible with the original 8051 family, this device specifies the same parameters as such devices, using the same symbols. For completeness, the following is an explanation of the symbols.

t	Time	I	Instruction	W	$\overline{WR}$ signal
A	Address	P	$\overline{PSEN}$	X	No longer a valid logic level
C	Clock	Q	Output data		
D	Input data	R	$\overline{RD}$ signal	Z	Tri-State
H	Logic level high	V	Valid		
L	Logic level low				

POWER-CYCLE TIMING CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Startup Time	t_{CSU}		1.8		ms	1
Power-On Reset Delay	t_{POR}			65,536	t_{CLCL}	2

Note 1: Startup time for crystals varies with load capacitance and manufacturer. Time shown is for an 11.0592MHz crystal manufactured by Fox.

Note 2: Reset delay is a synchronous counter of crystal oscillations after crystal startup. At 33MHz, this time is 1.99ms.

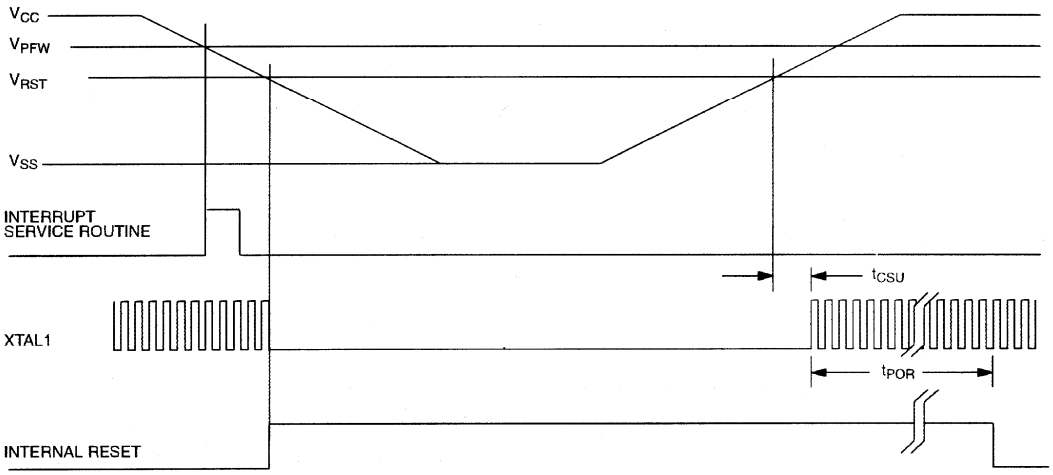
EPROM PROGRAMMING AND VERIFICATION

(V_{CC} = 4.5V to 5.5V, T_A = +21°C to +27°C.)

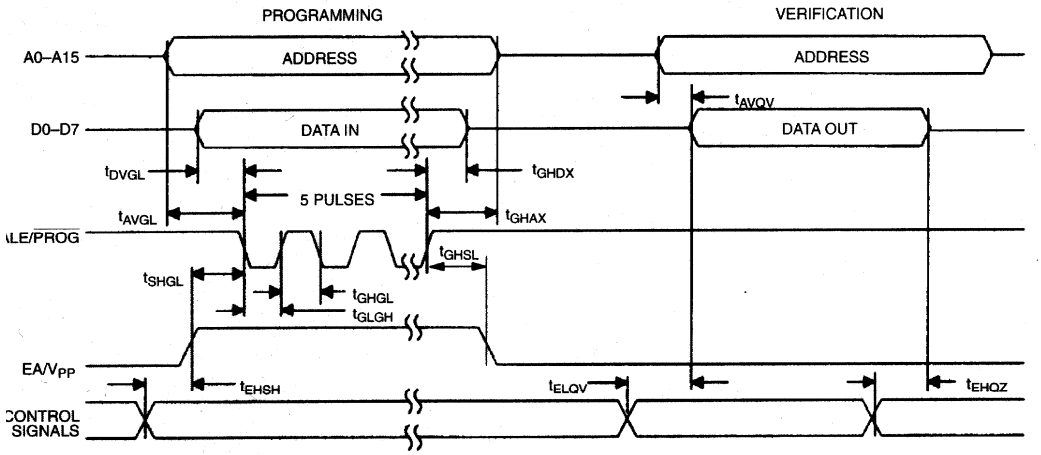
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Programming Voltage	V_{PP}	12.5		13.0	V	1
Programming Supply Current	I_{PP}			50	mA	
Oscillator Frequency	$1/t_{CLCL}$	4		6	MHz	
Address Setup to $\overline{PROG}$ Low	t_{AVGL}	$48t_{CLCL}$				
Address Hold after $\overline{PROG}$	t_{GHAX}	$48t_{CLCL}$				
Data Setup to $\overline{PROG}$ Low	t_{DVGL}	$48t_{CLCL}$				
Data Hold after $\overline{PROG}$	t_{GHDX}	$48t_{CLCL}$				
Enable High to V_{PP}	t_{EHSH}	$48t_{CLCL}$				
V_{PP} Setup to $\overline{PROG}$ Low	t_{SHGL}	10			µs	
V_{PP} Hold after $\overline{PROG}$	t_{GHSL}	10			µs	
$\overline{PROG}$ Width	t_{GLGH}	90		110	µs	
Address to Data Valid	t_{AVQV}			$48t_{CLCL}$		
Enable Low to Data Valid	t_{ELQV}			$48t_{CLCL}$		
Data Float after Enable	t_{EHQZ}	0		$48t_{CLCL}$		
$\overline{PROG}$ High to $\overline{PROG}$ Low	t_{GHGL}	10			µs	

Note 1: All voltages are referenced to ground.

POWER-CYCLE TIMING



EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



DATA SHEET REVISION SUMMARY

REVISION	DESCRIPTION
071107	1) Corrected P1.5 pin for TQFP package from 4 to 1 (page 5).
070505	2) Added Pb-free/RoHS-compliant part numbers to Ordering Information table. 3) Deleted the "A" from the IPC/JEDEC J-STD-020 specification in the Absolute Maximum Ratings.
040104	4) Removed "Preliminary" status. 5) Soldering temperature parameter now references JEDEC specification. 6) Added note to absolute maximums clarifying voltages referenced to ground and storage temperature. 7) Updated I_{CC}, I_{IDLE}, I_{STOP}, I_{SPBG}, I_{IL}, and I_{TL} to incorporate errata conditions. 8) Added note clarifying DC electrical test conditions. 9) Added note clarifying V_{OH3} specification applies to first clock cycle following the transition. 10) Updated AC and MOVX electrical characteristics with final characterization values. 11) Added t_{AVLL2} specification and corrected MOVX timing diagrams to show t_{AVLL2} instead of t_{AVLL}. 12) Updated I_{BAT} to incorporate errata conditions.
112299	Contact factory for details.
070798	1) Added DS83C530 to data sheet. 2) Updated PMM operating current estimates. 3) Added note to clarify I_{IL} specification. 4) Added note to prevent accidental corruption of Watchdog Timer count while changing counter length. 5) Changed I_{BAT} specification to 1µA over extended temperature range. 6) Changed minimum oscillator frequency to 1MHz when using external crystal. 7) Changed RST pulldown resistance from 170kΩ to 200kΩ maximum. 8) Corrected "Data memory write with stretch" diagrams to show falling edge of ALE coincident with rising edge of C3 clock.
022097	1) Updated ALE pin description. 2) Added note pertaining to erasure window. 3) Added note pertaining to internal MOVX SRAM. 4) Changed Note 6 from RST=5.5V to RST=V_{CC}. 5) Changed Note 10 from RST=5.5V to RST=V_{CC}. 6) Changed serial port mode 0 timing diagram label from t_{QVXL} to t_{QVXH}. 7) Added information pertaining to 52-pin TQFP package.
060895	Initial release.

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