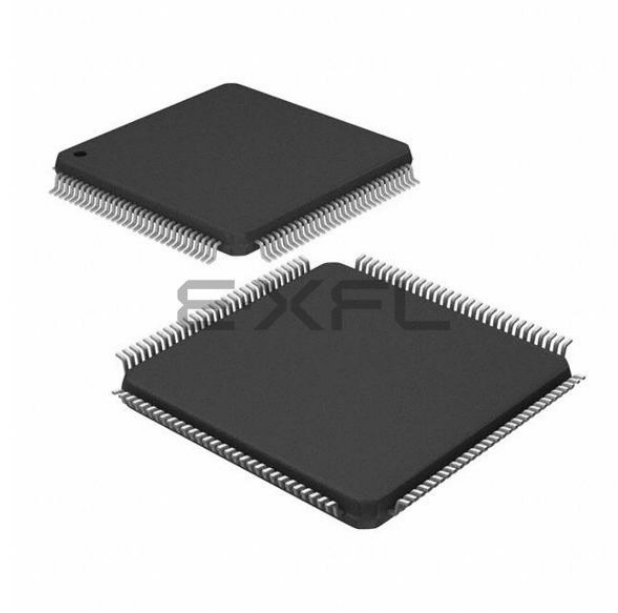

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Xstormy16
Core Size	16-Bit
Speed	10MHz
Connectivity	I²C, SIO, UART/USART
Peripherals	LCD, PWM, WDT
Number of I/O	20
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 12x8/12b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	120-TQFP
Supplier Device Package	120-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/onsemi/lc88f85d0au-tqfp-h

■Serial interfaces

- SIO0: 8-bit synchronous SIO
  <1> LSB first/MSB first selectable
  <2> Supports communication of less than 8 bits (1 to 8 bits specifiable).
  <3> Built-in 8-bit baudrate generator (transfer clock cycles of 4 tCYC to 512 tCYC)
  <4> Automatic continuous data transfer (9 to 32768 bits specifiable in 1-bit units)
  <5> Interval function (interval time specifiable in 0 to 64 tSCK units)
  <6> Wakeup function
- SMIIC0: Single-master I^2C/8-bit synchronous SIO
  Mode 0: Single-master master mode communication
  Mode 1: 8-bit synchronous serial I/O (MSB first)
- UART0
  <1> Data length: 8 bits (LSB first)
  <2> Start bits: 1 bit
  <3> Stop bits: 1 bit
  <4> Parity bits: None/even parity/odd parity
  <5> Transfer rate: 4/8 tCYC
  <6> Baudrate clock source: The P07 input signal is used as a 1 cycle signal (T0PWMH can be used as the clock source) or a timer 4 period.
  <7> Full duplex communication
- UART2
  <1> Data length: 8 bits (LSB first)
  <2> Start bits: 1 bit
  <3> Stop bits: 1/2 bit
  <4> Parity bit: None/even parity/odd parity
  <5> Transfer rate: 8 to 4096 tCYC
  <6> Baudrate clock source: System clock/OSC0/OSC1/P21 input signal
  <7> Wakeup function
  <8> Full duplex communication

■AD converter

<1> 8/12-bit resolution selectable
<2> Analog inputs: 12 channels
<3> Comparator mode
<4> Automatic reference voltage generation

■Watchdog timer

<1> Runs on the base timer + internal watchdog timer dedicated counter.
<2> Interrupt or reset signals selectable

■Infrared remote control receiver

<1> Noise rejection function
(Noise filter time constant: Approx. 120μs when the 32.768kHz crystal oscillator is selected as the reference clock source)
<2> Supports PPM (Pulse Position Modulation), Manchester and other encoding systems.
<3> HOLDX mode release function

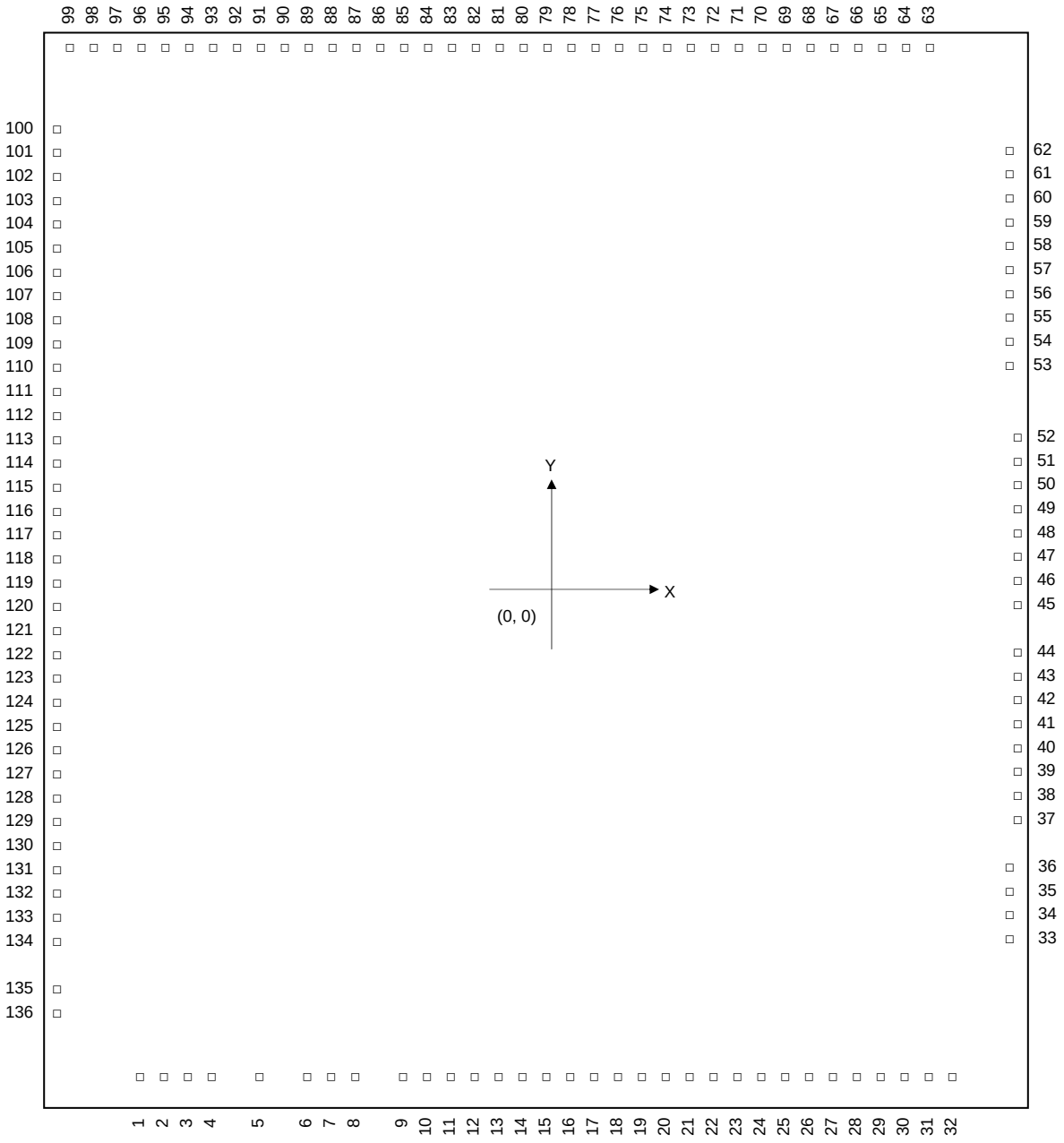
■Interrupts (peripheral function)

Either "Normal" or "LC888300 Compatible" mode is selectable by user option.
* Note: The "LC888300 Compatible" mode is an option that is available to provide compatibility between this model and the LC888300. It is to be unavailable in future developed models.

<1> Provides three levels of multiplex interrupt control. Any interrupt request of the level equal to or lower than the current interrupt is not accepted.
<2> When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

Pad Assignment

- Chip size (X × Y) : 4.10mm × 3.40mm
- PAD opening siz : 59μm
- PAD pitch : 80μm
- Chip thickness : 280μm ± 20μm



- Note: Package pin numbers differ from chip pad numbers. The numbers shown in the above figure are pad numbers.

Table of PAD Coordinates

Pad No.	Pin Name	Coordinate		Pad No.	Pin Name	Coordinate	
		X μm	Y μm			X μm	Y μm
1	$V_{LCD}4$	-1647.9	-1569.9	48	SEG52	1958.5	208.2
2	$V_{LCD}3$	-1567.9	-1569.9	49	SEG51	1958.5	298.2
3	$V_{LCD}2$	-1483.2	-1569.9	50	SEG50	1958.5	388.2
4	$V_{LCD}1$	-1403.2	-1569.9	51	SEG49	1958.5	478.2
5	TST	-1184.0	-1569.9	52	SEG48	1958.5	568.2
6	XT2	-890.0	-1569.9	53	SEG47	1919.9	710.0
7	XT1	-781.5	-1569.9	54	SEG46	1919.9	790.0
8	RESB	-670.0	-1569.9	55	SEG45	1919.9	870.0
9	V_{DD}	-494.5	-1569.9	56	SEG44	1919.9	950.0
10		-374.5	-1569.9	57	SEG43	1919.9	1030.0
11		-263.5	-1569.9	58	SEG42	1919.9	1110.0
12	CF1	-165.0	-1569.9	59	SEG41	1919.9	1190.0
13	CF2	-85.0	-1569.9	60	SEG40	1919.9	1280.0
14	V_{SS}	10.0	-1569.9	61	SEG39	1919.9	1370.0
15		110.0	-1569.9	62	SEG38	1919.9	1460.0
16		210.0	-1569.9	63	$LCDV_{SS}1$	1420.0	1569.9
17	P00	300.0	-1569.9	64	SEG37	1300.0	1569.9
18	P01	380.0	-1569.9	65	SEG36	1190.0	1569.9
19	P02	460.0	-1569.9	66	SEG35	1080.0	1569.9
20	P03	540.0	-1569.9	67	SEG34	990.0	1569.9
21	P04	620.0	-1569.9	68	SEG33	910.0	1569.9
22	P05	700.0	-1569.9	69	SEG32	830.0	1569.9
23	P06	780.0	-1569.9	70	SEG31	750.0	1569.9
24	P07	860.0	-1569.9	71	SEG30	670.0	1569.9
25	P10	940.0	-1569.9	72	SEG29	590.0	1569.9
26	P11	1020.0	-1569.9	73	SEG28	510.0	1569.9
27	P12	1100.0	-1569.9	74	SEG27	430.0	1569.9
28	P13	1180.0	-1569.9	75	SEG26	350.0	1569.9
29	P14	1260.0	-1569.9	76	SEG25	270.0	1569.9
30	P15	1340.0	-1569.9	77	SEG24	190.0	1569.9
31	P16	1420.0	-1569.9	78	SEG23	110.0	1569.9
32	P17	1500.0	-1569.9	79	SEG22	30.0	1569.9
33	P20	1919.9	-1415.0	80	SEG21	-50.0	1569.9
34	P21	1919.9	-1325.0	81	SEG20	-130.0	1569.9
35	P22	1919.9	-1192.0	82	SEG19	-210.0	1569.9
36	P23	1919.9	-1057.0	83	SEG18	-290.0	1569.9
37	SEG63	1958.5	-871.8	84	SEG17	-370.0	1569.9
38	SEG62	1958.5	-781.8	85	SEG16	-450.0	1569.9
39	SEG61	1958.5	-691.8	86	-	-	-
40	SEG60	1958.5	-601.8	87	COM31/SEG15	-620.0	1569.9
41	SEG59	1958.5	-511.8	88	-	-	-
42	SEG58	1958.5	-421.8	89	COM30/SEG14	-780.0	1569.9
43	SEG57	1958.5	-331.8	90	-	-	-
44	SEG56	1958.5	-241.8	91	COM29/SEG13	-940.0	1569.9
45	SEG55	1958.5	-61.8	92	-	-	-
46	SEG54	1958.5	28.2	93	COM28/SEG12	-1100.0	1569.9
47	SEG53	1958.5	118.2	94	-	-	-

Continued on next page.

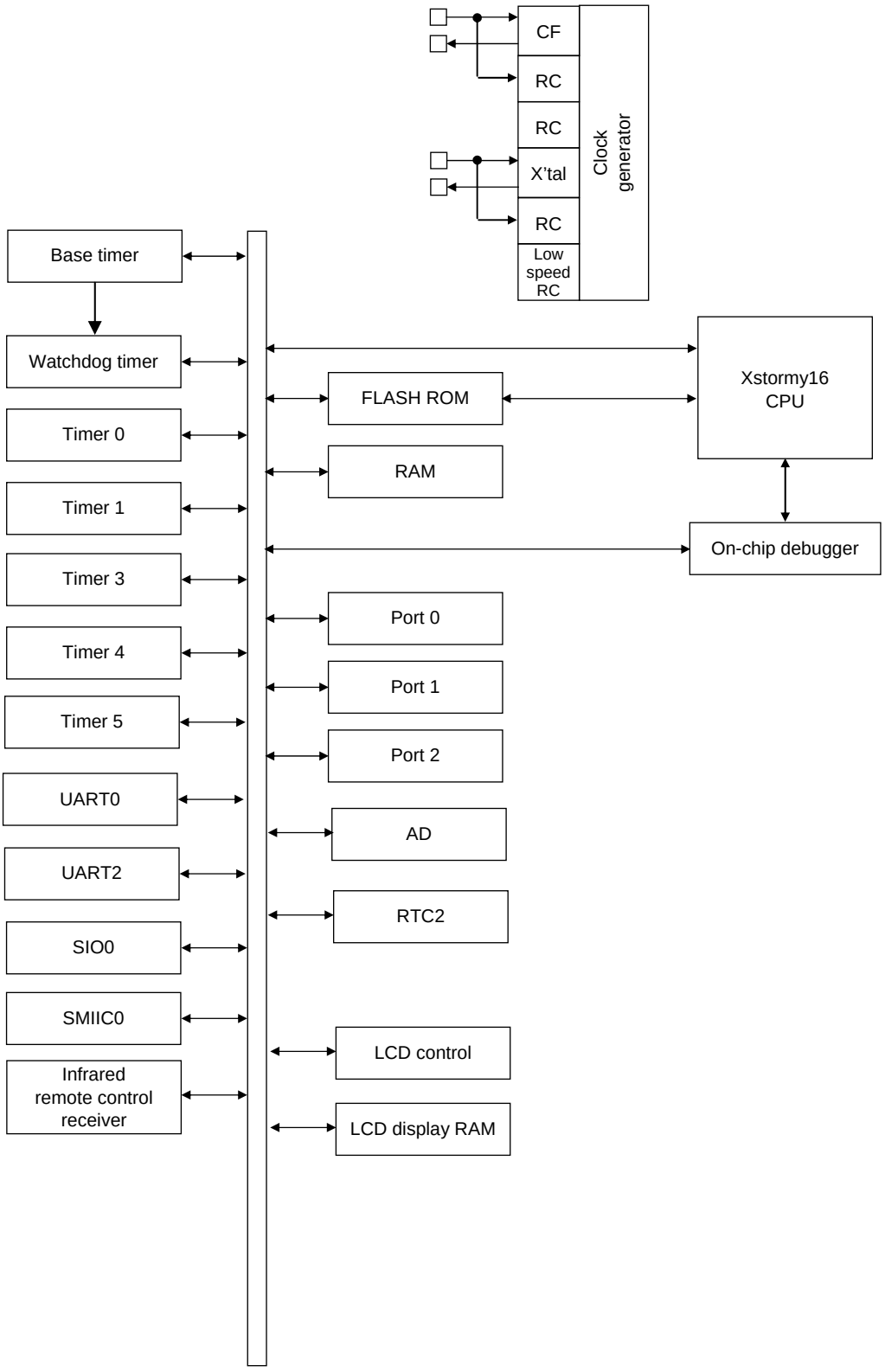
Continued from preceding page.

Pad No.	Pin Name	Coordinate		Pad No.	Pin Name	Coordinate	
		X μm	Y μm			X μm	Y μm
95	COM27/SEG11	-1260.0	1569.9	116	-	-	-
96	-	-	-	117	COM16/SEG0	-1919.9	60.0
97	COM26/SEG10	-1420.0	1569.9	118	COM15	-1919.9	-20.0
98	-	-	-	119	COM14	-1919.9	-100.0
99	COM25/SEG9	-1580.0	1569.9	120	COM13	-1919.9	-180.0
100	-	-	-	121	COM12	-1919.9	-260.0
101	COM24/SEG8	-1919.9	1340.0	122	COM11	-1919.9	-340.0
102	-	-	-	123	COM10	-1919.9	-420.0
103	COM23/SEG7	-1919.9	1180.0	124	COM9	-1919.9	-500.0
104	-	-	-	125	COM8	-1919.9	-580.0
105	COM22/SEG6	-1919.9	1020.0	126	COM7	-1919.9	-660.0
106	-	-	-	127	COM6	-1919.9	-740.0
107	COM21/SEG5	-1919.9	860.0	128	COM5	-1919.9	-820.0
108	-	-	-	129	COM4	-1919.9	-900.0
109	COM20/SEG4	-1919.9	700.0	130	COM3	-1919.9	-980.0
110	-	-	-	131	COM2	-1919.9	-1060.0
111	COM19/SEG3	-1919.9	540.0	132	COM1	-1919.9	-1140.0
112	-	-	-	133	COM0	-1919.9	-1220.0
113	COM18/SEG2	-1919.9	380.0	134	$LCSV_{SS}0$	-1919.9	-1320.0
114	-	-	-	135	CUP00	-1919.9	-1443.3
115	COM17/SEG1	-1919.9	220.0	136	CUP01	-1919.9	-1523.3

Note:

- The coordinate values shown in the above table represent the coordinates of the pin pads measured with the center coordinates of the IC set to (0, 0).
- There are three pads for each of the V_{DD} and V_{SS} pins. They should be triple bonded.

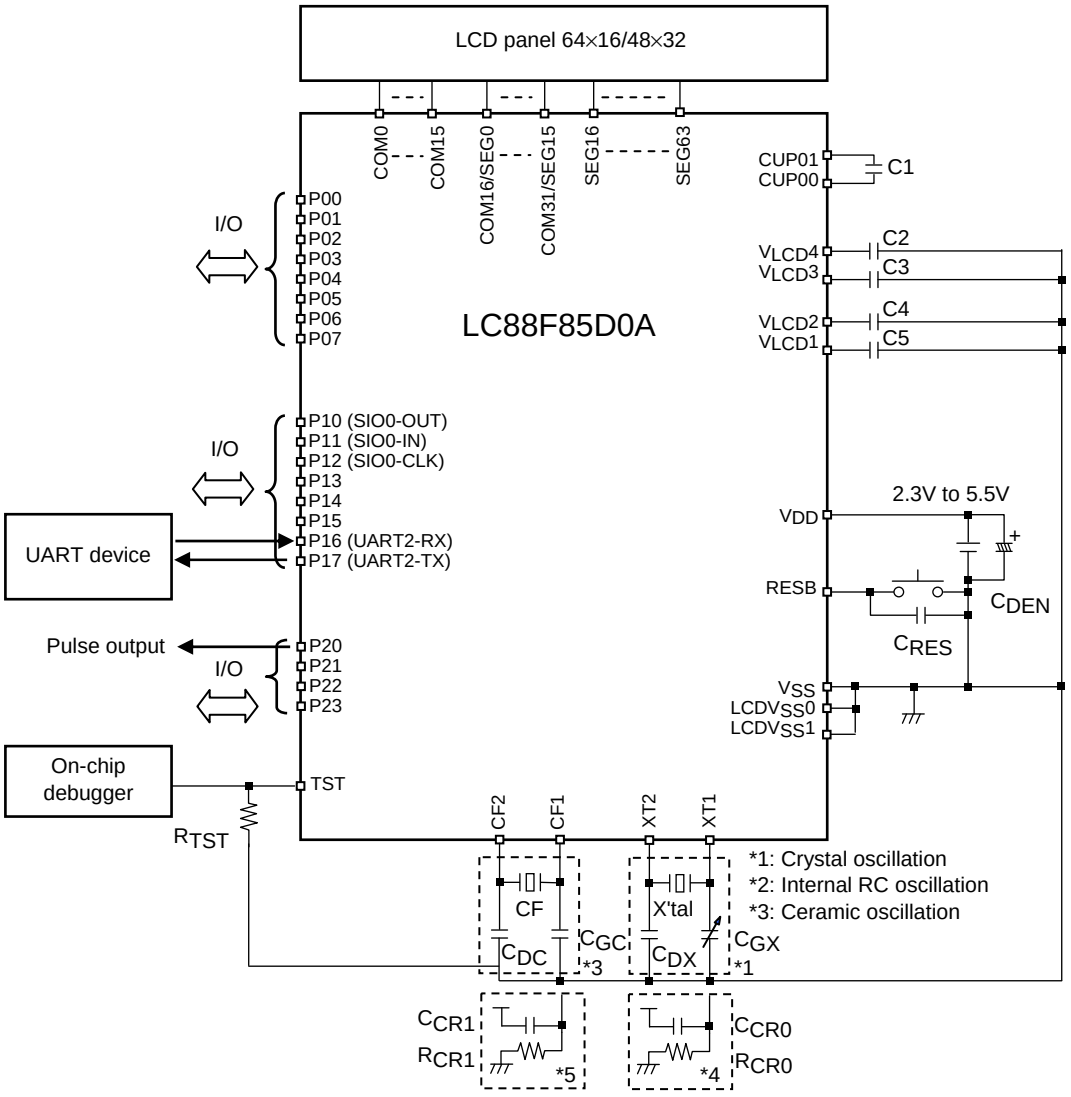
System Block Diagram



Pin Description

Pin Name	I/O	Description
V_{SS}	-	- Power supply pin
V_{DD}	-	+ Power supply pin
$V_{LCD}1$ to 4	-	LCD bias power source (connected to capacitors)
$LCDV_{SS}0$, $LCDV_{SS}1$	-	LCD port power source (-)
CUP00, CUP01	-	Switching pins for generating the LCD drive voltage. A capacitor must be connected across both pins.
PORT 0 P00 to P07	I/O	• 8-bit I/O port • I/O specifiable in 1 bit units • Pull-up registers can be turned on and off in 1-bit units. • HOLD releaset inputs (P00 to P03, P04, P05) • Port 0 interrupt inputs (P00 to P03, P04, P05) • Pin functions P00 (AN8) to P07 (AN15): AD converter inputs P06: Timer 0L output P07: Timer 0H output/UART0 clock input
PORT 1 P10 to P17	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up registers can be turned on and off in 1-bit units. • Pin functions P10: SIO0 data output P11: SIO0 data input/bus input/output P12: SIO0 clock input/output P13: Timer 3L output P14: Timer 3H output/UART0 receive P15: UART0 transmit P16: UART2 receive P17: UART2 transmit
PORT 2 P20 to P23	I/O	• 4-bit I/O port • I/O specifiable in 1-bit units • Pull-up registers can be turned on and off in 1-bit units. • Pin functions P20 (AN0) to P23 (AN3): AD converter inputs P20: Timer 4 output/remote controller receive P21: Timer 5 output P22: SMIIC0 clock input/output P23: SMIIC0 bus input/output/data input
COM0 to COM15	O	• LCD common output
COM16/SEG0 to COM31/SEG15	O	• LCD common output/segment output Common output/segment output switched by a register
SEG16 to SEG47	O	• LCD segment output
SEG48 to SEG63	I/O	• LCD segment output • SEG63-SEG48: General-purpose N-channel open drain output/general-purpose input SEG63-SEG48: LCD output in 4-bit units/general-purpose N-channel open drain output/general-purpose input selectable • SEG63-SEG56: Interrupt function (4-bit units) Chatter removal sampling frequency select (4-bit units) Level/edge sense mode select (4-bit units) Hi/low level or rising/falling edge sense mode select (1-bit units) • SEG63-SEG62: Timer 3 external input
TEST	I/O	• TEST pin • On-chip debugger communication pin • An external 100kΩ pull-down resistor must be connected.
RESB	I	Reset pin
CF1	I	Ceramic oscillator input/RC oscillator resistor to be connected
CF2	O	Ceramic oscillator output
XT1	I	32.768kHz crystal oscillator input/RC oscillator resistor to be connected
XT2	O	32.768kHz crystal oscillator output

Application circuit



X'tal	Crystal resonator	
C_{GX}	Trimmer capacitor	
C_{DX}	Capacitor for X'tal oscillator	
R_{CR0}	Resistor for low-speed oscillator	*4: RC oscillation type
C_{CR0}	Capacitor for low-speed oscillation stabilization	*4: RC oscillation type (*1)
(*1)	0.1µF capacitor is recommended when using XT1/XT2 as the system clock source.	
CF	Ceramic resonator	
C_{GC}	Capacitor for CF oscillator	
C_{DC}	Capacitor for CF oscillator	
R_{CR1}	Resistor for high-speed oscillation	*5: RC oscillation type
C_{CR1}	Capacitor for high-speed oscillation stabilization	*5: RC oscillation type
C1 to C5	Capacitor	
C_{DEN}	Electrolytic capacitor	
C_{RES}	Capacitance for RESB	
R_{TST}	Resistor used when using the on-chip debugger	

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = LCDV_{SS}0 = LCDV_{SS}1 = 0V

Parameter		Symbol	Pin/Remarks	Conditions		Specification			
					V_{DD}[V]	min	typ	max	unit
Maximum supply voltage		V_{DD} max	V_{DD}	V_{DD}		-0.3		+6.5	V
LCD supply voltage		V_{LCD} max	V_{LCD}2 to V_{LCD}4	V_{DD}		-0.3		+6.5	
Maximum LCD supply voltage		LCD max	SEG0 to SEG63 COM0 to COM31	V_{DD}, V_{LCD}4		-0.3		+6.5	
Input voltage		V_I(1)	CF1, XT1, RESB			-0.3		V_{DD}+0.3	
Input/output voltage		V_{IO}(1)	Ports 0, 1, 2 SEG63 to SEG48			-0.3		V_{DD}+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 2	CMOS output select Per 1 applicable pin		-5			mA
		IOPH(2)	Port 1	Per 1 applicable pin		-14			
	Mean output current (Note 1-1)	IOMH(1)	Ports 0, 2	CMOS output select Per 1 applicable pin		-3			
		IOMH(2)	Port 1	CMOS output select Per 1 applicable pin		-9			
	Total output current	ΣIOAH(1)	Ports 0, 2	Total of all applicable pins		-22.5			
		ΣIOAH(2)	Port 1	Total of all applicable pins		-25			
		ΣIOAH(3)	Ports 0, 1, 2	Total of all applicable pins		-47.5			
Low level output current	Peak output current	IOPL(1)	Ports 0, 2	Per 1 applicable pin				13	
		IOPL(2)	Port 1	Per 1 applicable pin				17	
	Mean output current (Note 1-1)	IOML(1)	Ports 0, 2	Per 1 applicable pin				7.5	
		IOML(2)	Port 1	Per 1 applicable pin				10.5	
	Total output current	ΣIOAL(1)	Ports 0, 2	Total of all applicable pins				35	
		ΣIOAL(2)	Port 1	Total of all applicable pins				60	
		ΣIOAL(3)	Ports 0, 1, 2	Total of all applicable pins				80	
Allowable power dissipation		Pd max		Ta=-20 to +75°C				250	mW
Operating ambient temperature		Topr				-20		+75	°C
Storage ambient temperature		Tstg				-65		+125	

Note 1-1: The mean output current is a mean value measured over 100ms.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Conditions at Ta = -20°C to +75°C, V_{SS} = $LCDV_{SS}0$ = $LCDV_{SS}1$ = 0V

Parameter	Symbol	Pin/Remarks	Conditions		Ratings			
				V_{DD}[V]	min	typ	max	unit
Operating supply voltage (Note2-1)	V_{DD}(1)	V_{DD}	0.098µs≤tCYC≤66µs		4.5		5.5	V
			0.123µs≤tCYC≤66µs		3.0		5.5	
			0.490µs≤tCYC≤66µs		2.0		5.5	
LCD drive voltage	V_{LCD}(1)	V_{LCD}2 to V_{LCD}4					5.5	
Memory sustaining supply voltage	VHD	V_{DD}	RAM and register contents sustained in HOLD mode.		2.0		5.5	
High level input voltage	V_{IH}(1)	Ports 0, 1, 2	Output disabled		0.30V_{DD} +0.70		V_{DD}	
	V_{IH}(2)	CF1, RESB			0.75V_{DD}		V_{DD}	
Low level input voltage	V_{IL}(1)	Ports 0, 1, 2	Output disabled		V_{SS}		0.10V_{DD} +0.40	
	V_{IL}(2)	CF1, RESB			V_{SS}		0.25V_{DD}	
Instruction cycle time (Note 2-2)	tCYC			4.5 to 5.5	0.098		66	µs
				3.0 to 5.5	0.123		66	
				2.0 to 5.5	0.490		66	
External system clock frequency	FEXCF(1)	CF1	• CF2 pin open • System clock frequency division ratio=1/1 • External system clock duty=50±5%	4.5 to 5.5	0.1		10	MHz
				3.0 to 5.5	0.1		8	
				2.0 to 5.5	0.1		2	
Oscillation frequency range (Note 2-3)	FmCF(1)	CF1,CF2	10MHz ceramic oscillation See Fig. 1.	4.5 to 5.5		10		MHz
	FmCF(2)	CF1,CF2	8MHz ceramic oscillation See Fig. 1.	3.0 to 5.5		8		
	FmCF(3)	CF1,CF2	4MHz ceramic oscillation See Fig. 1.	2.4 to 5.5		4		

Electrical Characteristics at Ta = -20°C to +75°C, V_{SS} = LCDV_{SS}0 = LCDV_{SS}1 = 0V

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
High level input current	I_{IH}(1)	Ports 0, 1, 2 RESB	Output disabled Pull-up resistor off V_{IN}=V_{DD} (including output Tr off leakage current)	2.0 to 5.5			1	μA
Low level input current	I_{IL}(1)	Ports 0, 1, 2	Output disabled Pull-up resistor off V_{IN}=V_{SS} (including output Tr off leakage current)	2.7 to 5.5	-1			μA
High-level output voltage	V_{OH}(1)	Ports 0, 1, 2	I_{OH}=-1.0mA	4.5 to 5.5	V_{DD}-1			V
	V_{OH}(2)		I_{OH}=-0.4mA	3.0 to 5.5	V_{DD}-0.4			
	V_{OH}(3)		I_{OH}=-0.1mA	2.0 to 5.5	V_{DD}-0.4			
	V_{OH}(4)	COM0 to COM31	I_{OH}=-25μA	2.0 to 5.5	V_{LCD}4 -0.05			
	V_{OH}(5)	SEG0 to SEG63	I_{OH}=-10μA	2.0 to 5.5	V_{LCD}4 -0.05			
Low level output voltage	V_{OL}(1)	Ports 0, 1, 2	I_{OL}(1)=10mA	4.5 to 5.5			1.5	
	V_{OL}(2)		I_{OL}(1)=1.6mA	3.0 to 5.5			0.4	
	V_{OL}(3)		I_{OL}(1)=0.7mA	2.0 to 5.5			0.4	
	V_{OL}(4)	COM0 to COM31	I_{OLH}=25μA	2.0 to 5.5			V_{SS} +0.05	
	V_{OL}(5)	SEG0 to SEG63	I_{OL}=10μA	2.0 to 5.5			V_{SS} +0.05	
Pull-up resistance	Rpu(1)	Ports 0, 1, 2	V_{OH}=0.9V_{DD}	4.5 to 5.5	15	35	80	kΩ
	Rpu(2)			2.0 to 4.5	18	55	180	
Hysteresis voltage	VHYS	Ports 0, 1, 2 RESB		2.0 to 5.5		0.1V_{DD}		V
Pin capacitance	CP	All pins	For pins other than that under test V_{IN}=V_{SS} f=1MHz Ta=25°C	2.0 to 5.5		10		pF

SIO1 Serial I/O Characteristics (When wakeup function is not in used) (Note 4-2-1)

Parameter			Symbol	Pin/Remarks	Conditions		Specification			
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK(3)	SCK0(P12)	• See Fig. 6.	2.0 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
			tSCKHBSY(3)				2			
Serial input	Data setup time		tsDI(2)	SI0(P11), SB0(P11)	• Specified with respect to rising edge of SIOCLK. • See Fig. 6.	2.0 to 5.5	0.03			µs
	Data hold time		thDI(2)				0.03			
Serial output	Input clock	Output delay time	tdD0(3)	SO0(P10), SB0(P11)	• (Note4-2-2)	2.0 to 5.5			1tCYC +0.05	

Note 4-2-1: These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.

Note 4-2-2: Specified with respect to the falling edge of SIOCLK. Specified as the time up to the time the output state is changed in the open drain output mode. See Fig. 6.

SMIIC0 Simple SIO Mode I/O Characteristics

Parameter			Symbol	Pin/Remarks	Conditions		Specification			
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK(7)	SM0CK (P22)	• See Fig. 6.	2.0 to 5.5	4			tCYC
		Low level pulse width	tSCKL(7)				2			
		High level pulse width	tSCKH(7)				2			
	Output clock	Period	tSCK(8)	SM0CK (P22)	• CMOS output type selected • See Fig. 6.		4			
		Low level pulse width	tSCKL(8)				1/2			tSCK
		High level pulse width	tSCKH(8)				1/2			
Serial input	Data setup time		tsDI(5)	SM0DA (P23)	• Specified with respect to rising edge of SIOCLK • See Fig. 6.	2.0 to 5.5	0.03			µs
	Data hold time		thDI(5)				0.03			
Serial output	Output delay time		tdD0(7)	SM0DA (P23)	• Specified with respect to falling edge of SIOCLK • Specified as the time up to the beginning of output change . • See Fig. 6.	2.0 to 5.5			1tCYC +0.05	

Note 4-3-1: These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.

SMIIC0 I²C Mode I/O Characteristics

Parameter			Symbol	Pin/Remarks	Conditions	Specification				
						V_{DD}[V]	min	typ	max	unit
Clock	Input clock	Period	tSCL	SM0CK (P22)	• See Fig. 8.	2.0 to 5.5	5			Tfilt
		Low level pulse width	tSCLL				2.5			
		High level pulse width	tSCLH				2			
	Output clock	Period	tSCLx	SM0CK (P22)	• Specified as the time up to the beginning of output change.	2.0 to 5.5	10			tSCL
		Low level pulse width	tSCLLx				1/2			
		High level pulse width	tSCLHx				1/2			
SM0CK, SM0DA pin input spike suppression time			tsp	SM0CK(P22) SM0DA(P23)	• See Fig. 8.	2.0 to 5.5			1	Tfilt
Start-to-stop period bus release time	Input		tBUF	SM0CK(P22) SM0DA(P23)	• See Fig. 8.	2.0 to 5.5	2.5			Tfilt
	Output		tBUFx	SM0CK(P22) SM0DA(P23)	• Standard clock mode • Specified as the time up to the beginning of output change.		5.5			µs
					• High-speed clock mode • Specified as the time up to the beginning of output change.		1.6			
Start/restart condition hold time	Input		tHD;STA	SM0CK(P22) SM0DA(P23)	• When SMIIC register control bit I²CSHDS=0 • See Fig. 8.	2.0 to 5.5	2.0			Tfilt
					• When SMIIC register control bit I²CSHDS=1 • See Fig. 8.		2.5			
	Output		tHD;STAx	SM0CK(P22) SM0DA(P23)	• Standard clock mode • Specified as the time up to the beginning of output change.		4.1			µs
					• High-speed clock mode • Specified as the time up to the beginning of output change.		1.0			
Restart condition setup time	Input		tSU;STA	SM0CK(P22) SM0DA(P23)	• See Fig. 8.	2.0 to 5.5	1.0			Tfilt
	Output		tSU;STAx	SM0CK(P22) SM0DA(P23)	• Standard clock mode • Specified as the time up to the beginning of output change.		5.5			µs
					• High-speed clock mode • Specified as the time up to the beginning of output change.		1.6			

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Parameter		Symbol	Pin/Remarks	Conditions	Specification				
					V_{DD}[V]	min	typ	max	Unit
Stop condition setup time	Input	tSU;STO	SM0CK(P22) SM0DA(P23)	• See Fig. 8.	2.0 to 5.5	1.0			Tfilt
	Output	tSU;STOx	SM0CK(P22) SM0DA(P23)	• Standard clock mode • Specified as the time up to the beginning of output change.		4.9			µs
				• High-speed clock mode • Specified as the time up to the beginning of output change.		1.1			
Data hold time	Input	tHD;DAT	SM0CK(P22) SM0DA(P23)	• See Fig. 8.	2.0 to 5.5	0			Tfilt
	Output	tHD;DATx	SM0CK(P22) SM0DA(P23)	• Specified as the time up to the beginning of output change.		1		1.5	
Data setup time	Input	tSU;DAT	SM0CK(P22) SM0DA(P23)	• See Fig. 8.	2.0 to 5.5	1			Tfilt
	Output	tSU;DATx	SM0CK(P22) SM0DA(P23)	• Specified as the time up to the beginning of output change.		1tSCL-1.5Tfilt			
SM0CK, SM0DA pin fall time	Input	tF	SM0CK(P22) SM0DA(P23)	• See Fig. 8.	2.0 to 5.5			300	ns
	Output	tF	SM0CK(P22) SM0DA(P23)	• When SMIIC register control bits PSLW=1, P5V=1	5	20+0.1Cb		250	
				• When SMIIC register control bits PSLW=1, P5V=0	3	20+0.1Cb		250	
				• When SM0CK and SM0DA port outputs are placed in fast mode • Cb≤400pF	3.0 to 5.5			100	

Note 4-4-1: These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.

Note 4-4-2: Tfilt denotes the value that is determined by the values of register SMIC0BRG, bits 7 and 6 (BRP1, BRP0) and the system clock frequency.

BRP1	BRP0	Tfilt
0	0	tCYC×1
0	1	tCYC×2
1	0	tCYC×3
1	1	tCYC×4

Set up (BPR1, BPR0) so that Tfilt falls within the following range:

250ns ≥ Tfilt > 140ns

Note 4-4-3: Cb denotes the total capacitance (in pF) of the loads connected to each bus. Cb ≤ 400pF

Note 4-4-4: The standard clock mode refers to a mode that is entered by configuring SMIC0BRG within the following ranges:

250ns ≥ Tfilt > 140ns

BRDQ (bit 5) = 1

SCL frequency setting ≤ 100kHz

The high-speed clock mode refers to a mode that is entered by configuring SMIC0BRG as follows:

250ns ≥ Tfilt > 140ns

BRDQ (bit 5) = 0

SCL frequency setting ≤ 400kHz

UART0 Operating Conditions at Ta = -20 to +75°C, V_{SS} = LCDV$_{SS}$0 = LCDV$_{SS}$1 = 0V

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Transfer rate	UBR0	U0RX(P14), U0TX(P15), U0BRG(P07)		2.0 to 5.5	4		8	tBGCYC

Note 4-5: tBGCYC denotes 1 period of the baudrate clock source.

UART2 Operating Conditions at Ta = -20 to +75°C, V_{SS} = LCDV$_{SS}$0 = LCDV$_{SS}$1 = 0V

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Transfer rate	UBR2	U2RX(P16), U2TX(P17)		2.0 to 5.5	8		4096	tBGCYC

Note 4-6: tBGCYC denotes 1 period of the baudrate clock source.

Pulse Input Conditions at Ta = -20 to +75°C, V_{SS} = LCDV$_{SS}$0 = LCDV$_{SS}$1 = 0V

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
	tPIL(2)	RESB	Resettable.	2.0 to 5.5	10			μs

AD Converter Characteristics at Ta = -20 to +75°C, V_{SS} = LCDV$_{SS}$0 = LCDV$_{SS}$1 = 0V

12-bits AD Conversion Mode

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Resolution	NAD	AN0(P20), AN1(P21), AN2(P22), AN3(P23), AN8(P00) to AN15(P07)		2.9 to 5.5		12		bit
Absolute accuracy	ETAD		(Note 6-1)	2.9 to 5.5			±16	LSB
Conversion time	TCAD12		Conversion time is calculated.	4.5 to 5.5	27		209	μs
				2.9 to 5.5	67		209	
Analog input voltage range	VAIN							

8.5(S72. 59U8BT7.9246536-ref2329brgSSBT48001 reit6584 remax)8V32. 59U8BT7.02468 r5

Consumption Current Characteristics at Ta = -20 to +75°C, V_{SS} = $LCDV_{SS}0$ = $LCDV_{SS}1$ = 0V

Parameter	Symbol	Pin/ Remarks	Conditions		V_{DD}[V]	Specification min	typ	max	unit
Normal mode consumption current (Note 7-1)	IDDOP(1)	V_{DD}	• FOSC0=32.768kHz • System clock set to FOSC0 side • Internal RC oscillation stopped • FOSC1=0Hz (oscillation stopped) • Frequency division ratio set to 1/1 • Normal XT mode [No panel load]	LCD display ON	2.0 to 5.5		87	170	µA
	IDDOP(2)				2.0 to 3.6		44	110	
	IDDOP(3)			LCD display OFF	2.0 to 5.5		75	155	
	IDDOP(4)				2.0 to 3.6		35	95	
	IDDOP(5)		• FOSC0=32.768kHz • System clock set to FOSC0 side • Internal RC oscillation stopped • FOSC1=0Hz (oscillation stopped) • Frequency division ratio set to 1/1 • Low power XT mode [No panel load]	LCD display ON	2.0 to 5.5		53	100	
	IDDOP(6)				2.0 to 3.6		35	65	
	IDDOP(7)			LCD display OFF	2.0 to 5.5		48	92	
	IDDOP(8)				2.0 to 3.6		31	55	
	IDDOP(9)		• FmCF=10MHz ceramic oscillator • FOSC0=0Hz (oscillation stopped) • System clock set to 10MHz side • Internal RC oscillation stopped • Frequency division ratio set to 1/1		4.5 to 5.5		8.4	15.2	mA
	IDDOP(10)		• FmCF=8MHz ceramic oscillator oscillator • FOSC0=0Hz (oscillation stopped) • System clock set to 8MHz side • Internal RC oscillation stopped • Frequency division ratio set to 1/1		4.5 to 5.5		7.6	14.7	
	IDDOP(11)				3.0 to 4.5		5.8	11	
	IDDOP(12)		• FmCF=4MHz ceramic oscillator • FOSC0=0Hz (oscillation stopped) • System clock set to 4MHz • Internal RC oscillation stopped • Frequency division ratio set to 1/2		4.5 to 5.5		3.6	5.5	
	IDDOP(13)				2.2 to 4.5		2.2	4.7	
	IDDOP(14)		• System clock set to internal RC side • Internal RC oscillation oscillated • FOSC0=0Hz (oscillation stopped) • FOSC1=0Hz (oscillation stopped) • Frequency division ratio set to 1/1		2.0 to 5.5		2.2	5.6	
	IDDOP(15)				2.0 to 3.6		1.2	3.6	
	IDDOP(16)		• FOSC1=1MHz R_{CR1}=470kΩ • System clock set to FOSC1 side • Internal RC oscillation stopped • FOSC0=0Hz (oscillation stopped) • Frequency division ratio set to 1/1 *Ta=0 to 60°C		2.0 to 5.5		1.5	2.6	
	IDDOP(17)				2.0 to 3.6		1.0	2.5	
	IDDOP(18)		• FOSC0=64kHz R_{CR0}=910kΩ • System clock set to FOSC0 side • Internal RC oscillation stopped • FOSC1=0Hz (oscillation stopped) • Frequency division ratio set to 1/1 *Ta=0 to 60°C		2.0 to 5.5		100	187	µA
	IDDOP(19)				2.0 to 3.6		62	120	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

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Parameter	Symbol	Pin/ Remarks	Conditions		Specification				
					V_{DD}[V]	min	typ	max	unit
HALT mode consumption current (Note 7-2)	IDDHALT(1)	V_{DD}	HALT mode • FOSC0=32.768kHz • System clock set to FOSC0 side • Internal RC oscillation stopped • FOSC1=0Hz (oscillation stopped) • Frequency division ratio set to 1/1 • Normal XT mode [No panel load]	LCD display ON	2.0 to 5.5		45	110	µA
	IDDHALT(2)				2.0 to 3.6		16	50	
	IDDHALT(3)			LCD display OFF	2.0 to 5.5		36	90	
	IDDHALT(4)				2.0 to 3.6		7.8	51	
	IDDHALT(5)		HALT mode • FOSC0=32.768kHz • System clock set to FOSC0 side • Internal RC oscillation stopped • FOSC1=0Hz (oscillation stopped) • Frequency division ratio set to 1/1 • Low power XT mode [No panel load]	LCD display ON	2.0 to 5.5		15.5	53	
	IDDHALT(6)				2.0 to 3.6		12	30	
	IDDHALT(7)			LCD display OFF	2.0 to 5.5		6.5	40	
	IDDHALT(8)				2.0 to 3.6		4	30	
	IDDHALT(9)		HALT mode • FmCF=10MHz ceramic oscillator • FOSC0=0Hz (oscillation stopped) • System clock set to 10MHz side • Internal RC oscillation stopped • Frequency division ratio set to 1/1		4.5 to 5.5		2.0	3.4	mA
	IDDHALT(10)		HALT mode • FmCF=8MHz ceramic oscillator • Internal RC oscillation stopped • FOSC0=0Hz (oscillation stopped) • System clock set to 8MHz side • Internal RC oscillation stopped • Frequency division ratio set to 1/1		4.5 to 5.5		1.7	2.9	
	IDDHALT(11)				3.0 to 4.5		1.2	2.1	
	IDDHALT(12)		HALT mode • FmCF=4MHz ceramic oscillator • FOSC0=0Hz (oscillation stopped) • System clock set to 4MHz side • Internal RC oscillation stopped • Frequency division ratio set to 1/2		4.5 to 5.5		0.7	1.2	
	IDDHALT(13)				2.2 to 4.5		0.3	0.85	
	IDDHALT(14)		HALT mode • System clock set to internal RC side • Internal RC oscillation oscillated • FOSC0=0Hz (oscillation stopped) • FOSC1=0Hz (oscillation stopped) • Frequency division ratio set to 1/1		2.0 to 5.5		0.7	1.3	
	IDDHALT(15)				2.0 to 3.6		0.3	0.6	
	IDDHALT(16)		HALT mode • FOSC1=1MHz R_{CR1}=470kΩ • System clock set to FOSC1 side • Internal RC oscillation stopped • FOSC0=0Hz (oscillation stopped) • Frequency division ratio set to 1/1 *Ta=0 to 60°C		2.0 to 5.5		0.2	0.5	
	IDDHALT(17)				2.0 to 3.6		0.1	0.3	
	IDDHALT(18)		HALT mode • FOSC0=64kHz R_{CR0}=910kΩ • System clock set to FOSC0 side • Internal RC oscillation stopped • FOSC1=0Hz (oscillation stopped) • Frequency division ratio set to 1/1 *Ta=0 to 60°C		2.0 to 5.5		20	60	µA
	IDDHALT(19)				2.0 to 3.6		10	40	

Note 7-2: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

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Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
HOLD mode consumption current	IDDHOLD(1)	V_{DD}	HOLD mode • CF1=V_{DD} or open (external clock mode)	2.0 to 5.5		0.08	35	µA
	IDDHOLD(2)			2.0 to 3.6		0.02	25	
HOLDX mode consumption current	IDDHOLD(3)		HOLDX mode • CF1=V_{DD} or open (external clock mode) • FOSC0=32.768kHz • Normal XT mode	2.0 to 5.5		30	65	
	IDDHOLD(4)			2.0 to 3.6		5	55	
	IDDHOLD(5)		HOLDX mode • CF1=V_{DD} or open (external clock mode) • FOSC0=32.768kHz • Low power XT mode	2.0 to 5.5		0.6	35	
	IDDHOLD(6)			2.0 to 3.6		0.4	25	

Note 7-3: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

F-ROM Writing Characteristics at Ta = +10°C to +55°C, V_{SS} = $LCDV_{SS}0$ = $LCDV_{SS}1$ = 0V

Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Onboard writing current	IDDFW(1)	V_{DD}	• Excluding power dissipation in the microcontroller block	3.0 to 5.5			15	mA
Writing time	tFW(1)		• 512-/1K-byte erase operation	3.0 to 5.5			30	ms
	tFW(2)		• 2-byte writing operation	3.0 to 5.5			60	µs

Characteristics of a Sample OSC1 System Clock Oscillation Circuit

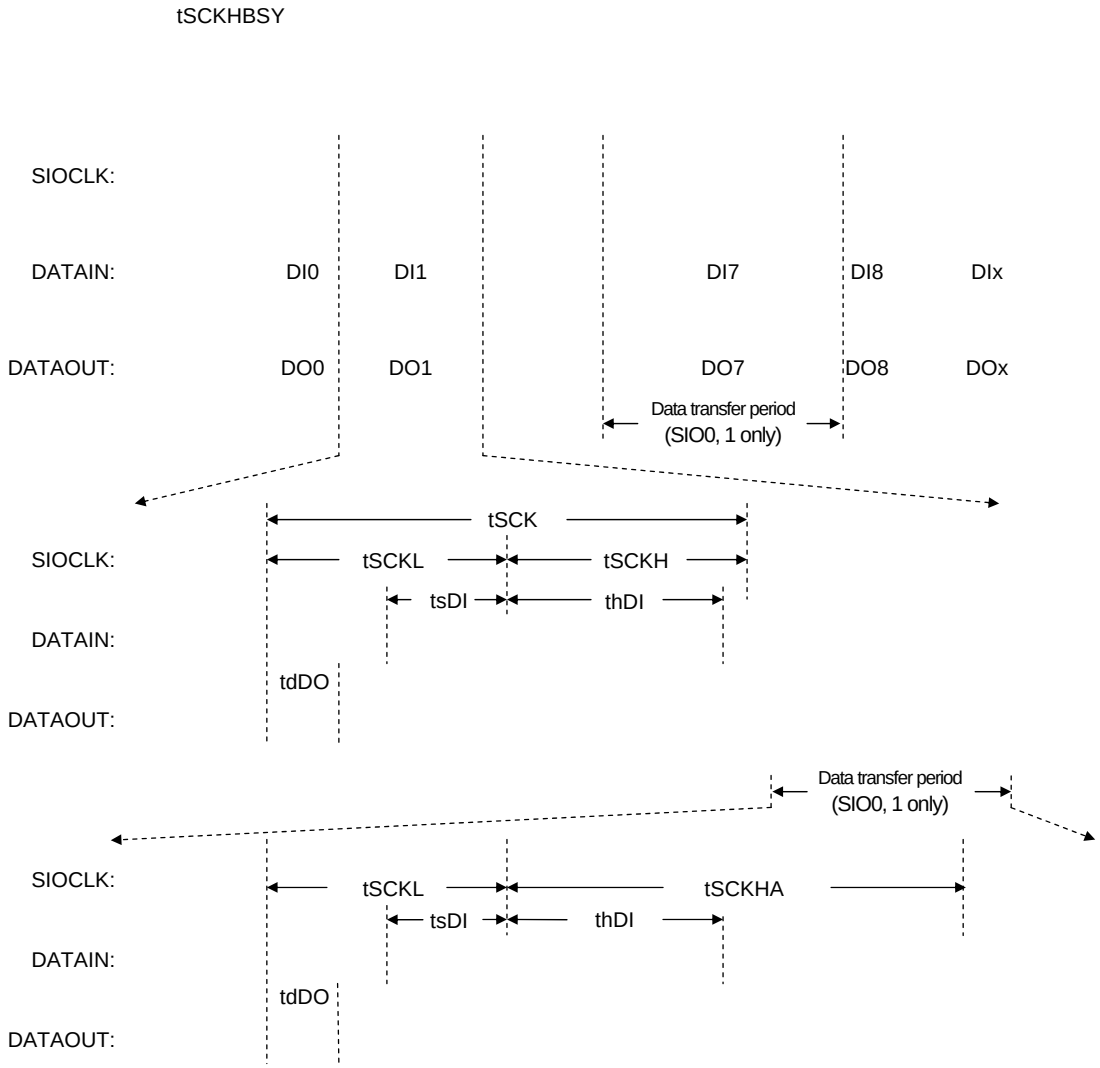
Sample main system clock oscillation circuit characteristics

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of the Main System Clock Oscillation Circuit that Uses a Ceramic Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf [Ω]	Rd2 [Ω]		typ [ms]	max [ms]	
10MHz	MURATA Manufacturing Co., Ltd.	CSTCE10M0G52-R0	(10)	(10)	OPEN	150	2.4 to 5.5	0.02	0.5	C1 and C2 integrated type
8MHz		CSTCE8M00G52-R0	(10)	(10)	OPEN	470	2.4 to 5.5	0.02	0.5	C1 and C2 integrated type
4MHz		CSTCR4M00G53-R0	(15)	(15)	OPEN	1.5K	2.2 to 5.5	0.02	0.5	C1 and C2 integrated type
		CSTCR4M00G53095-R0	(15)	(15)	OPEN	1.5K	2.0 to 5.5	0.02	0.5	C1 and C2 integrated type

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} exceeds its lower limit operating voltage (see Figure 4).



*: Remarks: DIx and DOx are the final communication bits. X = 0 to 32768

Figure 6 Serial I/O Waveforms Examples

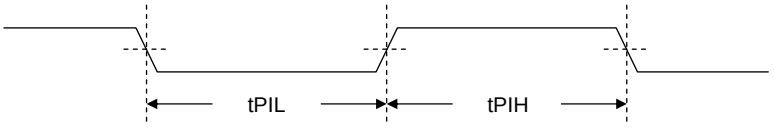
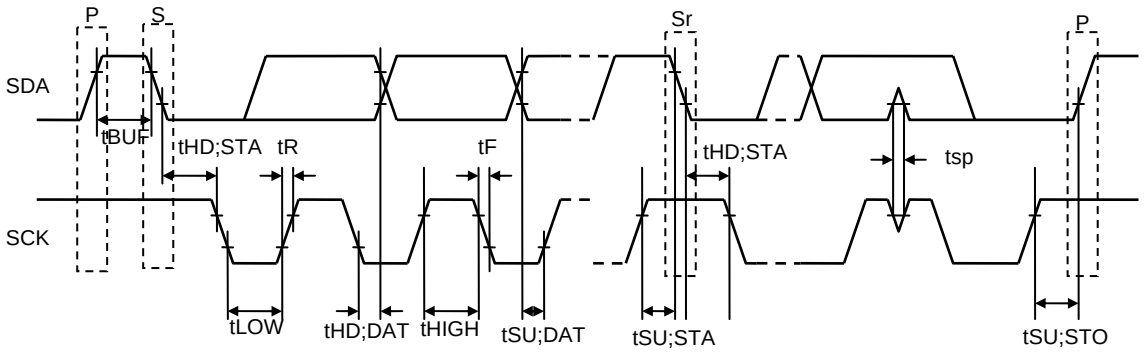


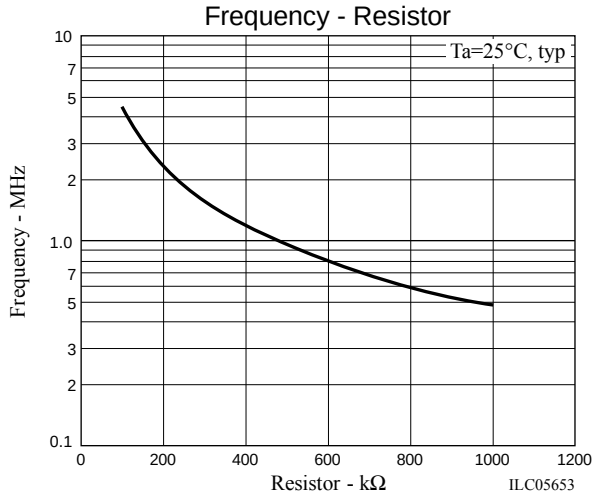
Figure 7 Pulse Input Timing Signal Waveform



S: Start condition
P: Stop condition
Sr: Restart condition

Figure 8 I^2C Timing

Note: The oscillation frequency of any RC oscillator using OSC1 or OSC0 varies according to the printed circuit patterns and components mounted on the board. It also varies greatly according to the shape and form of the product (chip, plastic package, etc.) and board capacitance. Consequently, the characteristics charts given below should be used merely as reference values and the resistance value be determined after evaluating them with the actual product.



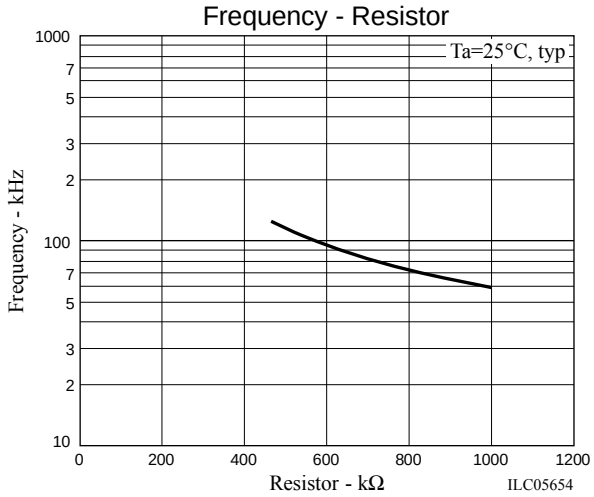


Figure 9 OSC1 Oscillation Frequency vs. Resistance Characteristics