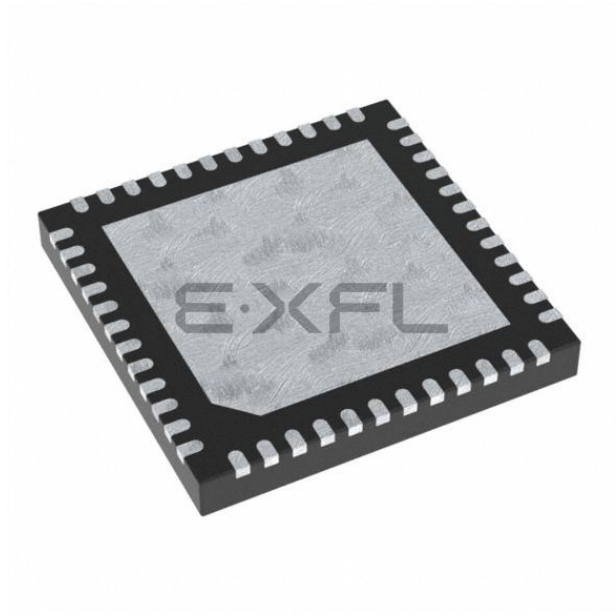

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	LED, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89c5131a-pltil

Description

AT89C5131A-L is a high-performance Flash version of the 80C51 single-chip 8-bit microcontrollers with full speed USB functions.

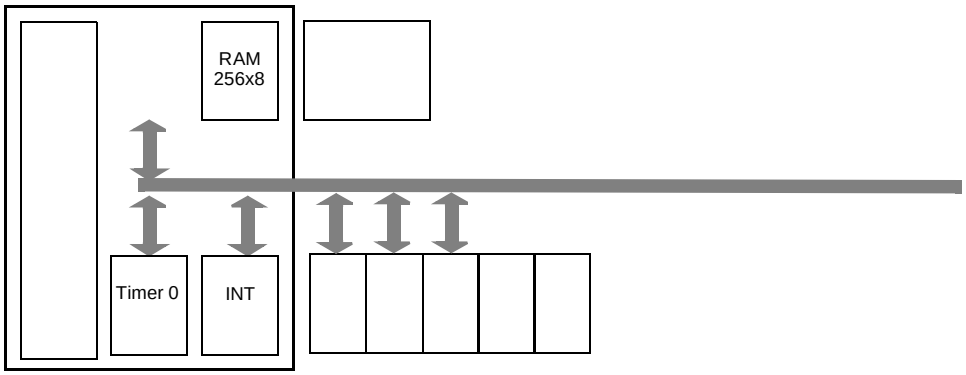
AT89C5131A-L features a full-speed USB module compatible with the USB specifications Version 1.1 and 2.0. This module integrates the USB transceivers with a 3.3V voltage regulator and the Serial Interface Engine (SIE) with Digital Phase Locked Loop and 48 MHz clock recovery. USB Event detection logic (Reset and Suspend/Resume) and FIFO buffers supporting the mandatory control Endpoint (EP0) and up to 6 versatile Endpoints (EP1/EP2/EP3/EP4/EP5/EP6) with minimum software overhead are also part of the USB module.

AT89C5131A-L retains the features of the Atmel 80C52 with extended Flash capacity (32-Kbyte), 256 bytes of internal RAM, a 4-level interrupt system, two 16-bit timer/counters (T0/T1), a full duplex enhanced UART (EUART) and an on-chip oscillator.

In addition, AT89C5131A-L has an on-chip expanded RAM of 1024 bytes (ERAM), a dual- data pointer, a 16-bit up/down Timer (T2), a Programmable Counter Array (PCA), up to 4 programmable LED current sources, a programmable hardware watchdog and a power-on reset.

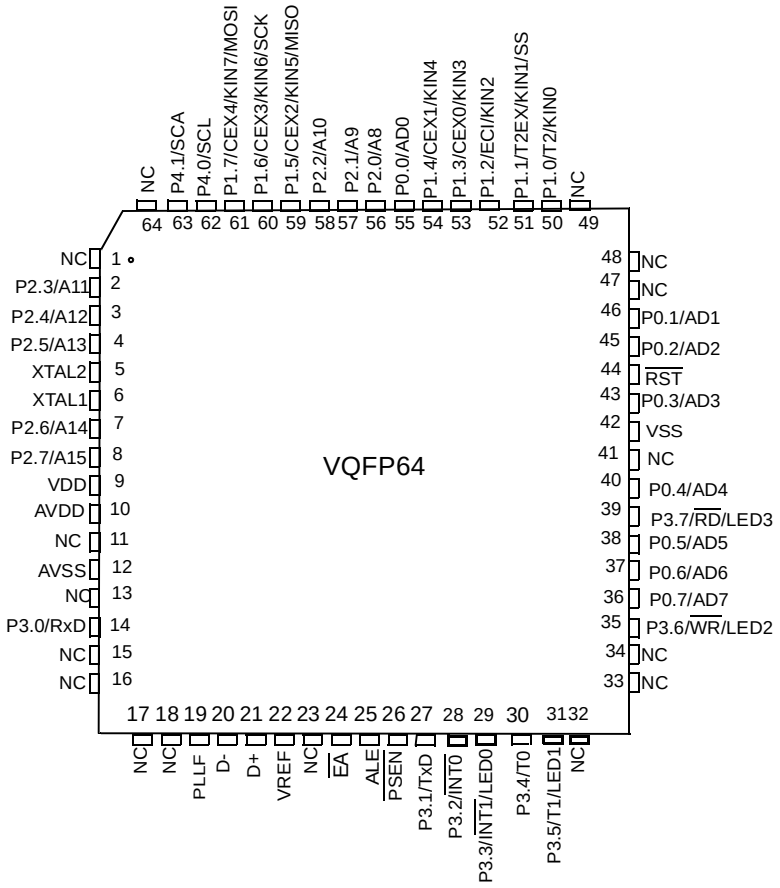
AT89C5131A-L has two software-selectable modes of reduced activity for further reduction in power consumption. In the idle mode the CPU is frozen while the timers, the serial ports and the interrupt system are still operating. In the power-down mode the RAM is saved, the peripheral clock is frozen, but the device has full wake-up capability through USB events or external interrupts.

Block Diagram



Notes: 1. Alternate function of Port 1
2. Alternate function of Port 3
3. Alternate function of Port 4

Figure 2. AT89C5131A-L 64-pin VQFP Pinout



Signals

All the AT89C5131A-L signals are detailed by functionality on Table 1 through Table 12.

Table 1. Keypad Interface Signal Description

Signal Name	Type	Description	Alternate Function
KIN[7:0]	I	**Keypad Input Lines** Holding one of these pins high or low for 24 oscillator periods triggers a keypad interrupt if enabled. Held line is reported in the KBCON register.	P1[7:0]

Table 2. Programmable Counter Array Signal Description

Signal Name	Type	Description	Alternate Function
ECI	I	**External Clock Input**	P1.2
CEX[4:0]	I/O	Capture External Input Compare External Output	P1.3 P1.4 P1.5 P1.6 P1.7

Table 3. Serial I/O Signal Description

Signal Name	Type	Description	Alternate Function
RxD	I	**Serial Input** The serial input is P3.0 after reset, but it can also be configured to P4.0 by software.	P3.0
TxD	O	**Serial Output** The serial output is P3.1 after reset, but it can also be configured to P4.1 by software.	P3.1

Table 4. Timer 0, Timer 1 and Timer 2 Signal Description

Signal Name	Type	Description	Alternate Function
INT0	I	**Timer 0 Gate Input** $\overline{INT0}$ serves as external run control for timer 0, when selected by GATE0 bit in TCON register. **External Interrupt 0** $\overline{INT0}$ input set IE0 in the TCON register. If bit IT0 in this register is set, bits IE0 are set by a falling edge on $\overline{INT0}$. If bit IT0 is cleared, bits IE0 is set by a low level on $\overline{INT0}$.	P3.2
INT1	I	**Timer 1 Gate Input** $\overline{INT1}$ serves as external run control for Timer 1, when selected by GATE1 bit in TCON register. **External Interrupt 1** $\overline{INT1}$ input set IE1 in the TCON register. If bit IT1 in this register is set, bits IE1 are set by a falling edge on $\overline{INT1}$. If bit IT1 is cleared, bits IE1 is set by a low level on $\overline{INT1}$.	P3.3

Table 4. Timer 0, Timer 1 and Timer 2 Signal Description (Continued)

Signal Name	Type	Description	Alternate Function
T0	I	**Timer Counter 0 External Clock Input** When Timer 0 operates as a counter, a falling edge on the T0 pin increments the count.	P3.4
T1	I	**Timer/Counter 1 External Clock Input** When Timer 1 operates as a counter, a falling edge on the T1 pin increments the count.	P3.5
T2	I O	**Timer/Counter 2 External Clock Input** Timer/Counter 2 Clock Output	P1.0
T2EX	I	Timer/Counter 2 Reload/Capture/Direction Control Input	P1.1

Table 5. LED Signal Description

Signal Name	Type	Description	Alternate Function
LED[3:0]	O	**Direct Drive LED Output** These pins can be directly connected to the Cathode of standard LEDs without external current limiting resistors. The typical current of each output can be programmed by software to 2, 6 or 10 mA. Several outputs can be connected together to get higher drive capabilities.	P3.3 P3.5 P3.6 P3.7

Table 6. TWI Signal Description

Signal Name	Type	Description	Alternate Function
SCL	I/O	**SCL: TWI Serial Clock** SCL output the serial clock to slave peripherals. SCL input the serial clock from master.	P4.0
SDA	I/O	**SDA: TWI Serial Data** SCL is the bidirectional TWI data line.	P4.1

Table 7. SPI Signal Description

Signal Name	Type	Description	Alternate Function
SS	I/O	**$\overline{\text{SS}}$:** SPI Slave Select	P1.1
MISO	I/O	**MISO:** SPI Master Input Slave Output line When SPI is in master mode, MISO receives data from the slave peripheral. When SPI is in slave mode, MISO outputs data to the master controller.	P1.5
SCK	I/O	**SCK:** SPI Serial Clock SCK outputs clock to the slave peripheral or receive clock from the master	P1.6
MOSI	I/O	**MOSI:** SPI Master Output Slave Input line When SPI is in master mode, MOSI outputs data to the slave peripheral. When SPI is in slave mode, MOSI receives data from the master controller	P1.7

Table 8. Ports Signal Description

Signal Name	Type	Description	Alternate Function
P0[7:0]	I/O	**Port 0** P0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. To avoid any parasitic current consumption, Floating P0 inputs must be pulled to V_{DD} or V_{SS}.	AD[7:0]
P1[7:0]	I/O	**Port 1** P1 is an 8-bit bidirectional I/O port with internal pull-ups, except for P1.6 and P1.7 that are true open drain outputs.	KIN[7:0] T2 T2EX ECI CEX[4:0]
P2[7:0]	I/O	**Port 2** P2 is an 8-bit bidirectional I/O port with internal pull-ups.	A[15:8]
P3[7:0]	I/O	**Port 3** P3 is an 8-bit bidirectional I/O port with internal pull-ups.	LED[3:0] RxD TxD $\overline{INT0}$ $\overline{INT1}$ T0 T1 $\overline{WR}$ $\overline{RD}$
P4[1:0]	I/O	**Port 4** P4 is an 2-bit open port.	SCL SDA

Table 9. Clock Signal Description

Signal Name	Type	Description	Alternate Function
XTAL1	I	**Input to the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin.	-
XTAL2	O	**Output of the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave XTAL2 unconnected.	-
PLLF	I	**PLL Low Pass Filter input** Receives the RC network of the PLL low pass filter (See Figure 5 on page 13).	-

Table 10. USB Signal Description

Signal Name	Type	Description	Alternate Function
D+	I/O	USB Data + signal	-
D-	I/O	USB Data - signal	-
VREF	O	**USB Reference Voltage** Connect this pin to D+ using a 1.5 kΩ resistor to use the Detach function.	-

Table 11. System Signal Description

Signal Name	Type	Description	Alternate Function
AD[7:0]	I/O	Multiplexed Address/Data LSB for external access Data LSB for Slave port access (used for 8-bit and 16-bit modes)	P0[7:0]
A[15:8]	I/O	Address Bus MSB for external access Data MSB for Slave port access (used for 16-bit mode only)	P2[7:0]
RD	I/O	**Read Signal** Read signal asserted during external data memory read operation. Control input for slave port read access cycles.	P3.7
WR	I/O	**Write Signal** Write signal asserted during external data memory write operation. Control input for slave write access cycles.	P3.6
$\overline{RST}$	I/O	**Reset** Holding this pin low for 64 oscillator periods while the oscillator is running resets the device. The Port pins are driven to their reset conditions when a voltage lower than V_{IL} is applied, whether or not the oscillator is running. This pin has an internal pull-up resistor which allows the device to be reset by connecting a capacitor between this pin and VSS. Asserting $\overline{RST}$ when the chip is in Idle mode or Power-down mode returns the chip to normal operation. This pin is set to 0 for at least 12 oscillator periods when an internal reset occurs (hardware watchdog or Power monitor).	-
ALE	O	**Address Latch Enable Output** The falling edge of ALE strobes the address into external latch. This signal is active only when reading or writing external memory using MOVX instructions.	-
PSEN	O	**Program** Test mode entry signal. This pin must be set to V_{DD} for normal operation.	-
EA	I	**External Access Enable** This pin must be held low to force the device to fetch code from external program memory starting at address 0000h. It is latched during reset and cannot be dynamically changed during operation.	-

Table 12. Power Signal Description

Signal Name	Type	Description	Alternate Function
AVSS	GND	**Alternate Ground** AVSS is used to supply the on-chip PLL and the USB PAD.	-
AVDD	PWR	**Alternate Supply Voltage** AVDD is used to supply the on-chip PLL and the USB PAD.	-
VSS	GND	**Digital Ground** VSS is used to supply the buffer ring and the digital core.	-
VDD	PWR	**Digital Supply Voltage** VDD is used to supply the buffer ring on all versions of the device. It is also used to power the on-chip voltage regulator of the Standard versions or the digital core of the Low Power versions.	-

Typical Application

The following figure represents the typical wiring schematic.

Figure 5. Typical Application

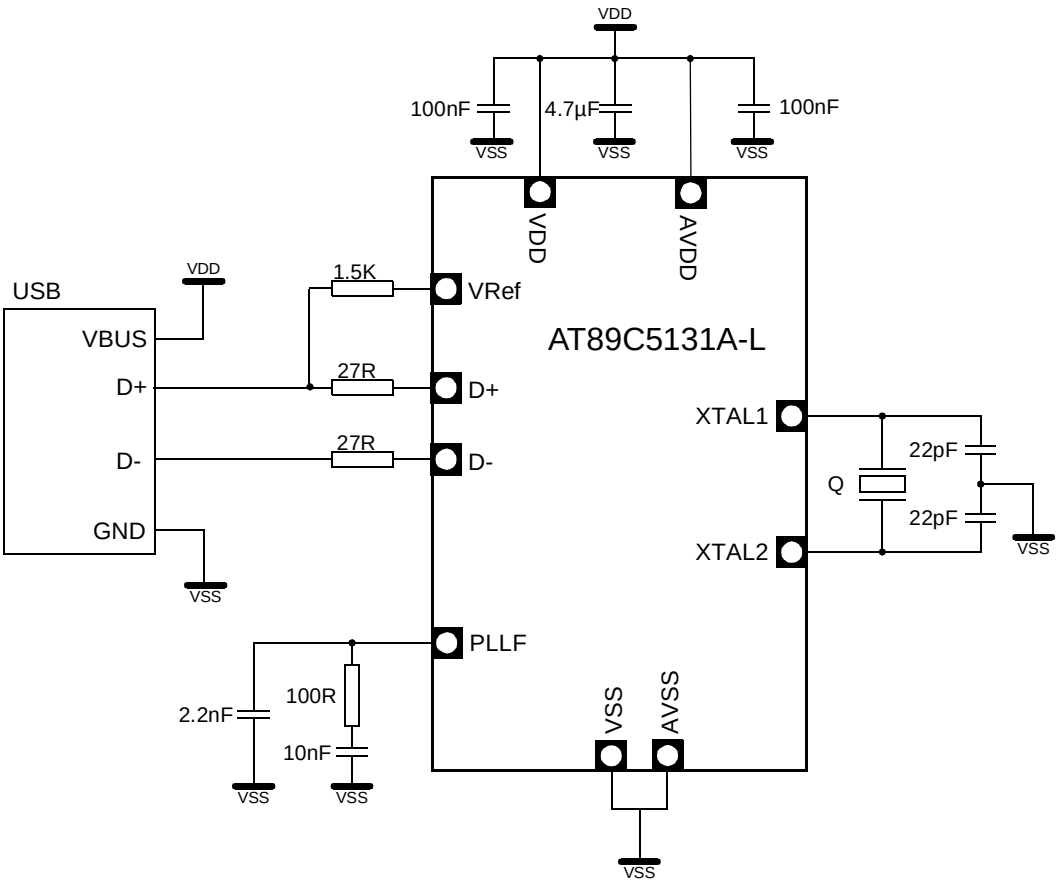
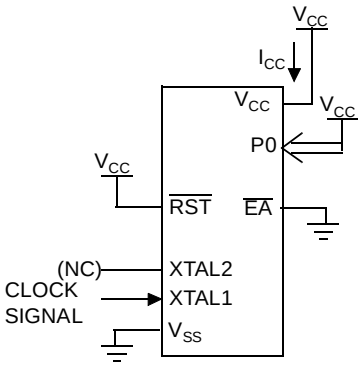
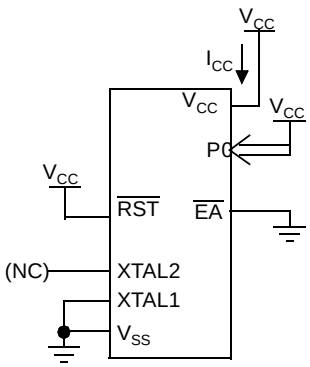


Figure 7. I_{CC} Test Condition, Idle Mode



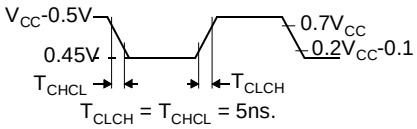
All other pins are disconnected.

Figure 8. I_{CC} Test Condition, Power-down Mode



All other pins are disconnected.

Figure 9. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes



LED's

Table 13. LED Outputs DC Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{OL}	Output Low Current, P3.6 and P3.7 LED modes	1	2	4	mA	2 mA configuration
		2	4	8	mA	4 mA configuration
		5	10	20	mA	10 mA configuration

Note: 1. (T_A = -20°C to +50°C, V_{CC} - V_{OL} = 2 V ± 20%)

AC Parameters

Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a “T” (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example: T_{AVLL} = Time for Address Valid to ALE Low.
T_{LLPL} = Time for ALE Low to $\overline{PSEN}$ Low.

T_A = -40°C to +85°C; V_{SS} = 0V; V_{CC} = 3.3V ±10%; F = 0 to 40 MHz.

T_A = -40°C to +85°C; V_{SS} = 0V; V_{CC} = 3.3V ± 10%.

(Load Capacitance for port 0, ALE and PSEN = 60 pF; Load Capacitance for all other outputs = 60 pF.)

Table 14, Table 17 and Table 20 give the description of each AC symbols.

Table 15, Table 19 and Table 21 give for each range the AC parameter.

Table 16, Table 19 and Table 22 give the frequency derating formula of the AC parameter for each speed range description. To calculate each AC symbols. take the x value and use this value in the formula.

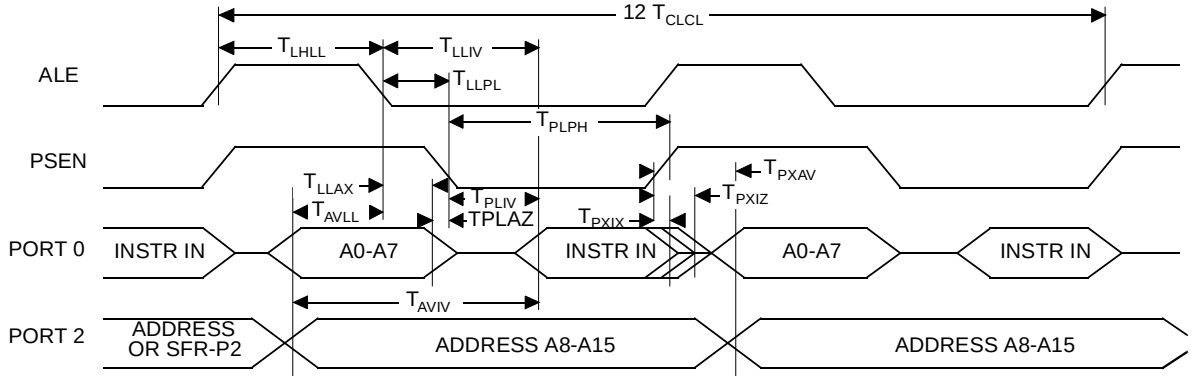
Example: T_{LLIV} and 20 MHz, Standard clock.
x = 30 ns
T = 50 ns
T_{CCIV} = 4T - x = 170 ns

External Program Memory Characteristics

Table 14. Symbol Description

Symbol	Parameter
T	Oscillator Clock Period
T_{LHLL}	ALE Pulse Width
T_{AVLL}	Address Valid to ALE
T_{LLAX}	Address Hold after ALE
T_{LLIV}	ALE to Valid Instruction In
T_{LLPL}	ALE to $\overline{PSEN}$
T_{PLPH}	$\overline{PSEN}$ Pulse Width
T_{PLIV}	$\overline{PSEN}$ to Valid Instruction In
T_{PXIX}	Input Instruction Hold after $\overline{PSEN}$
T_{PXIZ}	Input Instruction Float after $\overline{PSEN}$
T_{AVIV}	Address to Valid Instruction In
T_{PLAZ}	$\overline{PSEN}$ Low to Address Float

External Program Memory Read Cycle



External Data Memory Characteristics

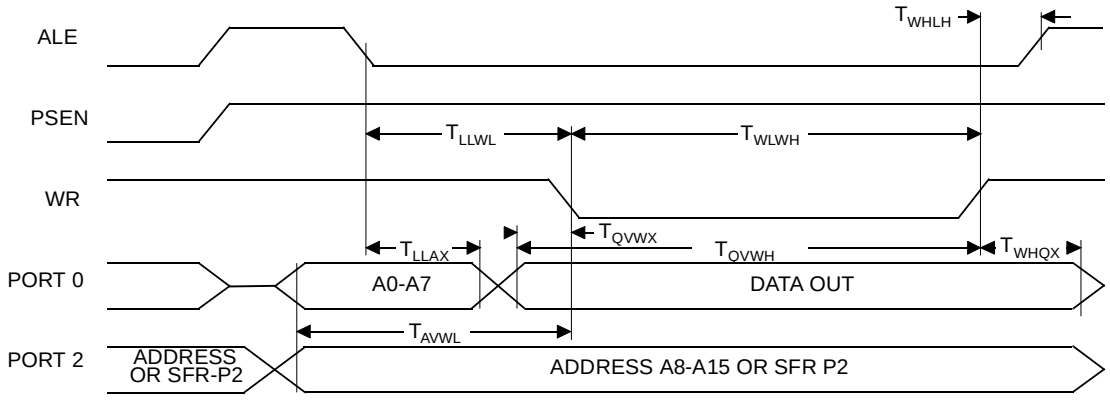
Table 17. Symbol Description

Symbol	Parameter
T_{RLRH}	$\overline{RD}$ Pulse Width
T_{WLWH}	$\overline{WR}$ Pulse Width
T_{RLDV}	$\overline{RD}$ to Valid Data In
T_{RHDX}	Data Hold After $\overline{RD}$
T_{RHDZ}	Data Float After $\overline{RD}$
T_{LLDV}	ALE to Valid Data In
T_{AVDV}	Address to Valid Data In
T_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$
T_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$
T_{QVWX}	Data Valid to $\overline{WR}$ Transition
T_{QVWH}	Data set-up to $\overline{WR}$ High
T_{WHQX}	Data Hold After $\overline{WR}$
T_{RLAZ}	$\overline{RD}$ Low to Address Float
T_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE high

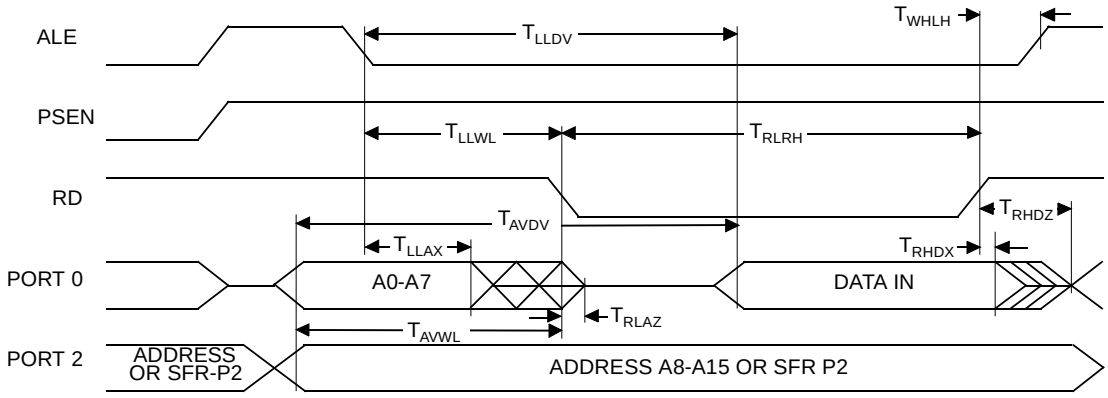
Table 19. AC Parameters for a Variable Clock

Symbol	Type	Standard Clock	X2 Clock	X Parameter	Units
T_{RLRH}	Min	6 T - x	3 T - x	20	ns
T_{WLWH}	Min	6 T - x	3 T - x	20	ns
T_{RLDV}	Max	5 T - x	2.5 T - x	25	ns
T_{RHDX}	Min	x	x	0	ns
T_{RHDZ}	Max	2 T - x	T - x	20	ns
T_{LLDV}	Max	8 T - x	4T -x	40	ns
T_{AVDV}	Max	9 T - x	4.5 T - x	60	ns
T_{LLWL}	Min	3 T - x	1.5 T - x	25	ns
T_{LLWL}	Max	3 T + x	1.5 T + x	25	ns
T_{AVWL}	Min	4 T - x	2 T - x	25	ns
T_{QVWX}	Min	T - x	0.5 T - x	15	ns
T_{QVWH}	Min	7 T - x	3.5 T - x	25	ns
T_{WHQX}	Min	T - x	0.5 T - x	10	ns
T_{RLAZ}	Max	x	x	0	ns
T_{WHLH}	Min	T - x	0.5 T - x	15	ns
T_{WHLH}	Max	T + x	0.5 T + x	15	ns

External Data Memory Write Cycle



External Data Memory Read Cycle



Serial Port Timing - Shift Register Mode

Table 20. Symbol Description (F = 40 MHz)

Symbol	Parameter
T_{XLXL}	Serial port clock cycle time
T_{QVHX}	Output data set-up to clock rising edge
T_{XHQX}	Output data hold after clock rising edge
T_{XHDX}	Input data hold after clock rising edge
T_{XHDV}	Clock rising edge to input data valid

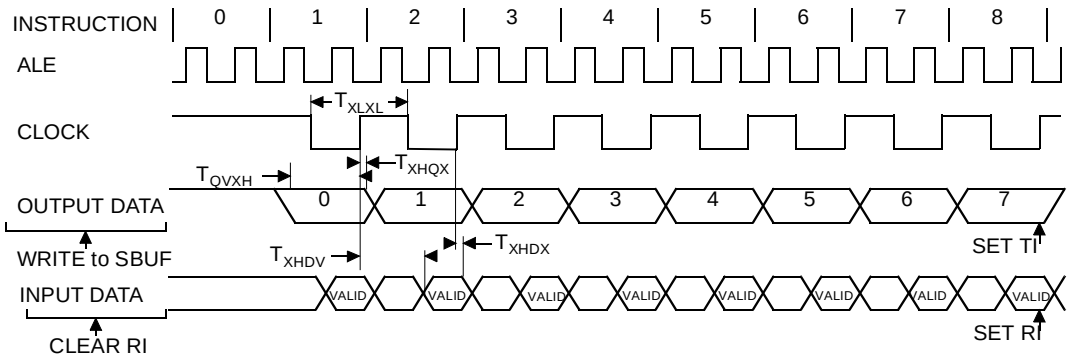
Table 21. AC Parameters for a Fix Clock (F = 40 MHz)

Symbol	Min	Max	Units
T_{XLXL}	300		ns
T_{QVHX}	200		ns
T_{XHQX}	30		ns
T_{XHDX}	0		ns
T_{XHDV}		117	ns

Table 22. AC Parameters for a Variable Clock

Symbol	Type	Standard Clock	X2 Clock	X Parameter for -M Range	Units
T_{XLXL}	Min	12 T	6 T		ns
T_{QVHX}	Min	10 T - x	5 T - x	50	ns
T_{XHQX}	Min	2 T - x	T - x	20	ns
T_{XHDX}	Min	x	x	0	ns
T_{XHDV}	Max	10 T - x	5 T- x	133	ns

Shift Register Timing Waveform

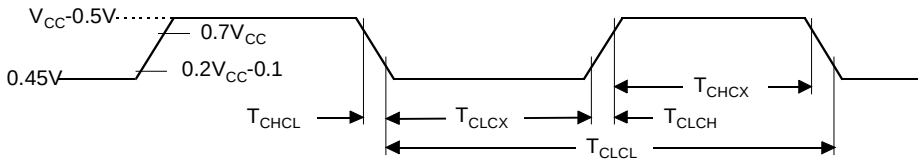


External Clock Drive Characteristics (XTAL1)

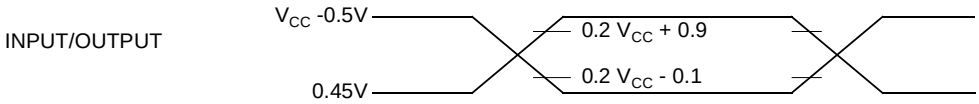
Table 23. AC Parameters

Symbol	Parameter	Min	Max	Units
T_{CLCL}	Oscillator Period	25		ns
T_{CHCX}	High Time	5		ns
T_{CLCX}	Low Time	5		ns
T_{CLCH}	Rise Time		5	ns
T_{CHCL}	Fall Time		5	ns
T_{CHCX}/T_{CLCX}	Cyclic ratio in X2 mode	40	60	%

External Clock Drive Waveforms

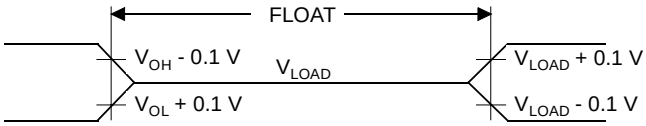


AC Testing Input/Output Waveforms

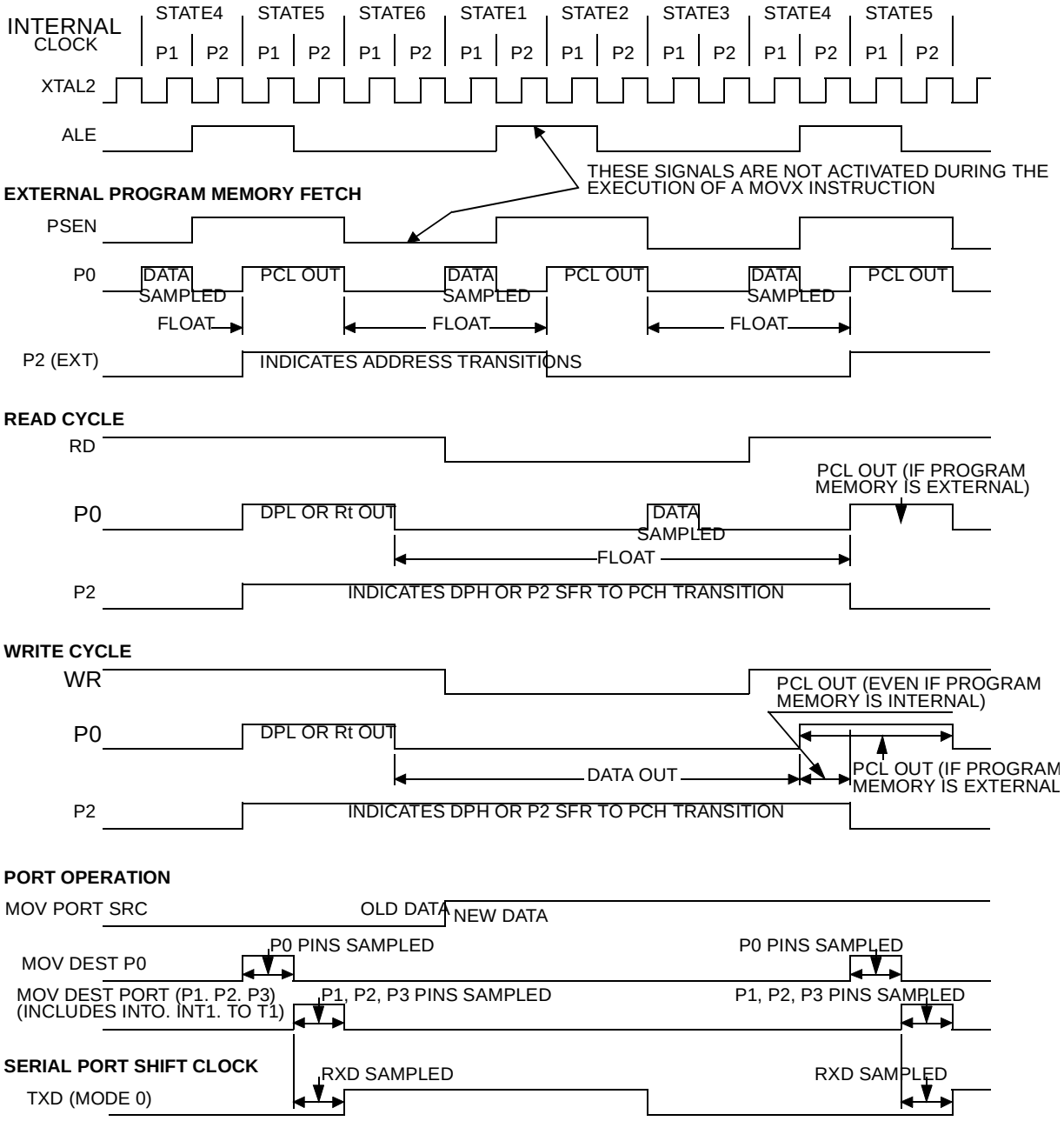


AC inputs during testing are driven at V_{CC} - 0.5 for a logic “1” and 0.45V for a logic “0”. Timing measurement are made at V_{IH} min for a logic “1” and V_{IL} max for a logic “0”.

Float Waveforms



Clock Waveforms Valid in normal clock mode. In X2 mode XTAL2 must be changed to XTAL2/2.



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though (T_A = 25°C fully loaded) $\overline{RD}$ and $\overline{WR}$ propagation delays are approximately 50 ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

Flash Memory

Table 24. Timing Symbol Definitions

Signals	
S (Hardware Condition)	$\overline{PSEN}$, EA
R	$\overline{RST}$
B	FBUSY Flag

Conditions	
L	Low
V	Valid
X	No Longer Valid

Table 25. Memory AC Timing
VDD = 3.3V ± 10%, T_A = -40 to +85°C

Symbol	Parameter	Min	Typ	Max	Unit
T_{SVRL}	Input $\overline{PSEN}$ Valid to $\overline{RST}$ Edge	50			ns
T_{RLSX}	Input $\overline{PSEN}$ Hold after $\overline{RST}$ Edge	50			ns
T_{BHBL}	Flash Internal Busy (Programming) Time		10		ms

Figure 10. Flash Memory - ISP Waveforms

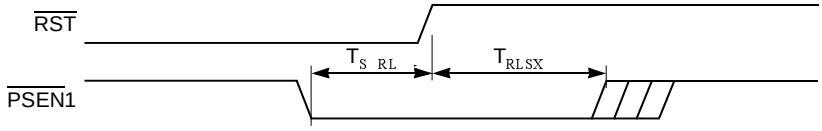
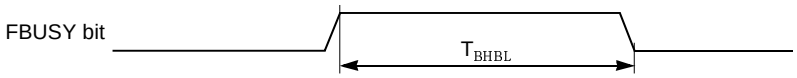


Figure 11. Flash Memory - Internal Busy Waveforms



USB AC Parameters

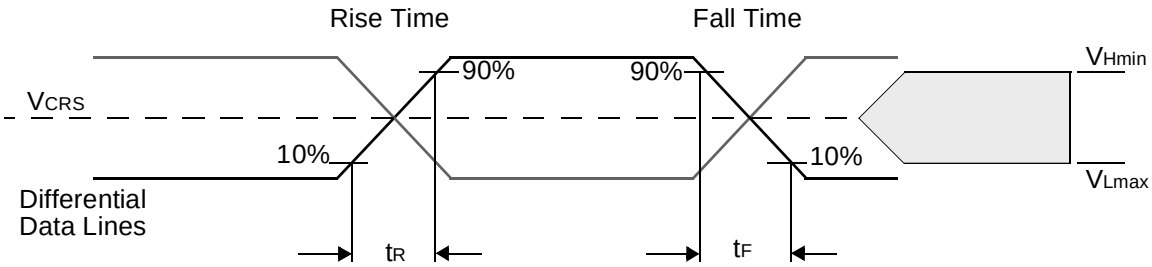
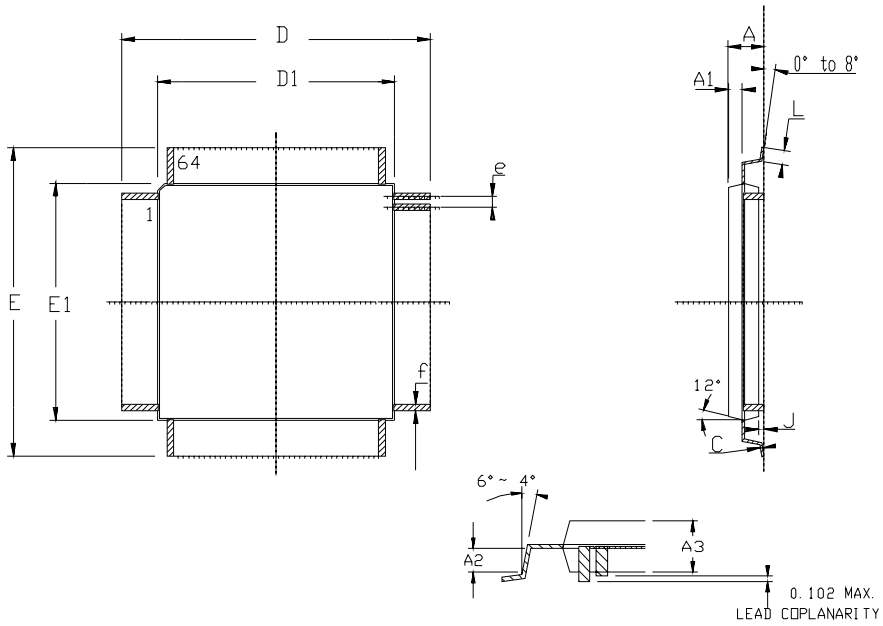


Table 26. USB AC Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
t_R	Rise Time	4		20	ns	
t_F	Fall Time	4		20	ns	
t_{FDRATE}	Full-speed Data Rate	11.9700		12.0300	Mb/s	
V_{CRS}	Crossover Voltage	1.3		2.0	V	
t_{DJ1}	Source Jitter Total to Next Transaction	-3.5		3.5	ns	
t_{DJ2}	Source Jitter Total for Paired Transactions	-4		4	ns	
t_{JR1}	Receiver Jitter to Next Transaction	-18.5		18.5	ns	
t_{JR2}	Receiver Jitter for Paired Transactions	-9		9	ns	

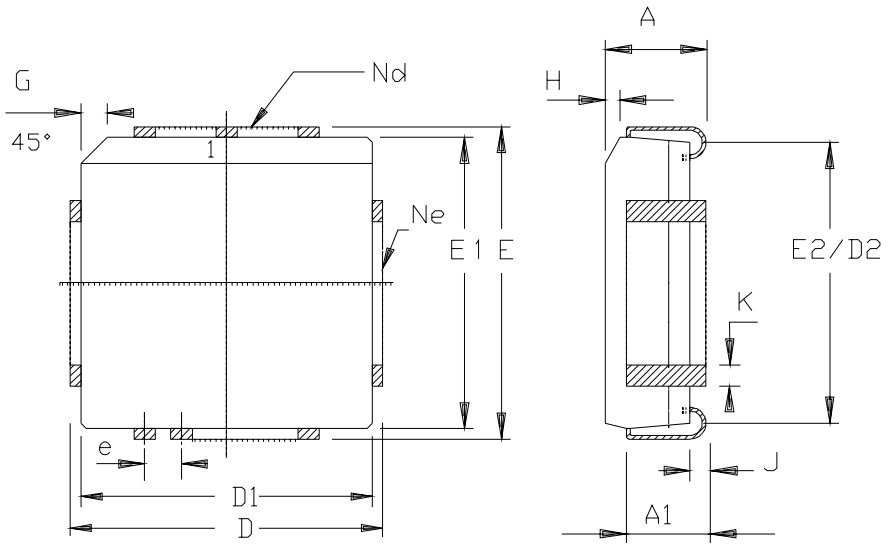
Packaging Information

64-lead VQFP



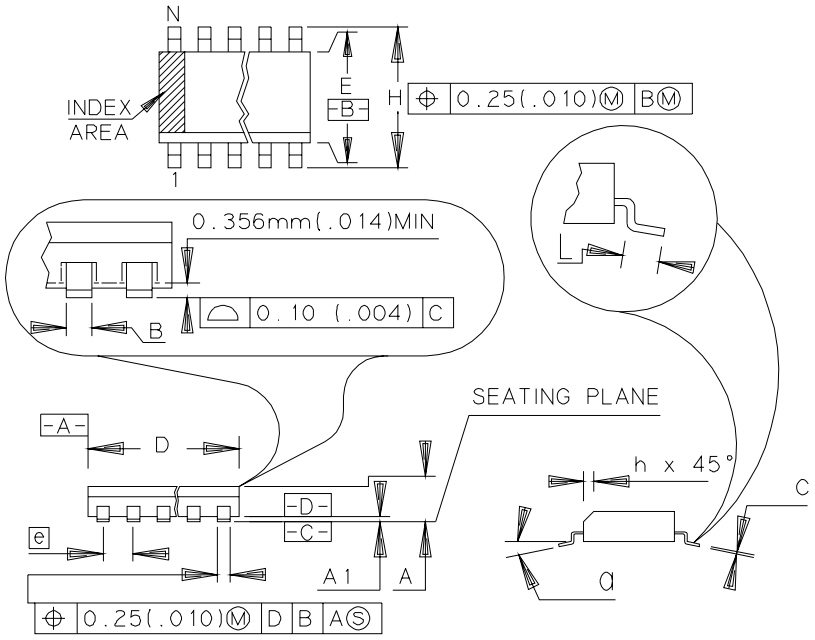
	MM		INCH	
	Min	Max	Min	Max
A	-	1.60	-	.063
A1	0.64 REF		.025 REF	
A2	0.64 REF		.025 REF	
A3	1.35	1.45	.053	.057
D	11.75	12.25	.463	.483
D1	9.90	10.10	.390	.398
E	11.75	12.25	.463	.483
E1	9.90	10.10	.390	.398
J	0.05	-	.002	-
L	0.45	0.75	.018	.030
e	0.50 BSC		.0197 BSC	
f	0.25 BSC		.010 BSC	

52-lead PLCC



	MM		INCH	
A	4.20	4.57	.165	.180
A1	2.29	3.30	.090	.130
D	19.94	20.19	.785	.795
D1	19.05	19.25	.750	.758
D2	17.53	18.54	.690	.730
E	19.94	20.19	.785	.795
E1	19.05	19.25	.750	.758
E2	17.53	18.54	.690	.730
e	1.27	BSC	.050	BSC
G	1.07	1.22	.042	.048
H	1.07	1.42	.042	.056
J	0.51	-	.020	-
K	0.33	0.53	.013	.021
Nd	13		13	
Ne	13		13	
PKG STD	00			

28-lead SO



	MM		INCH	
A	2.35	2.65	.093	.104
A1	0.10	0.30	.004	.012
B	0.35	0.49	.014	.019
C	0.23	0.32	.009	.013
D	17.70	18.10	.697	.713
E	7.40	7.60	.291	.299
e	1.27	BSC	.050	BSC
H	10.00	10.65	.394	.419
h	0.25	0.75	.010	.029
L	0.40	1.27	.016	.050
N	28		28	
a	0°		8°	