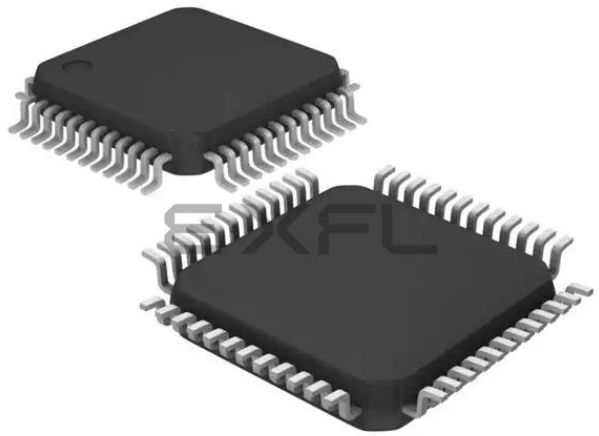

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SCI, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	5.5V ~ 18V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvl12f0mlf

— No external components required
— Reference divider and multiplier allow large variety of clock rates
— Automatic bandwidth control mode for low-jitter operation
— Automatic frequency lock detector
— Configurable option to spread spectrum for reduced EMC radiation (frequency modulation)
— Reference clock sources:
  – Internal 1 MHz RC oscillator (IRC)
  – External 4-16MHz crystal oscillator/resonator

1.4.3.2 Internal RC Oscillator (IRC)

- 1 MHz internal RC oscillator with +/-1.3% accuracy over rated temperature range

1.4.4 Main External Oscillator (XOSCLCP)

- Amplitude controlled Pierce oscillator using 4 MHz to 20 MHz crystal
  — Current gain control on amplitude output
  — Signal with low harmonic distortion
  — Low power
  — Good noise immunity
  — Eliminates need for external current limiting resistor
  — Transconductance sized for optimum start-up margin for typical crystals
  — Oscillator pins shared with GPIO functionality

1.4.5 Timer (TIM0 and TIM1)

- two independent timer modules with own 16-bit free-running counter and with 8-bit precision prescaler
  — 6 x 16-bit channels Timer module (TIM0) for input capture or output compare
  — 2 x 16-bit channels Timer module (TIM1) for input capture or output compare

1.4.6 Pulse Width Modulation Module (PWM0 and PMW1)

- Up to eight channel x 8-bit or up to four channel x 16-bit pulse width modulator
  — Programmable period and duty cycle per channel
  — Center-aligned or left-aligned outputs
  — Programmable clock select logic with a wide range of frequencies

1.4.7 Inter-IC Module (IIC)

- Multi-master operation
- Software programmable for one of 256 different serial clock frequencies

1.13 Module device level dependencies

1.13.1 COP Configuration

The COP time-out rate bits CR[2:0] and the WCOP bit in the CPMUCOP register are loaded from the Flash configuration field byte at global address 0xFF_FE0E during the reset sequence. See Table 1-13 and Table 1-14 for coding.

Table 1-13. Initial COP Rate Configuration

NV[2:0] in FOPT Register	CR[2:0] in COPCTL Register
000	111
001	110
010	101
011	100
100	011
101	010
110	001
111	000

Table 1-14. Initial WCOP Configuration

NV[3] in FOPT Register	WCOP in COPCTL Register
1	0
0	1

1.13.2 BDC Command Restriction

The BDC command READ_DBGTB returns 0x00 on this device because the DBG module does not feature a trace buffer.

Table 5-10. Field Location to Byte Access Mapping

Address[1:0]	Access Size	00	01	10	11	Note
00	32-bit	Data[31:24]	Data[23:16]	Data [15:8]	Data [7:0]	
01	32-bit	Data[31:24]	Data[23:16]	Data [15:8]	Data [7:0]	Realigned
10	32-bit	Data[31:24]	Data[23:16]	Data [15:8]	Data [7:0]	Realigned
11	32-bit	Data[31:24]	Data[23:16]	Data [15:8]	Data [7:0]	Realigned
00	16-bit	Data [15:8]	Data [7:0]			
01	16-bit		Data [15:8]	Data [7:0]		
10	16-bit			Data [15:8]	Data [7:0]	
11	16-bit			Data [15:8]	Data [7:0]	Realigned
00	8-bit	Data [7:0]				
01	8-bit		Data [7:0]			
10	8-bit			Data [7:0]		
11	8-bit				Data [7:0]	
			Denotes byte that is not transmitted			

5.4.5.2.1 FILL_MEM and DUMP_MEM Increments and Alignment

FILL_MEM and DUMP_MEM increment the previously accessed address by the previous access size to calculate the address of the current access. On misaligned longword accesses, the address bits [1:0] are forced to zero, therefore the following FILL_MEM or DUMP_MEM increment to the first address in the next 4-byte field. This is shown in Table 5-11, the address of the first DUMP_MEM.32 following READ_MEM.32 being calculated from 0x004000+4.

When misaligned word accesses are realigned, then the original address (not the realigned address) is incremented for the following FILL_MEM, DUMP_MEM command.

Misaligned word accesses can cause the same locations to be read twice as shown in rows 6 and 7. The hardware ensures alignment at an attempted misaligned word access across a 4-byte boundary, as shown in row 7. The following word access in row 8 continues from the realigned address of row 7.

Table 5-11. Consecutive Accesses With Variable Size

Row	Command	Address	Address[1:0]	00	01	10	11
1	READ_MEM.32	0x004003	11	Accessed	Accessed	Accessed	Accessed
2	DUMP_MEM.32	0x004004	00	Accessed	Accessed	Accessed	Accessed
3	DUMP_MEM.16	0x004008	00	Accessed	Accessed		
4	DUMP_MEM.16	0x00400A	10			Accessed	Accessed
5	DUMP_MEM.08	0x00400C	00	Accessed			
6	DUMP_MEM.16	0x00400D	01		Accessed	Accessed	
7	DUMP_MEM.16	0x00400E	10			Accessed	Accessed
8	DUMP_MEM.16	0x004010	01	Accessed	Accessed		

If PLL has locked (LOCK=1) $f_{VCO} = 2 \times f_{REF} \times (SYNDIV + 1)$

NOTE

f_{VCO} must be within the specified VCO frequency lock range. Bus frequency f_{bus} must not exceed the specified maximum.

The VCOFRQ[1:0] bits are used to configure the VCO gain for optimal stability and lock time. For correct PLL operation the VCOFRQ[1:0] bits have to be selected according to the actual target VCOCLK frequency as shown in Table 9-3. Setting the VCOFRQ[1:0] bits incorrectly can result in a non functional PLL (no locking and/or insufficient stability).

Table 9-3. VCO Clock Frequency Selection

VCOCLK Frequency Ranges	VCOFRQ[1:0]
32MHz <= f_{VCO} <= 48MHz	00
48MHz < f_{VCO} <= 64MHz	01
Reserved	10
Reserved	11

9.3.2.5 S12CPMU_UHV Reference Divider Register (CPMUREFDIV)

The CPMUREFDIV register provides a finer granularity for the PLL multiplier steps when using the external oscillator as reference.

Module Base + 0x0005

	7	6	5	4	3	2	1	0
R	REFFRQ[1:0]		0	0	REFDIV[3:0]			
W								
Reset	0	0	0	0	1	1	1	1

Figure 9-8. S12CPMU_UHV Reference Divider Register (CPMUREFDIV)

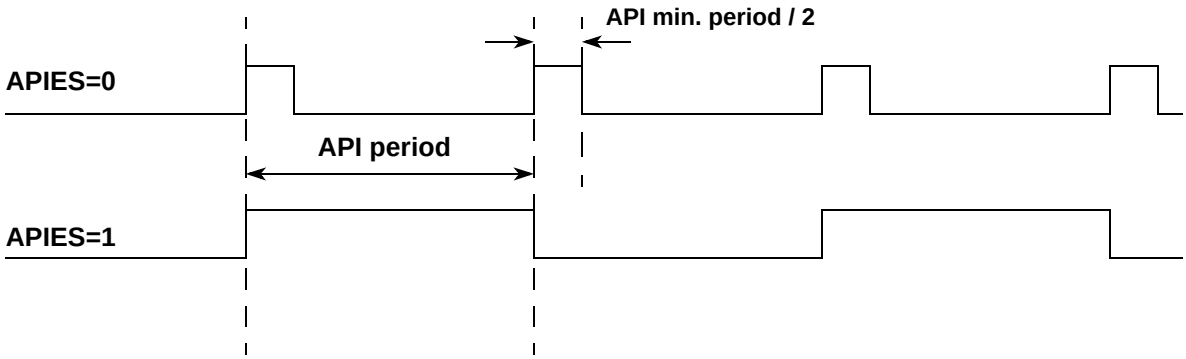
Read: Anytime

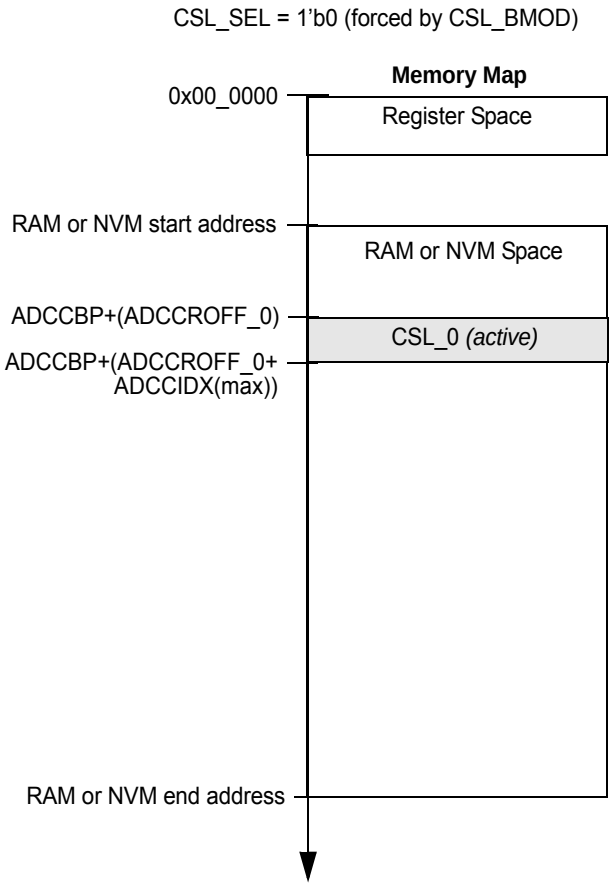
Write: If PROT=0 (CPMUPROT register) and PLLSEL=1 (CPMUCLKS register), then write anytime. Else write has no effect.

NOTE

Write to this register clears the LOCK and UPOSC status bits.

Figure 9-23. Waveform selected on API_EXTCLK pin (APIEA=1, APIFE=1)





Note: Address register names in () are not absolute addresses instead they are a sample offset or sample index

Figure 10-32. Command Sequence List Schema in Single Buffer Mode

While the ADC is enabled, one CSL is active (indicated by bit CSL_SEL) and the corresponding list should not be modified anymore. At the same time the alternative CSL can be modified to prepare the ADC for new conversion sequences in CSL double buffered mode. When the ADC is enabled, the command address registers (ADCCBP, ADCCROFF_0/2, ADCCIDX) are read only and register ADCCIDX is under control of the ADC.

11.4.2.1 Control Register (DACCTL)

Module Base + 0x0000 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	FVR	DRIVE	0	0	0	DACM[2:0]		
W								
Reset	1	0	0	0	0	0	0	0

= Unimplemented

Figure 11-3. Control Register (DACCTL)

[1] Read: Anytime
Write: Anytime

Table 11-3. DACCTL Field Description

Field	Description
7 FVR	**Full Voltage Range** — This bit defines the voltage range of the DAC. 0 DAC resistor network operates with the reduced voltage range 1 DAC resistor network operates with the full voltage range **Note:** For more details see Section 11.5.8, “Analog output voltage calculation”.
6 DRIVE	**Drive Select** — This bit selects the output drive capability of the operational amplifier, see electrical Spec. for more details. 0 Low output drive for high resistive loads 1 High output drive for low resistive loads
2:0 DACM[2:0]	**Mode Select** — These bits define the mode of the DAC. A write access with an unsupported mode will be ignored. 000 Off 001 Operational Amplifier 010 Internal DAC only 100 Unbuffered DAC 101 Unbuffered DAC with Operational Amplifier 111 Buffered DAC other Reserved

13.3.2.10 MSCAN Transmitter Message Abort Acknowledge Register (CANTAAK)

The CANTAAK register indicates the successful abort of a queued message, if requested by the appropriate bits in the CANTARQ register.

Module Base + 0x0009 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 13-13. MSCAN Transmitter Message Abort Acknowledge Register (CANTAAK)

1 Read: Anytime
Write: Unimplemented

NOTE

The CANTAAK register is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK = 1).

Table 13-16. CANTAAK Register Field Descriptions

Field	Description
2-0 ABTAK[2:0]	**Abort Acknowledge** — This flag acknowledges that a message was aborted due to a pending abort request from the CPU. After a particular message buffer is flagged empty, this flag can be used by the application software to identify whether the message was aborted successfully or was sent anyway. The ABTAKx flag is cleared whenever the corresponding TXE flag is cleared. 0 The message was not aborted. 1 The message was aborted.

13.3.2.11 MSCAN Transmit Buffer Selection Register (CANTBSEL)

The CANTBSEL register allows the selection of the actual transmit message buffer, which then will be accessible in the CANTXFG register space.

Module Base + 0x000A Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	TX2	TX1	TX0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 13-14. MSCAN Transmit Buffer Selection Register (CANTBSEL)

1 Read: Find the lowest ordered bit set to 1, all other bits will be read as 0
Write: Anytime when not in initialization mode

Module Base + 0x00X2

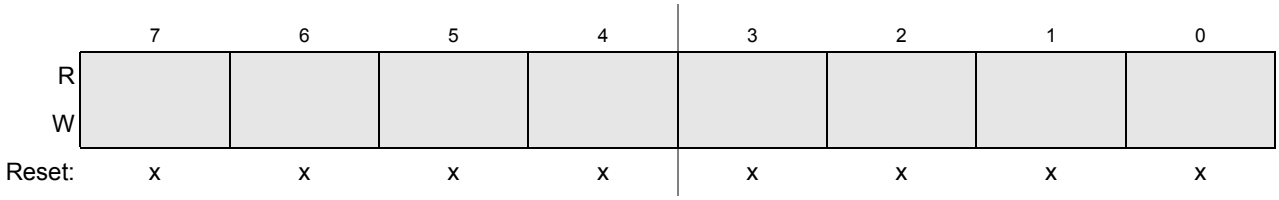


Figure 13-31. Identifier Register 2 — Standard Mapping

Module Base + 0x00X3

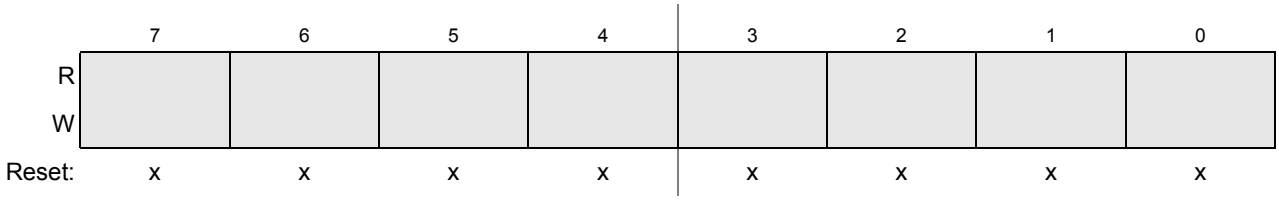


Figure 13-32. Identifier Register 3 — Standard Mapping

13.3.3.2 Data Segment Registers (DSR0-7)

The eight data segment registers, each with bits DB[7:0], contain the data to be transmitted or received. The number of bytes to be transmitted or received is determined by the data length code in the corresponding DLR register.

Module Base + 0x00X4 to Module Base + 0x00XB

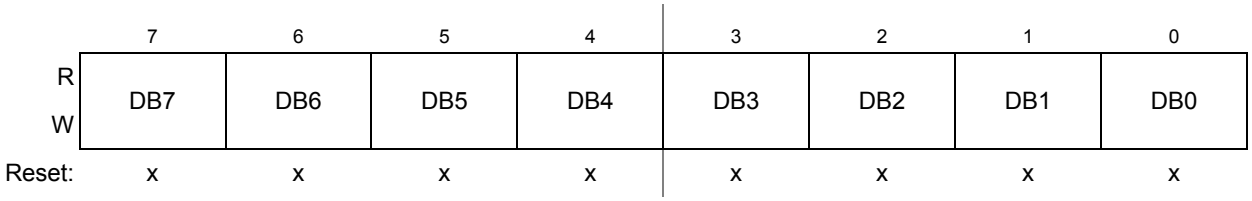


Figure 13-33. Data Segment Registers (DSR0–DSR7) — Extended Identifier Mapping

Table 13-32. DSR0–DSR7 Register Field Descriptions

Field	Description
7-0 DB[7:0]	**Data bits 7-0**

The Prescaler can be calculated as follows depending on logical value of the PTPS[7:0] and PRNT bit:

PRNT = 1 : Prescaler = PTPS[7:0] + 1

Table 15-17. Precision Timer Prescaler Selection Examples when PRNT = 1

PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0	Prescale Factor
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
0	0	0	0	0	0	1	1	4
-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-
0	0	0	1	0	0	1	1	20
0	0	0	1	0	1	0	0	21
0	0	0	1	0	1	0	1	22
-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-
1	1	1	1	1	1	0	0	253
1	1	1	1	1	1	0	1	254
1	1	1	1	1	1	1	0	255
1	1	1	1	1	1	1	1	256

15.4 Functional Description

This section provides a complete functional description of the timer TIM16B6CV3 block. Please refer to the detailed timer block diagram in Figure 15-22 as necessary.

16.3.2.11 Main Timer Interrupt Flag 2 (TFLG2)

Module Base + 0x000F

	7	6	5	4	3	2	1	0
R	TOF	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Unimplemented or Reserved

Figure 16-17. Main Timer Interrupt Flag 2 (TFLG2)

TFLG2 indicates when interrupt conditions have occurred. To clear a bit in the flag register, write the bit to one while TEN bit of TSCR1 .

Read: Anytime

Write: Used in clearing mechanism (set bits cause corresponding bits to be cleared).

Any access to TCNT will clear TFLG2 register if the TFFCA bit in TSCR register is set.

Table 16-14. TRLG2 Field Descriptions

Field	Description
7 TOF	**Timer Overflow Flag** — Set when 16-bit free-running timer overflows from 0xFFFF to 0x0000. Clearing this bit requires writing a one to bit 7 of TFLG2 register while the TEN bit of TSCR1 is set to one .

17.4.2.6 Center Aligned Outputs

For center aligned output mode selection, set the CAEx bit (CAEx = 1) in the PWMCAE register and the corresponding PWM output will be center aligned.

The 8-bit counter operates as an up/down counter in this mode and is set to up whenever the counter is equal to $00. The counter compares to two registers, a duty register and a period register as shown in the block diagram in Figure 17-16. When the PWM counter matches the duty register, the output flip-flop changes state, causing the PWM waveform to also change state. A match between the PWM counter and the period register changes the counter direction from an up-count to a down-count. When the PWM counter decrements and matches the duty register again, the output flip-flop changes state causing the PWM output to also change state. When the PWM counter decrements and reaches zero, the counter direction changes from a down-count back to an up-count and a load from the double buffer period and duty registers to the associated registers is performed, as described in Section 17.4.2.3, “PWM Period and Duty”. The counter counts from 0 up to the value in the period register and then back down to 0. Thus the effective period is PWMPERx*2.

NOTE

Changing the PWM output mode from left aligned to center aligned output (or vice versa) while channels are operating can cause irregularities in the PWM output. It is recommended to program the output mode before enabling the PWM channel.

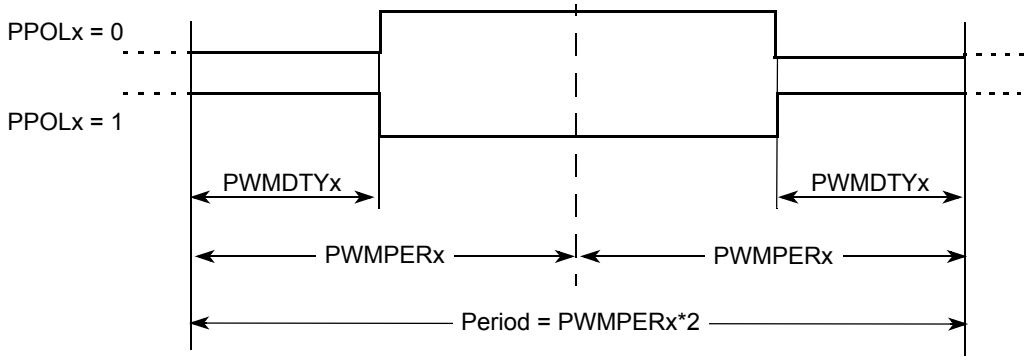


Figure 17-19. PWM Center Aligned Output Waveform

To calculate the output frequency in center aligned output mode for a particular channel, take the selected clock source frequency for the channel (A, B, SA, or SB) and divide it by twice the value in the period register for that channel.

- PWMx Frequency = Clock (A, B, SA, or SB) / (2*PWMPERx)
- PWMx Duty Cycle (high time as a% of period):
  - Polarity = 0 (PPOLx = 0)
    Duty Cycle = [(PWMPERx-PWMDTYx)/PWMPERx] * 100%
  - Polarity = 1 (PPOLx = 1)
    Duty Cycle = [PWMDTYx / PWMPERx] * 100%

As an example of a center aligned output, consider the following case:

Chapter 18
Serial Communication Interface (S12SCIV6)

Table 18-1. Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
06.06	03/11/2013			fix typo of BDL reset value,Figure 18-4 fix typo of Table 18-2,Table 18-16,reword 18.4.4/18-523
06.07	09/03/2013			update Figure 18-14./18-520 Figure 18-16./18-524 Figure 18-20./18-529 update 18.4.4/18-523,more detail for two baud add note for Table 18-16./18-523 update Figure 18-2./18-508,Figure 18-12./18-518
06.08	10/14/2013			update Figure 18-4./18-509 18.3.2.9/18-518

18.1 Introduction

This block guide provides an overview of the serial communication interface (SCI) module.

The SCI allows asynchronous serial communications with peripheral devices and other CPUs.

18.1.1 Glossary

IR: InfraRed

IrDA: Infrared Design Associate

IRQ: Interrupt Request

LIN: Local Interconnect Network

LSB: Least Significant Bit

MSB: Most Significant Bit

NRZ: Non-Return-to-Zero

RZI: Return-to-Zero-Inverted

RXD: Receive Pin

SCI : Serial Communication Interface

TXD: Transmit Pin

20.4.1.11 General Call Address

To broadcast using a general call, a device must first generate the general call address($00), then after receiving acknowledge, it must transmit data.

In communication, as a slave device, provided the GCEN is asserted, a device acknowledges the broadcast and receives data until the GCEN is disabled or the master device releases the bus or generates a new transfer. In the broadcast, slaves always act as receivers. In general call, IAAS is also used to indicate the address match.

In order to distinguish whether the address match is the normal address match or the general call address match, IBDR should be read after the address byte has been received. If the data is $00, the match is general call address match. The meaning of the general call address is always specified in the first data byte and must be dealt with by S/W, the IIC hardware does not decode and process the first data byte.

When one byte transfer is done, the received data can be read from IBDR. The user can control the procedure by enabling or disabling GCEN.

20.4.2 Operation in Run Mode

This is the basic mode of operation.

20.4.3 Operation in Wait Mode

IIC operation in wait mode can be configured. Depending on the state of internal bits, the IIC can operate normally when the CPU is in wait mode or the IIC clock generation can be turned off and the IIC module enters a power conservation state during wait mode. In the later case, any transmission or reception in progress stops at wait mode entry.

20.4.4 Operation in Stop Mode

The IIC is inactive in stop mode for reduced power consumption. The STOP instruction does not affect IIC register states.

20.5 Resets

The reset state of each individual bit is listed in Section 20.3, “Memory Map and Register Definition,” which details the registers and their bit-fields.

20.6 Interrupts

IICV3 uses only one interrupt vector.

Table 20-11. Interrupt Summary

Interrupt	Offset	Vector	Priority	Source	Description

Table 22-31. Allowed P-Flash and EEPROM Simultaneous Operations on a single hardblock

	EEPROM				
Program Flash	**Read**	**Margin Read[2]**	**Program**	**Sector Erase**	**Mass Erase[2]**
Read	OK[1]	OK	OK	OK	
Margin Read[2]					
Program					
Sector Erase					
Mass Erase[3]					OK

1 Strictly speaking, only one read of either the P-Flash or EEPROM can occur at any given instant, but the memory controller will transparently arbitrate P-Flash and EEPROM accesses giving uninterrupted read access whenever possible.

2 A 'Margin Read' is any read after executing the margin setting commands 'Set User Margin Level' or 'Set Field Margin Level' with anything but the 'normal' level specified. See the Note on margin settings in Section 22.4.7.12 and Section 22.4.7.13.

3 The 'Mass Erase' operations are commands 'Erase All Blocks' and 'Erase Flash Block'

22.4.7 Flash Command Description

This section provides details of all available Flash commands launched by a command write sequence. The ACCERR bit in the FSTAT register will be set during the command write sequence if any of the following illegal steps are performed, causing the command not to be processed by the Memory Controller:

- Starting any command write sequence that programs or erases Flash memory before initializing the FCLKDIV register
- Writing an invalid command as part of the command write sequence
- For additional possible errors, refer to the error handling table provided for each command

If a Flash block is read during execution of an algorithm (CCIF = 0) on that same block, the read operation may return invalid data resulting in an illegal access (as described on Section 22.4.6).

If the ACCERR or FPVIOL bits are set in the FSTAT register, the user must clear these bits before starting any command write sequence (see Section 22.3.2.7).

CAUTION

A Flash word or phrase must be in the erased state before being programmed. Cumulative programming of bits within a Flash word or phrase is not allowed.

22.4.7.1 Erase Verify All Blocks Command

The Erase Verify All Blocks command will verify that all P-Flash and EEPROM blocks have been erased.

Table A-8. Thermal Package Characteristics for ZVL(S)32/16/8[1]

Num	Rating	Symbol	Min	Typ	Max	Unit
48LQFP						
1	Thermal resistance 48LQFP, single sided PCB[1] Natural Convection	θ_{JA}	—	80	—	°C/W
2	Thermal resistance 48LQFP, double sided PCB with 2 internal planes[2]. Natural Convection.	θ_{JA}	—	56	—	°C/W
3	Thermal resistance 48LQFP, single sided PCB[1] (@200 ft/min)	θ_{JA}	—	67	—	°C/W
4	Thermal resistance 48LQFP, double sided PCB with 2 internal planes[2] (@200 ft/min).	θ_{JA}	—	50	—	°C/W
5	Junction to Board 48LQFP[3]	θ_{JB}	—	34	—	°C/W
6	Junction to Case Top 48LQFP[4]	θ_{JCtop}	—	24	—	°C/W
7	Junction to Package Top 48LQFP[5]	Ψ_{JT}	—	6	—	°C/W
32LQFP						
8	Thermal resistance 32LQFP, single sided PCB[1] Natural Convection	θ_{JA}	—	84	—	°C/W
9	Thermal resistance 32LQFP, double sided PCB with 2 internal planes[2]. Natural Convection	θ_{JA}	—	56	—	°C/W
10	Thermal resistance 32LQFP, single sided PCB[1] (@200 ft/min)	θ_{JA}	—	71	—	°C/W
11	Thermal resistance 32LQFP, double sided PCB with 2 internal planes[2] (@200 ft/min).	θ_{JA}	—	49	—	°C/W
12	Junction to Board 32LQFP[3]	θ_{JB}	—	32	—	°C/W
13	Junction to Case Top 32LQFP[4]	θ_{JCtop}	—	23	—	°C/W
14	Junction to Package Top 32LQFP[5]	Ψ_{JT}	—	6	—	°C/W
32QFN-EP						
15	Thermal resistance 32QFN-EP, single sided PCB[1] Natural Convection	θ_{JA}	—	96	—	°C/W
16	Thermal resistance 32QFN-EP, double sided PCB with 2 internal planes[2]. Natural Convection	θ_{JA}	—	33	—	°C/W
17	Thermal resistance 32QFN-EP, single sided PCB[1] (@200 ft/min)	θ_{JA}	—	80	—	°C/W
18	Thermal resistance 32QFN-EP, double sided PCB with 2 internal planes[2] (@200 ft/min).	θ_{JA}	—	28	—	°C/W
19	Junction to Board 32QFN-EP[3]	θ_{JB}	—	13	—	°C/W
20	Junction to Case Top 32QFN-EP[4]	θ_{JCtop}	—	25	—	°C/W
21	Junction to Case Bottom 32QFN-EP[5]	$\theta_{JCbottom}$	—	2.22	—	°C/W
22	Junction to Package Top 32QFN-EP[5]	Ψ_{JT}	—	3	—	°C/W

[1] Junction to ambient thermal resistance, θ_{JA} was simulated to be equivalent to JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.

A.1.8.1 Measurement Conditions

Current is measured on VSUP. VDDX is connected to VDDA. It does not include the current to drive external loads. Unless otherwise noted the currents are measured in special single chip mode and the CPU code is executed from RAM. For Run and Wait current measurements PLL is on and the reference clock is the IRC1M trimmed to 1MHz. The bus clock frequency is set to the max value of 32MHz. Table A-13, Table A-14 and Table A-15 show the configuration of the CPMU module and the peripherals for Run, Wait and Stop current measurement.

Table A-13. CPMU Configuration for Pseudo Stop Current Measurement

CPMU REGISTER	Bit settings/Conditions
CPMUCLKS	PLLSEL=0, PSTP=1, CSAD=0, PRE=PCE=RTIOSCSEL=1 COPOSCSEL[1:0]=01
CPMUOSC	OSCE=1, External Square wave on EXTAL f_{EXTAL}=4MHz, V_{IH}= 1.8V, V_{IL}=0V
CPMURTI	RTDEC=0, RTR[6:4]=111, RTR[3:0]=1111;
CPMUCOP	WCOP=1, CR[2:0]=111

Table A-14. CPMU Configuration for Run/Wait and Full Stop Current Measurement

CPMU REGISTER	Bit settings/Conditions
CPMUSYNR	VCOFRQ[1:0]= 1,SYNDIV[5:0] = 31
CPMUPOSTDIV	POSTDIV[4:0]=0
CPMUCLKS	PLLSEL=1, CSAD=0
CPMUOSC	OSCE=0, Reference clock for PLL is f_{ref}=f_{irc1m} trimmed to 1MHz
API settings for STOP current measurement	
CPMUAPICTL	APIEA=0, APIFE=1, APIE=0
CPMUACLKTR	trimmed to >=20Khz
CPMUAPIRH/RL	set to 0xFFFF

Table A-15. Peripheral Configurations for Run & Wait Current Measurement

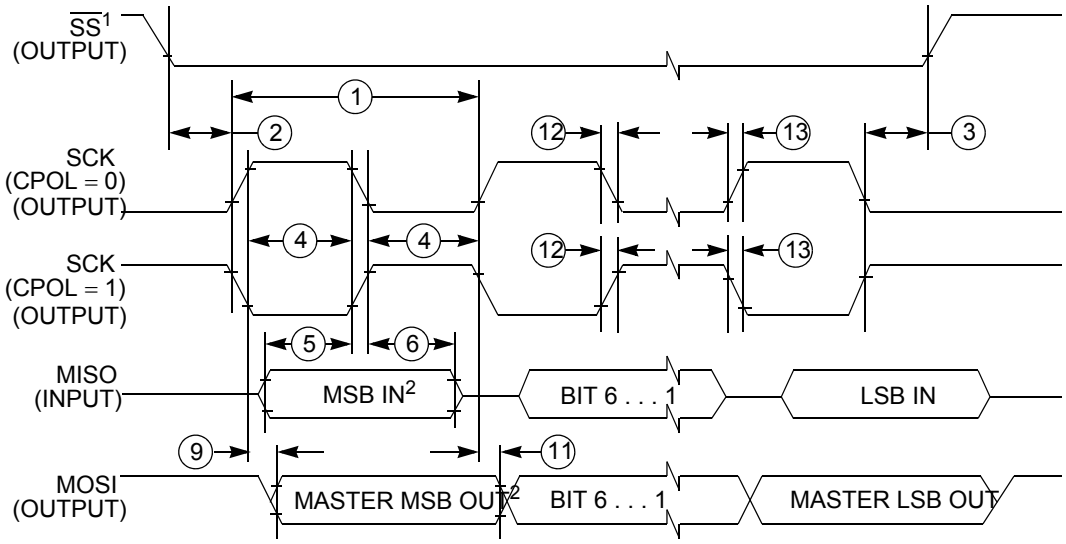
Peripheral	Configuration
SCI	Continuously transmit data (0x55) at speed of 19200 baud

F.1 Dynamic Electrical Characteristics

Table F-2. Dynamic Electrical Characteristics - Supply Voltage Sense - (BATS)

Characteristics noted under conditions $5.5V \leq V_{SUP} \leq 18V$, unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25°C$[1] under nominal conditions unless otherwise noted.						
Num	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	Enable Stabilization Time	T_{EN_UNC}	–	1	–	µs
2	Voltage Warning Low Pass Filter	f_{VWLP_filter}	–	0.5	–	Mhz

1 T_A: Ambient Temperature



1. If enabled.
2. LSBFE = 0. For LSBFE = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure K-2. SPI Master Timing (CPHA=1)

In Table K-2 the timing characteristics for master mode are listed.

Table K-2. SPI Master Mode Timing Characteristics

Num	Characteristic	Symbol				Unit
			Min	Typ	Max	
1	SCK Frequency	f_{sck}	1/2048	—	1/2	f_{bus}
1	SCK Period	t_{sck}	2	—	2048	t_{bus}
2	Enable Lead Time	t_L	—	1/2	—	t_{sck}
3	Enable Trail Time	t_T	—	1/2	—	t_{sck}
4	Clock (SCK) High or Low Time	t_{wsck}	—	1/2	—	t_{sck}
5	Data Setup Time (Inputs)	t_{su}	8	—	—	ns
6	Data Hold Time (Inputs)	t_{hi}	8	—	—	ns
9	Data Valid after SCK Edge	t_{vsck}	—	—	15	ns
10	Data Valid after $\overline{SS}$ fall (CPHA=0)	t_{vss}	—	—	15	ns
11	Data Hold Time (Outputs)	t_{ho}	20	—	—	ns
12	Rise and Fall Time Inputs	t_{rfi}	—	—	8	ns
13	Rise and Fall Time Outputs	t_{rfo}	—	—	8	ns

K.2 Slave Mode

In Figure K-3 the timing diagram for slave mode with transmission format CPHA=0 is depicted.

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THIS IS A NON–JEDEC REGISTERED PACKAGE.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
5. MIN. METAL GAP SHOULD BE 0.2 MM.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASA00656D	REV: O
QFN, THERMALLY ENHANCED, 5 X 5 X 0.85, 0.5 PITCH, 32 TERMINAL	STANDARD: NON–JEDEC	
	10 DEC 2013	