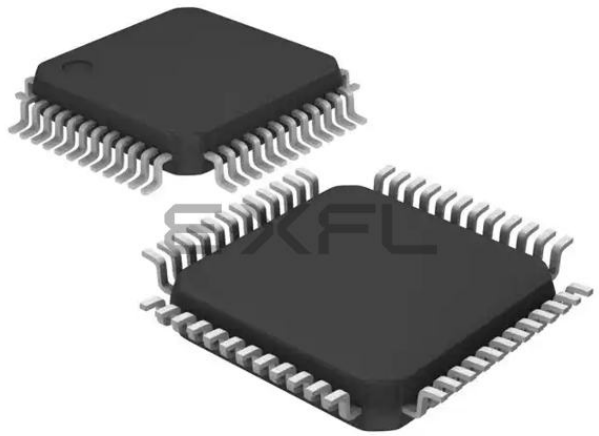

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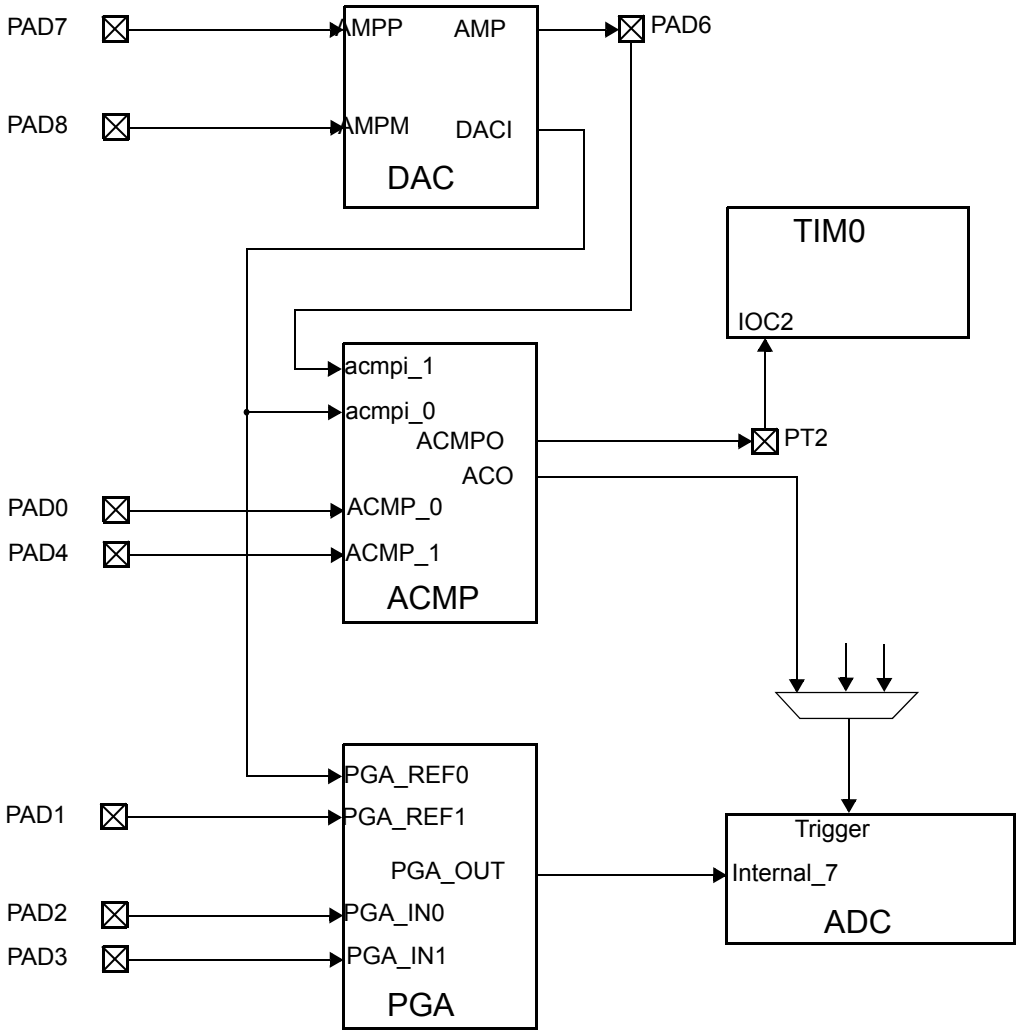

Figure 1-6. MC9S12ZVLA ACMP - PGA - DAC - ADC Connectivity

On the MC9S12ZVLA device follow ADC option bit decoding is used.

Table 1-8. ADC option bit decoding

ADC option bit OPT[1:0]	PGA input source selection
2’b00	no input selected
2’b01	PGA_IN0 is used as input voltage
2’b10	PGA_IN1 is used as input voltage
other	Reserved

Port	Pin	Pin Function & Priority	I/O	Description	Routing Register Bit	Pin Function after Reset
S	PS3	ECLK	O	Free-running clock	—	GPIO
		(IOC0_5)	I/O	TIM0 channel 5	T0C5RR	
		$\overline{SS0}$	I/O	SPI0 slave select	—	
		PTS[3]/ KWS[3]	I/O	General-purpose; with interrupt and key-wakeup	—	
	PS2	DBGEEV	I	DBG external event	—	
		TXCAN0	O	MSCAN0 transmit	CAN0RR	
		(IOC0_4)	I/O	TIM0 channel 4	T0C4RR	
		SCK0	I/O	SPI0 serial clock	—	
		PTS[2]/ KWS[2]	I/O	General-purpose; with interrupt and key-wakeup	—	
	PS1	(IOC0_3[2])	I/O	TIM0 channel 3	T0C3RR, T0IC3RR1-0	
		(TXD0)/ (LPDC0)	O	SCI0 transmit/ LPTXD0 direct control by LP0DR[LP0DR1]	S0L0RR2-0	
		(PWM6)	O	PWM option 6	PWM6RR	
		MOSI0	I/O	SPI0 master out/slave in	—	
		PTS[1]/ KWS[1]	I/O	General-purpose; with interrupt and key-wakeup	—	
	PS0	RXCAN0	I	MSCAN0 receive	CAN0RR	
		(IOC0_2)	I/O	TIM0 channel 2	T0C2RR	
		(RXD0)	I	SCI0 receive	S0L0RR2-0	
		(PWM4)	O	PWM option 4	PWM4RR	
		MISO0	I/O	SPI0 master in/slave out	—	
		PTS[0]/ KWS[0]	I/O	General-purpose; with interrupt and key-wakeup	—	

3.8 Interrupts

Table 3-6 shows the interrupt generated by the ACMP.

Table 3-6. ACMP Interrupt Sources

Module Interrupt Sources	Local Enable
ACMP interrupt	ACMPC2[ACIE]

If the handshake protocol is disabled, the access is always independent of free cycles, whereby BDC has higher priority than CPU. Since at least 2 bytes (command byte + data byte) are transferred over BKGD the maximum intrusiveness is only once every few hundred cycles.

After decoding an internal access command, the BDC then awaits the next internal core clock cycle. The relationship between BDCSI clock and core clock must be considered. If the host retrieves the data immediately, then the BDCSI clock frequency must not be more than 4 times the core clock frequency, in order to guarantee that the BDC gains bus access within 16 the BDCSI cycle DLY period following an access command. If the BDCSI clock frequency is more than 4 times the core clock frequency, then the host must use a suitable delay time before retrieving data (see 5.5.1/5-164). Furthermore, for stretched read accesses to external resources via a device expanded bus (if implemented) the potential extra stretch cycles must be taken into consideration before attempting to obtain read data.

If the access does not succeed before the host starts data retrieval then the NORESP flag is set but the access is not aborted. The NORESP state can be used by the host to recognize an unexpected access conflict due to stretched expanded bus accesses. Although the NORESP bit is set when an access does not succeed before the start of data retrieval, the access may succeed in following bus cycles if the internal access has already been initiated.

5.4.10 Single Stepping

When a STEP1 command is issued to the BDC in active BDM, the CPU executes a single instruction in the user code and returns to active BDM. The STEP1 command can be issued repeatedly to step through the user code one instruction at a time.

If an interrupt is pending when a STEP1 command is issued, the interrupt stacking operation occurs but no user instruction is executed. In this case the stacking counts as one instruction. The device re-enters active BDM with the program counter pointing to the first instruction in the interrupt service routine.

When stepping through the user code, the execution of the user code is done step by step but peripherals are free running. Some peripheral modules include a freeze feature, whereby their clocks are halted when the device enters active BDM. Timer modules typically include the freeze feature. Serial interface modules typically do not include the freeze feature. Hence possible timing relations between CPU code execution and occurrence of events of peripherals no longer exist.

If the handshake protocol is enabled and BDCCIS is set then stepping over the STOP instruction causes the Long-ACK pulse to be generated and the BDCCSR STOP flag to be set. When stop mode is exited due to an interrupt the device enters active BDM and the PC points to the start of the corresponding interrupt service routine. Stepping can be continued.

Stepping over a WAI instruction, the STEP1 command cannot be finished because active BDM cannot be entered after CPU starts to execute the WAI instruction.

Stepping over the WAI instruction causes the BDCCSR WAIT and NORESP flags to be set and, if the handshake protocol is enabled, then the Long-ACK pulse is generated. Then the device enters wait mode, clears the BDMACT bit and awaits an interrupt to leave wait mode. In this time non-intrusive BDC commands are possible, although the STEP1 has actually not finished. When an interrupt occurs the device leaves wait mode, enters active BDM and the PC points to the start of the corresponding interrupt service routine. A further ACK related to stepping over the WAI is not generated.

8.2.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field functions follow the register diagrams, in bit order.

8.2.2.1 ECC Status Register (ECCSTAT)

Module Base + 0x00000 — Access: User read only[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	RDY
W								
Reset	0	0	0	0	0	0	0	0

1 Read: Anytime
Write: Never

Figure 8-2. ECC Status Register (ECCSTAT)

Table 8-2. ECCSTAT Field Description

Field	Description
0 RDY	**ECC Ready**— Shows the status of the ECC module. 0 Internal SRAM initialization is ongoing, access to the SRAM is disabled 1 Internal SRAM initialization is done, access to the SRAM is enabled

8.2.2.2 ECC Interrupt Enable Register (ECCIE)

Module Base + 0x00001 — Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	SBEEIE
W								
Reset	0	0	0	0	0	0	0	0

1 Read: Anytime
Write: Anytime

Figure 8-3. ECC Interrupt Enable Register (ECCIE)

Table 8-3. ECCIE Field Description

Field	Description
0 SBEEIE	**Single bit ECC Error Interrupt Enable** — Enables Single ECC Error interrupt. 0 Interrupt request is disabled 1 Interrupt will be requested whenever SBEEIF is set

Figure 9-2 shows a block diagram of the XOSCLCP.

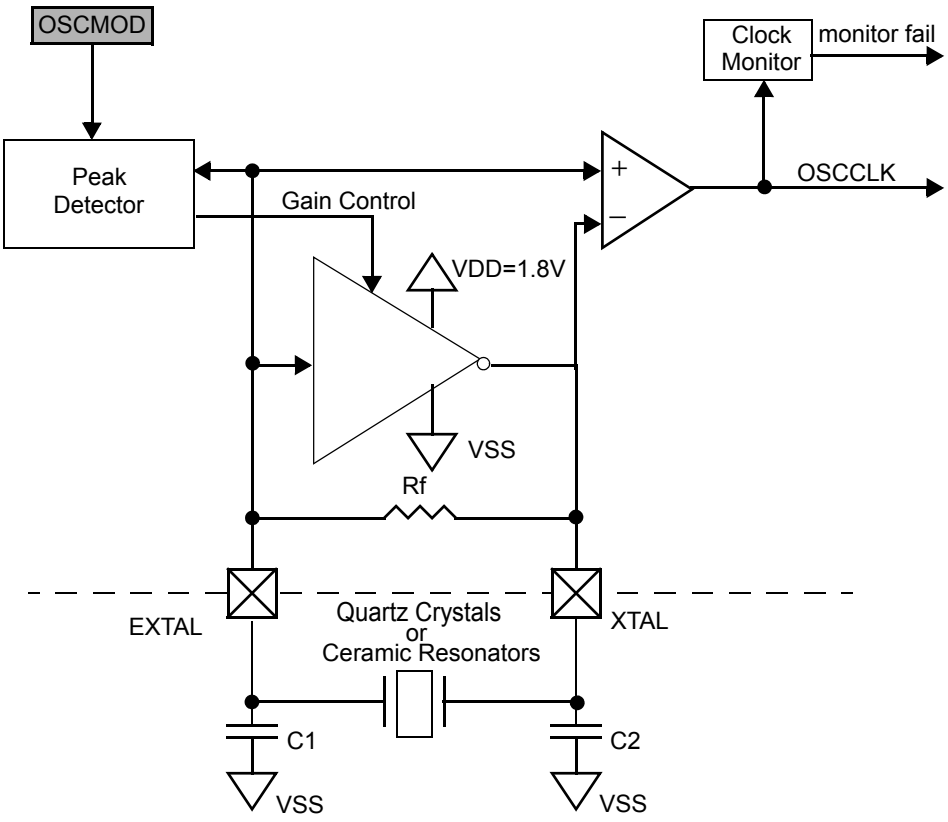

Figure 9-2. XOSCLCP Block Diagram

9.3.2.12 S12CPMU_UHV COP Control Register (CPMUCOP)

This register controls the COP (Computer Operating Properly) watchdog.

The clock source for the COP is either ACLK, IRCCLK or OSCCLK depending on the setting of the COPOSCSEL0 and COPOSCSEL1 bit (see also Table 9-8).
In Stop Mode with PSTP=1 (Pseudo Stop Mode), COPOSCSEL0=1 and COPOSCEL1=0 and PCE=1 the COP continues to run, else the COP counter halts in Stop Mode with COPOSCSEL1 =0.
In Full Stop Mode and Pseudo Stop Mode with COPOSCSEL1=1 the COP continues to run.

Module Base + 0x000C

	7	6	5	4	3	2	1	0
R	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
W			WRTMASK					
Reset	F	0	0	0	0	F	F	F

After de-assert of System Reset the values are automatically loaded from the Flash memory. See Device specification for details.

= Unimplemented or Reserved

Figure 9-15. S12CPMU_UHV COP Control Register (CPMUCOP)

Read: Anytime

Write:

1. RSBCK: Anytime in Special Mode; write to “1” but not to “0” in Normal Mode
2. WCOP, CR2, CR1, CR0:
   - — Anytime in Special Mode, when WRTMASK is 0, otherwise it has no effect
   - — Write once in Normal Mode, when WRTMASK is 0, otherwise it has no effect.
     - – Writing CR[2:0] to “000” has no effect, but counts for the “write once” condition.
     - – Writing WCOP to “0” has no effect, but counts for the “write once” condition.

When a non-zero value is loaded from Flash to CR[2:0] the COP time-out period is started.

A change of the COPOSCSEL0 or COPOSCSEL1 bit (writing a different value) or loosing UPOSC status while COPOSCSEL1 is clear and COPOSCSEL0 is set, re-starts the COP time-out period.

In Normal Mode the COP time-out period is restarted if either of these conditions is true:

1. Writing a non-zero value to CR[2:0] (anytime in special mode, once in normal mode) with WRTMASK = 0.
2. Writing WCOP bit (anytime in Special Mode, once in Normal Mode) with WRTMASK = 0.
3. Changing RSBCK bit from “0” to “1”.

In Special Mode, any write access to CPMUCOP register restarts the COP time-out period.

9.4.6 System Clock Configurations

9.4.6.1 PLL Engaged Internal Mode (PEI)

This mode is the default mode after System Reset or Power-On Reset.

The Bus Clock is based on the PLLCLK, the reference clock for the PLL is internally generated (IRC1M). The PLL is configured to 50 MHz VCOCLK with POSTDIV set to 0x03. If locked (LOCK=1) this results in a PLLCLK of 12.5 MHz and a Bus Clock of 6.25 MHz. The PLL can be re-configured to other bus frequencies.

The clock sources for COP and RTI can be based on the internal reference clock generator (IRC1M) or the RC-Oscillator (ACLK).

9.4.6.2 PLL Engaged External Mode (PEE)

In this mode, the Bus Clock is based on the PLLCLK as well (like PEI). The reference clock for the PLL is based on the external oscillator.

The clock sources for COP and RTI can be based on the internal reference clock generator or on the external oscillator clock or the RC-Oscillator (ACLK).

This mode can be entered from default mode PEI by performing the following steps:

1. Configure the PLL for desired bus frequency.
2. Enable the external Oscillator (OSCE bit).
3. Wait for oscillator to start-up and the PLL being locked (LOCK = 1) and (UPOSC =1).
4. Clear all flags in the CPMUIFLG register to be able to detect any future status bit change.
5. Optionally status interrupts can be enabled (CPMUINT register).

Loosing PLL lock status (LOCK=0) means loosing the oscillator status information as well (UPOSC=0).

The impact of loosing the oscillator status (UPOSC=0) in PEE mode is as follows:

- The PLLCLK is derived from the VCO clock (with its actual frequency) divided by four until the PLL locks again.

Application software needs to be prepared to deal with the impact of loosing the oscillator status at any time.

10.5.2 Register Descriptions

This section describes in address order all the ADC12B_LBA registers and their individual bits.

10.5.2.1 ADC Control Register 0 (ADCCTL_0)

Module Base + 0x0000

	15	14	13	12	11	10	9	8
R W	ADC_EN	ADC_SR	FRZ_MOD	SWAI	ACC_CFG[1:0]		STR_SEQA	MOD_CFG
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 10-4. ADC Control Register 0 (ADCCTL_0)

Read: Anytime

Write:

- Bits ADC_EN, ADC_SR, FRZ_MOD and SWAI writable anytime
- Bits MOD_CFG, STR_SEQA and ACC_CFG[1:0] writable if bit ADC_EN clear or bit SMOD_ACC set

Table 10-3. ADCCTL_0 Field Descriptions

Field	Description
15 ADC_EN	**ADC Enable Bit** — This bit enables the ADC (e.g. sample buffer amplifier etc.) and controls accessibility of ADC register bits. When this bit gets cleared any ongoing conversion sequence will be aborted and pending results or the result of current conversion gets discarded (not stored). The ADC cannot be re-enabled before any pending action or action in process is finished or aborted, which could take up to a maximum latency time of $t_{DISABLE}$ (see device reference manual for more details). Because internal components of the ADC are turned on/off with this bit, the ADC requires a recovery time period (t_{REC}) after ADC is enabled until the first conversion can be launched via a trigger. 0 ADC disabled. 1 ADC enabled.
14 ADC_SR	**ADC Soft-Reset** — This bit causes an ADC Soft-Reset if set after a severe error occurred (see list of severe errors in Section 10.5.2.9, “ADC Error Interrupt Flag Register (ADCEIF) that causes the ADC to cease operation). It clears all overrun flags and error flags and forces the ADC state machine to its idle state. It also clears the Command Index Register, the Result Index Register, and the CSL_SEL and RVL_SEL bits (to be ready for a new control sequence to load new command and start execution again from top of selected CSL). A severe error occurs if an error flag is set which cause the ADC to cease operation. In order to make the ADC operational again an ADC Soft-Reset must be issued. Once this bit is set it can not be cleared by writing any value. It is cleared only by ADC hardware after the Soft-Reset has been executed. 0 No ADC Soft-Reset issued. 1 Issue ADC Soft-Reset.
13 FRZ_MOD	**Freeze Mode Configuration** — This bit influences conversion flow during Freeze Mode. 0 ADC continues conversion in Freeze Mode. 1 ADC freezes the conversion at next conversion boundary at Freeze Mode entry.
12 SWAI	**Wait Mode Configuration** — This bit influences conversion flow during Wait Mode. 0 ADC continues conversion in Wait Mode. 1 ADC halts the conversion at next conversion boundary at Wait Mode entry.

10.5.2.9 ADC Error Interrupt Flag Register (ADCEIF)

If one of the following error flags is set the ADC ceases operation:

- IA_EIF
- CMD_EIF
- EOL_EIF
- TRIG_EIF

In order to make the ADC operational again an ADC Soft-Reset must be issued which clears above listed error interrupt flags.

The error interrupt flags RSTAR_EIF and LDOK_EIF do not cause the ADC to cease operation. If set the ADC continues operation. Each of the two bits can be cleared by writing a value of 1’b1. Both bits are also cleared if an ADC Soft-Reset is issued.

All bits are cleared if bit ADC_EN is clear. Writing any flag with value 1’b0 does not clear a flag. Writing any flag with value 1’b1 does not set the flag.

Module Base + 0x0008

	7	6	5	4	3	2	1	0
R	IA_EIF	CMD_EIF	EOL_EIF	Reserved	TRIG_EIF	RSTAR_EIF	LDOK_EIF	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 10-12. ADC Error Interrupt Flag Register (ADCEIF)

Read: Anytime

Write:

- Bits RSTAR_EIF and LDOK_EIF are writable anytime
- Bits IA_EIF, CMD_EIF, EOL_EIF and TRIG_EIF are not writable

Table 10-14. ADCEIF Field Descriptions

Field	Description
7 IA_EIF	**Illegal Access Error Interrupt Flag** — This flag indicates that storing the conversion result caused an illegal access error or conversion command loading from outside system RAM or NVM area occurred. The ADC ceases operation if this error flag is set (issue of type severe). 0 No illegal access error occurred. 1 An illegal access error occurred.
6 CMD_EIF	**Command Value Error Interrupt Flag** — This flag indicates that an invalid command is loaded (Any command that contains reserved bit settings) or illegal format setting selected (reserved SRES[2:0] bit settings). The ADC ceases operation if this error flag is set (issue of type severe). 0 Valid conversion command loaded. 1 Invalid conversion command loaded.
5 EOL_EIF	**“End Of List” Error Interrupt Flag** — This flag indicates a missing “End Of List” command type in current executed CSL. The ADC ceases operation if this error flag is set (issue of type severe). 0 No “End Of List” error. 1 “End Of List” command type missing in current executed CSL.

– *Function:*
Start the first conversion of a conversion sequence which is defined in the active Command Sequence List

– *Requested by:*
- Positive edge of internal interface signal Trigger
- Write Access via data bus to set control bit TRIG

– *When finished:*
This bit is cleared by the ADC when the first conversion of the sequence is beginning to sample

– *Mandatory Requirements:*
- In all ADC conversion flow control modes bit TRIG is only set (Trigger Event executed) if the Trigger Event occurs while no conversion or conversion sequence is ongoing (ADC idle)
- In ADC conversion flow control mode “Restart Mode” with a Restart Event in progress it is not allowed that a Trigger Event occurs before the background command load phase has finished (Restart Event has been executed) else the error flag TRIG_EIF is set
- In ADC conversion flow control mode “Trigger Mode” a Restart Event causes bit TRIG being set automatically. Bit TRIG is set when no conversion or conversion sequence is ongoing (ADC idle) and the RVL done condition is reached by one of the following:
* A “End Of List” command type has been executed
* A Sequence Abort Event is in progress or has been executed
The ADC executes the Restart Event followed by the Trigger Event.
- In ADC conversion flow control mode “Trigger Mode” a Restart Event and a simultaneous Trigger Event via internal interface or data bus causes the TRIG_EIF bit being set and ADC cease operation.

• **Restart Event** (with current active CSL)
Internal Interface Signal: Restart
Corresponding Bit Name: RSTA

– *Function:*
- Go to top of active CSL (clear index register for CSL)
- Load one background command register and wait for Trigger (CSL offset register is not switched independent of bit CSL_BMOD)
- Set error flag RSTA_EIF when a Restart Request occurs before one of the following conditions was reached:
* The "End Of List" command type has been executed
* Depending on bit STR_SEQA if the "End Of List" command type is about to be executed
* The current CSL has been aborted or is about to be aborted due to a Sequence Abort Request.

– *Requested by:*
- Positive edge of internal interface signal Restart
- Write Access via data bus to set control bit RSTA

11.3.4 AMPM Input Pin

This analog pin is used as input for the operational amplifier negative input pin, if the according mode is selected, see register bit DACM[2:0].

11.4 Memory Map and Register Definition

This sections provides the detailed information of all registers for the DAC_8B5V module.

11.4.1 Register Summary

Figure 11-2 shows the summary of all implemented registers inside the DAC_8B5V module.

NOTE

Register Address = Module Base Address + Address Offset, where the Module Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Address Offset / Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 DACCTL	R	FVR	DRIVE	0	0	0	DACM[2:0]		
	W								
0x0001 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0002 DACVOL	R	VOLTAGE[7:0]							
	W								
0x0003 - 0x0006 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0007 Reserved	R	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	W								

= Unimplemented

Figure 11-2. DAC_8B5V Register Summary

11.4.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

11.4.2.2 Analog Output Voltage Level Register (DACVOL)

Module Base + 0x0002 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	VOLTAGE[7:0]							
Reset	0	0	0	0	0	0	0	0

Figure 11-4. Analog Output Voltage Level Register (DACVOL)

1 Read: Anytime
Write: Anytime

Table 11-4. DACVOL Field Description

Field	Description
7:0 VOLTAGE[7:0]	**VOLTAGE** — This register defines (together with the FVR bit) the analog output voltage. For more detail see Equation 11-1 and Equation 11-2.

11.4.2.3 Reserved Register

Module Base + 0x0007 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
W								
Reset	0	0	0	0	0	0	0	0

Figure 11-5. Reserved Registerfv_dac_8b5v_RESERVED

1 Read: Anytime
Write: Only in special mode

NOTE

This reserved register bits are designed for factory test purposes only and are not intended for general user access. Writing to this register when in special modes can alter the modules functionality.

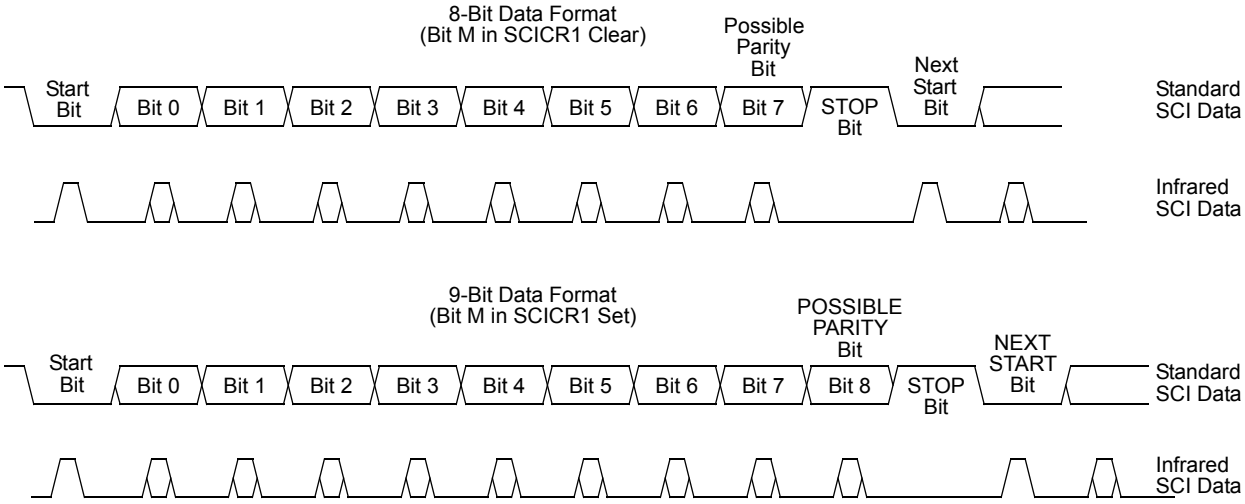

Figure 18-15. SCI Data Formats

Each data character is contained in a frame that includes a start bit, eight or nine data bits, and a stop bit. Clearing the M bit in SCI control register 1 configures the SCI for 8-bit data characters. A frame with eight data bits has a total of 10 bits. Setting the M bit configures the SCI for nine-bit data characters. A frame with nine data bits has a total of 11 bits.

Table 18-14. Example of 8-Bit Data Formats

Start Bit	Data Bits	Address Bits	Parity Bits	Stop Bit
1	8	0	0	1
1	7	0	1	1
1	7	1[1]	0	1

1 The address bit identifies the frame as an address character. See Section 18.4.6.6, “Receiver Wakeup”.

When the SCI is configured for 9-bit data characters, the ninth data bit is the T8 bit in SCI data register high (SCIDRH). It remains unchanged after transmission and can be used repeatedly without rewriting it. A frame with nine data bits has a total of 11 bits.

Table 18-15. Example of 9-Bit Data Formats

Start Bit	Data Bits	Address Bits	Parity Bits	Stop Bit
1	9	0	0	1
1	8	0	1	1
1	8	1[1]	0	1

1 The address bit identifies the frame as an address character. See Section 18.4.6.6, “Receiver Wakeup”.

18.5.2 Modes of Operation

18.5.2.1 Run Mode

Normal mode of operation.

To initialize a SCI transmission, see Section 18.4.5.2, “Character Transmission”.

18.5.2.2 Wait Mode

SCI operation in wait mode depends on the state of the SCISWAI bit in the SCI control register 1 (SCICR1).

- If SCISWAI is clear, the SCI operates normally when the CPU is in wait mode.
- If SCISWAI is set, SCI clock generation ceases and the SCI module enters a power-conservation state when the CPU is in wait mode. Setting SCISWAI does not affect the state of the receiver enable bit, RE, or the transmitter enable bit, TE.

  If SCISWAI is set, any transmission or reception in progress stops at wait mode entry. The transmission or reception resumes when either an internal or external interrupt brings the CPU out of wait mode. Exiting wait mode by reset aborts any transmission or reception in progress and resets the SCI.

18.5.2.3 Stop Mode

The SCI is inactive during stop mode for reduced power consumption. The STOP instruction does not affect the SCI register states, but the SCI bus clock will be disabled. The SCI operation resumes from where it left off after an external interrupt brings the CPU out of stop mode. Exiting stop mode by reset aborts any transmission or reception in progress and resets the SCI.

The receive input active edge detect circuit is still active in stop mode. An active edge on the receive input can be used to bring the CPU out of stop mode.

18.5.3 Interrupt Operation

This section describes the interrupt originated by the SCI block.The MCU must service the interrupt requests. Table 18-20 lists the eight interrupt sources of the SCI.

Table 18-20. SCI Interrupt Sources

Interrupt	Source	Local Enable	Description
TDRE	SCISR1[7]	TIE	Active high level. Indicates that a byte was transferred from SCIDRH/L to the transmit shift register.
TC	SCISR1[6]	TCIE	Active high level. Indicates that a transmit is complete.
RDRF	SCISR1[5]	RIE	Active high level. The RDRF interrupt indicates that received data is available in the SCI data register.
OR	SCISR1[3]		Active high level. This interrupt indicates that an overrun condition has occurred.
IDLE	SCISR1[4]	ILIE	Active high level. Indicates that receiver input has become idle.

Table 20-7. IIC Divider and Hold Values (Sheet 4 of 6)

IBC[7:0] (hex)	SCL Divider (clocks)	SDA Hold (clocks)	SCL Hold (start)	SCL Hold (stop)
59	192	18	92	98
5A	224	34	108	114
5B	256	34	124	130
5C	288	50	140	146
5D	320	50	156	162
5E	384	66	188	194
5F	480	66	236	242
60	320	34	156	162
61	384	34	188	194
62	448	66	220	226
63	512	66	252	258
64	576	98	284	290
65	640	98	316	322
66	768	130	380	386
67	960	130	476	482
68	640	66	316	322
69	768	66	380	386
6A	896	130	444	450
6B	1024	130	508	514
6C	1152	194	572	578
6D	1280	194	636	642
6E	1536	258	764	770
6F	1920	258	956	962
70	1280	130	636	642
71	1536	130	764	770
72	1792	258	892	898
73	2048	258	1020	1026
74	2304	386	1148	1154
75	2560	386	1276	1282
76	3072	514	1532	1538
77	3840	514	1916	1922
78	2560	258	1276	1282
79	3072	258	1532	1538
7A	3584	514	1788	1794
7B	4096	514	2044	2050
7C	4608	770	2300	2306
7D	5120	770	2556	2562
7E	6144	1026	3068	3074
7F	7680	1026	3836	3842
MUL=4				
80	72	28	24	44
81	80	28	28	48
82	88	32	32	52
83	96	32	36	56
84	104	36	40	60

Field	Description
1 LPWUE	LIN Wake-Up Enable — This bit controls the wake-up feature in standby mode. 0 In standby mode the wake-up feature is disabled. 1 In standby mode the wake-up feature is enabled.
0 LPPUE	LIN Pullup Resistor Enable — Selects pullup resistor. 0 The pullup resistor is high ohmic (330 kΩ). 1 The 34 kΩ pullup is switched on (except if LPE=0 or when in standby mode with LPWUE=0).

21.3.2.3 Reserved Register

Module Base + Address 0x0002 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset	x	x	x	x	x	x	x	x

= Unimplemented

Figure 21-5. LIN Test register

[1] Read: Anytime
Write: Only in special mode

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in special mode can alter the module's functionality.

Table 21-4. Reserved Register Field Description

Field	Description
7-0 Reserved	These reserved bits are used for test purposes. Writing to these bits can alter the module functionality.

21.3.2.4 LIN Slew Rate Mode Register (LPSLRM)

Module Base + Address 0x0003 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	LPDTDIS	0	0	0	0	0	LPSLR1	LPSLR0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 21-6. LIN Slew Rate Mode Register (LPSLRM)

[1] Read: Anytime
Write: Only in shutdown mode (LPE=0)

The erase-all function requires the clock divider register FCLKDIV (see Section 22.3.2.1) to be loaded before invoking this function using *soc_erase_all_req* input pin. The FCLKDIV configuration for this feature is described at device level. If FCLKDIV is not properly set the erase-all operation will not execute and the ACCERR flag in FSTAT register will set. After the execution of the erase-all function the FCLKDIV register will be reset and the value of register FCLKDIV must be loaded before launching any other command afterwards.

Before invoking the erase-all function using the *soc_erase_all_req* pin, the ACCERR and FPVIOL flags in the FSTAT register must be clear. When invoked from *soc_erase_all_req* the erase-all function will erase all P-Flash memory and EEPROM memory space regardless of the protection settings. If the post-erase verify passes, the routine will then release security by setting the SEC field of the FSEC register to the unsecure state (see Section 22.3.2.2). The security byte in the Flash Configuration Field will be programmed to the unsecure state (see Table 22-8). The status of the erase-all request is reflected in the ERSAREQ bit in the FCNFG register (see Section 22.3.2.5). The ERSAREQ bit in FCNFG will be cleared once the operation has completed and the normal FSTAT error reporting will be available as described inTable 22-46.

At the end of the erase-all sequence Protection will remain configured as it was before executing the erase-all function. If the application requires programming P-Flash and/or EEPROM after the erase-all function completes, the existing protection limits must be taken into account. If protection needs to be disabled the user may need to reset the system right after completing the erase-all function.

Table 22-46. Erase All Pin Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if command not available in current mode (see Table 22-28)
	MGSTAT1	Set if any errors have been encountered during the erase verify operation, or during the program verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the erase verify operation, or during the program verify operation

22.4.7.8 Erase Flash Block Command

The Erase Flash Block operation will erase all addresses in a P-Flash or EEPROM block.

Table 22-47. Erase Flash Block Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x09	Global address [23:16] to identify Flash block
FCCOB1	Global address [15:0] in Flash block to be erased	

Upon clearing CCIF to launch the Erase Flash Block command, the Memory Controller will erase the selected Flash block and verify that it is erased. The CCIF flag will set after the Erase Flash Block operation has completed.

Table A-8. Thermal Package Characteristics for ZVL(S)32/16/8[1]

Num	Rating	Symbol	Min	Typ	Max	Unit
48LQFP						
1	Thermal resistance 48LQFP, single sided PCB[1] Natural Convection	θ_{JA}	—	80	—	°C/W
2	Thermal resistance 48LQFP, double sided PCB with 2 internal planes[2]. Natural Convection.	θ_{JA}	—	56	—	°C/W
3	Thermal resistance 48LQFP, single sided PCB[1] (@200 ft/min)	θ_{JA}	—	67	—	°C/W
4	Thermal resistance 48LQFP, double sided PCB with 2 internal planes[2] (@200 ft/min).	θ_{JA}	—	50	—	°C/W
5	Junction to Board 48LQFP[3]	θ_{JB}	—	34	—	°C/W
6	Junction to Case Top 48LQFP[4]	θ_{JCtop}	—	24	—	°C/W
7	Junction to Package Top 48LQFP[5]	Ψ_{JT}	—	6	—	°C/W
32LQFP						
8	Thermal resistance 32LQFP, single sided PCB[1] Natural Convection	θ_{JA}	—	84	—	°C/W
9	Thermal resistance 32LQFP, double sided PCB with 2 internal planes[2]. Natural Convection	θ_{JA}	—	56	—	°C/W
10	Thermal resistance 32LQFP, single sided PCB[1] (@200 ft/min)	θ_{JA}	—	71	—	°C/W
11	Thermal resistance 32LQFP, double sided PCB with 2 internal planes[2] (@200 ft/min).	θ_{JA}	—	49	—	°C/W
12	Junction to Board 32LQFP[3]	θ_{JB}	—	32	—	°C/W
13	Junction to Case Top 32LQFP[4]	θ_{JCtop}	—	23	—	°C/W
14	Junction to Package Top 32LQFP[5]	Ψ_{JT}	—	6	—	°C/W
32QFN-EP						
15	Thermal resistance 32QFN-EP, single sided PCB[1] Natural Convection	θ_{JA}	—	96	—	°C/W
16	Thermal resistance 32QFN-EP, double sided PCB with 2 internal planes[2]. Natural Convection	θ_{JA}	—	33	—	°C/W
17	Thermal resistance 32QFN-EP, single sided PCB[1] (@200 ft/min)	θ_{JA}	—	80	—	°C/W
18	Thermal resistance 32QFN-EP, double sided PCB with 2 internal planes[2] (@200 ft/min).	θ_{JA}	—	28	—	°C/W
19	Junction to Board 32QFN-EP[3]	θ_{JB}	—	13	—	°C/W
20	Junction to Case Top 32QFN-EP[4]	θ_{JCtop}	—	25	—	°C/W
21	Junction to Case Bottom 32QFN-EP[5]	$\theta_{JCbottom}$	—	2.22	—	°C/W
22	Junction to Package Top 32QFN-EP[5]	Ψ_{JT}	—	3	—	°C/W

[1] Junction to ambient thermal resistance, θ_{JA} was simulated to be equivalent to JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.

Appendix F
BATS Electrical Specifications

This section describe the electrical characteristics of the Supply Voltage Sense module.Static Electrical Characteristics.

Table F-1. Static Electrical Characteristics - Supply Voltage Sense - (BATS)

Characteristics noted under conditions 5.5V ≤ V_{SUP} ≤ 18V, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C[1] under nominal conditions unless otherwise noted.						
Num	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	Low Voltage Warning (LBI 1)					
	Ratio = 9					
	Assert (Measured on selected pin, falling edge)	$V_{LBI1\_A\_9}$	4.75	5.5	6	V
	Deassert (Measured on selected pin, rising edge)	$V_{LBI1\_D\_9}$	–	–	6.5	V
	Hysteresis (measured on selected pin)	$V_{LBI1\_H\_9}$	–	0.4	–	V
	Ratio = 17[2]					
	Assert (Measured on selected pin, falling edge)	$V_{LBI1\_A\_17}$	5.0	5.5	6.5	V
	Deassert (Measured on selected pin, rising edge)	$V_{LBI1\_D\_17}$	–	–	7.5	V
	Hysteresis (measured on selected pin)	$V_{LBI1\_H\_17}$	–	1.0	–	V
2	Low Voltage Warning (LBI 2)					
	Ratio = 9					
	Assert (Measured on selected pin, falling edge) on S12ZVL(S)32/16/8	$V_{LBI2\_A\_9}$	5.75	6.75	7.25	V
	Assert (Measured on selected pin, falling edge) on S12ZVL(A)128/96/64	$V_{LBI2\_A\_9}$	5.5	6.75	7.25	V
	Deassert (Measured on selected pin, rising edge)	$V_{LBI2\_D\_9}$	–	–	7.75	
	Hysteresis (measured on selected pin)	$V_{LBI2\_H\_9}$	–	0.4	–	V
	Ratio = 17[2]					V
	Assert (Measured on selected pin, falling edge)	$V_{LBI2\_A\_17}$	6.5	7.5	9.0	
	Deassert (Measured on selected pin, rising edge)	$V_{LBI2\_D\_17}$	–	–	10.0	
	Hysteresis (measured on selected pin)	$V_{LBI2\_H\_17}$	–	1.0	–	
3	Low Voltage Warning (LBI 3)					
	Ratio = 9					
	Assert (Measured on selected pin, falling edge)	$V_{LBI3\_A\_9}$	7	7.75	8.5	V
	Deassert (Measured on selected pin, rising edge)	$V_{LBI3\_D\_9}$	–	–	9	V
	Hysteresis (measured on selected pin)	$V_{LBI3\_H\_9}$	–	0.4	–	V
	Ratio = 17[2]					
	Assert (Measured on selected pin, falling edge)	$V_{LBI3\_A\_17}$	6.5	7.5	8.5	V
	Deassert (Measured on selected pin, rising edge)	$V_{LBI3\_D\_17}$	–	–	9.5	V
	Hysteresis (measured on selected pin)	$V_{LBI3\_H\_17}$	–	1.0	–	V