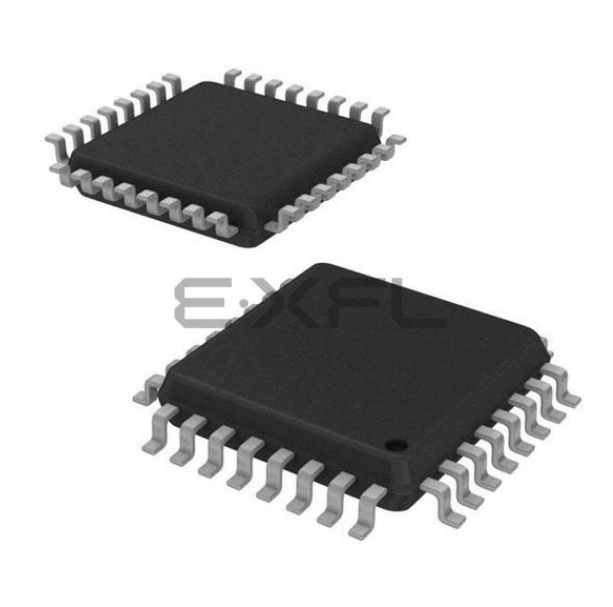

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Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
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Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
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Chapter 19
Serial Peripheral Interface (S12SPIV5)

Chapter 20
Inter-Integrated Circuit (IICV3)

Port	Pin	Pin Function & Priority	I/O	Description	Routing Register Bit	Pin Function after Reset
P	PP7[3]	(IOC1_0)	I/O	TIM1 channel 0	T1C0RR	GPIO
		PWM7	O	PWM option 7	PWM7RR	
		PTP[7]/ KWP[7]/ EVDD1	I/O	General-purpose; with interrupt and key-wakeup	—	
	PP6	PWM6	O	PWM option 6	PWM6RR	
		(ETRIG0)	I	ADC0 external trigger	TRIG0RR1:TRIG0RR0	
		PTP[6]/ KWP[6]	I/O	General-purpose; with interrupt and key-wakeup	—	
	PP5[4]	$\overline{\text{XIRQ}}$[5]	I	Non-maskable level-sensitive interrupt	—	
		PWM5	O	PWM option 5	PWM5RR	
		PTP[5]/ KWP[5]	I/O	General-purpose; with interrupt and key-wakeup	—	
	PP4	PWM4	O	PWM option 4	PWM4RR	
		PTP[4]/ KWP[4]	I/O	General-purpose; with interrupt and key-wakeup	—	
	PP3[4]	$\overline{\text{IRQ}}$	I	Maskable level- or falling edge-sensitive interrupt	—	
		PWM3	O	PWM option 3	—	
		PTP[3]/ KWP[3]	I/O	General-purpose; with interrupt and key-wakeup	—	
	PP2	PWM2	O	PWM option 2	PWM2RR	
		PTP[2]/ KWP[2]	I/O	General-purpose; with interrupt and key-wakeup	—	
	PP1[4]	(IOC1_1)	I/O	TIM1 channel 1	T1C1RR	
		PWM1	O	PWM option 1	—	
		PTP[1]/ KWP[1]	I/O	General-purpose; with interrupt and key-wakeup	—	
	PP0	PWM0	O	PWM option 0	PWM0RR	
		PTP[0]/ KWP[0]	I/O	General-purpose; with interrupt and key-wakeup	—	
J	PJ1	(TXCAN0)	O	MSCAN0 transmit	CAN0RR	GPIO
		(PWM7)	O	PWM option 7	PWM7RR	
		SCL0	I/O	IIC0	IIC0RR	
		PTJ[1]	I/O	General-purpose	—	
	PJ0	(RXCAN0)	I	MSCAN0 receive	CAN0RR	
		(PWM5)	O	PWM option 5	PWM5RR	
		SDA0	I/O	IIC0	IIC0RR	
		PTJ[0]	I/O	General-purpose	—	
L	PL0	PTIL[0]/ KWL[0]	I	General-purpose high-voltage input (HVI); with interrupt and wakeup; optional ADC link	—	GPI (HVI)

1 Function active when $\overline{\text{RESET}}$ asserted

2 Routable input capture function

Table 7-17 shows the effect for RWE and RW on the comparison conditions. These bits are ignored if INST is set, because matches based on opcodes reaching the execution stage are data independent.

Table 7-17. Read or Write Comparison Logic Table

RWE Bit	RW Bit	RW Signal	Comment
0	x	0	RW not used in comparison
0	x	1	RW not used in comparison
1	0	0	Write match
1	0	1	No match
1	1	0	No match
1	1	1	Read match

7.3.2.9 Debug Comparator A Address Register (DBGAAH, DBGAAM, DBGAAL)

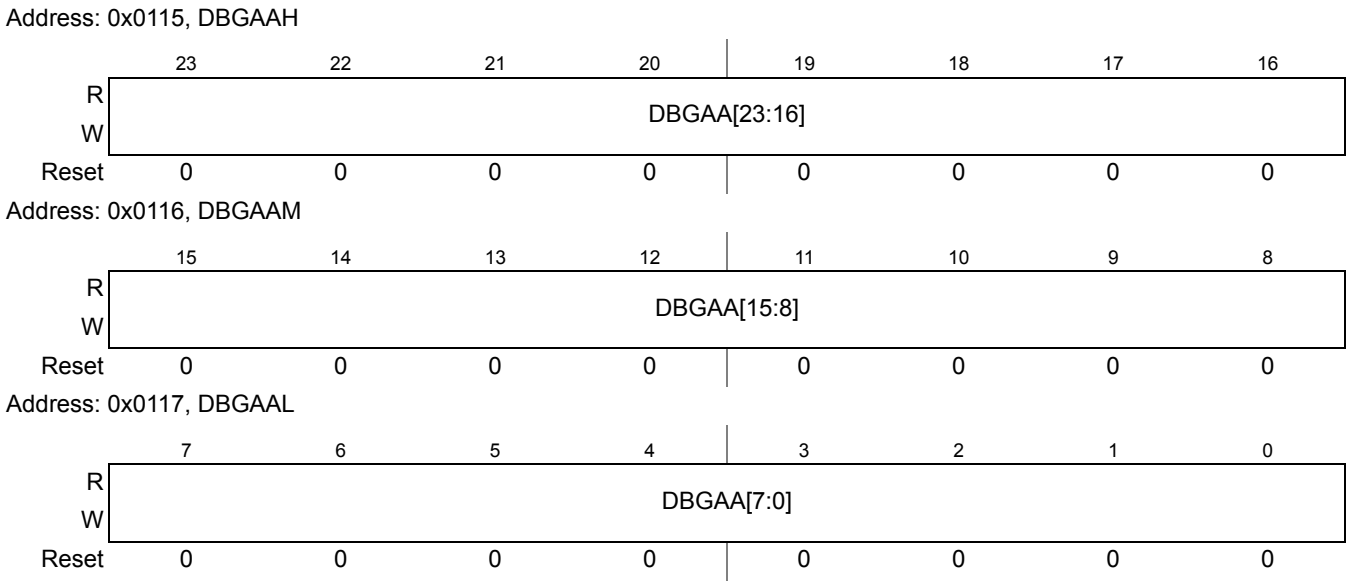


Figure 7-12. Debug Comparator A Address Register

Read: Anytime.

Write: If DBG not armed.

Table 7-18. DBGAAH, DBGAAM, DBGAAL Field Descriptions

Field	Description
23–16 DBGAA [23:16]	**Comparator Address Bits [23:16]**— These comparator address bits control whether the comparator compares the address bus bits [23:16] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one
15–0 DBGAA [15:0]	**Comparator Address Bits [15:0]**— These comparator address bits control whether the comparator compares the address bus bits [15:0] to a logic one or logic zero. 0 Compare corresponding address bit to a logic zero 1 Compare corresponding address bit to a logic one

7.4.2.1 Exact Address Comparator Match

With range comparisons disabled, the match condition is an exact equivalence of address bus with the value stored in the comparator address registers. Qualification of the type of access (R/W) is also possible.

Code may contain various access forms of the same address, for example a 16-bit access of ADDR[n] or byte access of ADDR[n+1] both access n+1. The comparators ensure that any access of the address defined by the comparator address register generates a match, as shown in the example of Table 7-27. Thus if the comparator address register contains ADDR[n+1] any access of ADDR[n+1] matches. This means that a 16-bit access of ADDR[n] or 32-bit access of ADDR[n-1] also match because they also access ADDR[n+1]. The right hand columns show the contents of DBGxA that would match for each access.

Table 7-27. Comparator Address Bus Matches

Access	Address	ADDR[n]	ADDR[n+1]	ADDR[n+2]	ADDR[n+3]
32-bit	ADDR[n]	Match	Match	Match	Match
16-bit	ADDR[n]	Match	Match	No Match	No Match
16-bit	ADDR[n+1]	No Match	Match	Match	No Match
8-bit	ADDR[n]	Match	No Match	No Match	No Match

If the comparator INST bit is set, the comparator address register contents are compared with the PC, the data register contents and access type bits are ignored. The comparator address register must be loaded with the address of the first opcode byte.

7.4.2.2 Address and Data Comparator Match

Comparator A features data comparators, for data access comparisons. The comparators do not evaluate if accessed data is valid. Accesses across aligned 32-bit boundaries are split internally into consecutive accesses. The data comparator mapping to accessed addresses for the CPU is shown in Table 7-28, whereby the Address column refers to the lowest 2 bits of the lowest accessed address. This corresponds to the most significant data byte.

Table 7-28. Comparator Data Byte Alignment

Address[1:0]	Data Comparator
00	DBGxD0
01	DBGxD1
10	DBGxD2
11	DBGxD3

The fixed mapping of data comparator bytes to addresses within a 32-bit data field ensures data matches independent of access size. To compare a single data byte within the 32-bit field, the other bytes within that field must be masked using the corresponding data mask registers. This ensures that any access of that byte (32-bit,16-bit or 8-bit) with matching data causes a match. If no bytes are masked then the data comparator always compares all 32-bits and can only generate a match on a 32-bit access with correct 32-bit data value. In this case, 8-bit or 16-bit accesses within the 32-bit field cannot generate a match even if the contents of the addressed bytes match because all 32-bits must match. In Table 7-29 the Access

access is always a 2 byte aligned memory access, so that no ECC check is performed and no single or double bit ECC error indication is activated.

8.3.7.2 ECC Debug Memory Read Access

Writing one to the ECCDR bit performs a debug read access from the memory address defined by register DPTR. If the ECCDR bit is cleared then the register DDATA contains the uncorrected read data from the memory. The register DECC contains the ECC value read from the memory. Independent of the ECCDRR register bit setting, the debug read access will not perform an automatic ECC repair during read access. During the debug read access no ECC check is performed, so that no single or double bit ECC error indication is activated.

If the ECCDW and the ECCDR bits are set at the same time, then only the debug write access is performed.

9.4.6 System Clock Configurations

9.4.6.1 PLL Engaged Internal Mode (PEI)

This mode is the default mode after System Reset or Power-On Reset.

The Bus Clock is based on the PLLCLK, the reference clock for the PLL is internally generated (IRC1M). The PLL is configured to 50 MHz VCOCLK with POSTDIV set to 0x03. If locked (LOCK=1) this results in a PLLCLK of 12.5 MHz and a Bus Clock of 6.25 MHz. The PLL can be re-configured to other bus frequencies.

The clock sources for COP and RTI can be based on the internal reference clock generator (IRC1M) or the RC-Oscillator (ACLK).

9.4.6.2 PLL Engaged External Mode (PEE)

In this mode, the Bus Clock is based on the PLLCLK as well (like PEI). The reference clock for the PLL is based on the external oscillator.

The clock sources for COP and RTI can be based on the internal reference clock generator or on the external oscillator clock or the RC-Oscillator (ACLK).

This mode can be entered from default mode PEI by performing the following steps:

1. Configure the PLL for desired bus frequency.
2. Enable the external Oscillator (OSCE bit).
3. Wait for oscillator to start-up and the PLL being locked (LOCK = 1) and (UPOSC =1).
4. Clear all flags in the CPMUIFLG register to be able to detect any future status bit change.
5. Optionally status interrupts can be enabled (CPMUINT register).

Loosing PLL lock status (LOCK=0) means loosing the oscillator status information as well (UPOSC=0).

The impact of loosing the oscillator status (UPOSC=0) in PEE mode is as follows:

- The PLLCLK is derived from the VCO clock (with its actual frequency) divided by four until the PLL locks again.

Application software needs to be prepared to deal with the impact of loosing the oscillator status at any time.

Table 10-3. ADCCTL_0 Field Descriptions (continued)

Field	Description
11-10 ACC_CFG[1:0]	**ADCFLWCTL Register Access Configuration** — These bits define if the register ADCFLWCTL is controlled via internal interface only or data bus only or both. See Table 10-4. for more details.
9 STR_SEQA	**Control Of Conversion Result Storage and RSTAR_EIF flag setting at Sequence Abort or Restart Event** — This bit controls conversion result storage and RSTAR_EIF flag setting when a Sequence Abort Event or Restart Event occurs as follows: *If STR_SEQA = 1'b0 and if a:* • Sequence Abort Event or Restart Event is issued during a conversion the data of this conversion is not stored and the respective conversion complete flag is not set • Restart Event only is issued before the last conversion of a CSL is finished and no Sequence Abort Event is in process (SEQA clear) causes the RSTA_EIF error flag to be asserted and bit SEQA gets set by hardware *If STR_SEQA = 1'b1 and if a:* • Sequence Abort Event or Restart Event is issued during a conversion the data of this conversion is stored and the respective conversion complete flag is set and Intermediate Result Information Register is updated. • Restart Event only occurs during the last conversion of a CSL and no Sequence Abort Event is in process (SEQA clear) does not set the RSTA_EIF error flag • Restart Event only is issued before the CSL is finished and no Sequence Abort Event is in process (SEQA clear) causes the RSTA_EIF error flag to be asserted and bit SEQA gets set by hardware
8 MOD_CFG	**(Conversion Flow Control) Mode Configuration** — This bit defines the conversion flow control after a Restart Event and after execution of the "End Of List" command type: - Restart Mode - Trigger Mode (For more details please see also section Section 10.6.3.2, "Introduction of the Programmer's Model and following.) 0 "Restart Mode" selected. 1 "Trigger Mode" selected.

Table 10-4. ADCFLWCTL Register Access Configurations

ACC_CFG[1]	ACC_CFG[0]	ADCFLWCTL Access Mode
0	0	None of the access paths is enabled (default / reset configuration)
0	1	Single Access Mode - Internal Interface (ADCFLWCTL access via internal interface only)
1	0	Single Access Mode - Data Bus (ADCFLWCTL access via data bus only)
1	1	Dual Access Mode (ADCFLWCTL register access via internal interface and data bus)

10.5.2.7 ADC Error Interrupt Enable Register (ADCEIE)

Module Base + 0x0006

	7	6	5	4	3	2	1	0
R	IA_EIE	CMD_EIE	EOL_EIE	Reserved	TRIG_EIE	RSTAR_EIE	LDOK_EIE	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 10-10. ADC Error Interrupt Enable Register (ADCEIE)

Read: Anytime

Write: Anytime

Table 10-12. ADCEIE Field Descriptions

Field	Description
7 IA_EIE	**Illegal Access Error Interrupt Enable Bit** — This bit enables the illegal access error interrupt. 0 Illegal access error interrupt disabled. 1 Illegal access error interrupt enabled.
6 CMD_EIE	**Command Value Error Interrupt Enable Bit** — This bit enables the command value error interrupt. 0 Command value interrupt disabled. 1 Command value interrupt enabled.
5 EOL_EIE	**"End Of List" Error Interrupt Enable Bit** — This bit enables the "End Of List" error interrupt. 0 "End Of List" error interrupt disabled. 1 "End Of List" error interrupt enabled.
3 TRIG_EIE	**Conversion Sequence Trigger Error Interrupt Enable Bit** — This bit enables the conversion sequence trigger error interrupt. 0 Conversion sequence trigger error interrupt disabled. 1 Conversion sequence trigger error interrupt enabled.
2 RSTAR_EIE	**Restart Request Error Interrupt Enable Bit**— This bit enables the restart request error interrupt. 0 Restart Request error interrupt disabled. 1 Restart Request error interrupt enabled.
1 LDOK_EIE	**Load OK Error Interrupt Enable Bit** — This bit enables the Load OK error interrupt. 0 Load OK error interrupt disabled. 1 Load OK error interrupt enabled.

10.6.3.2.1 Introduction of The Command Sequence List (CSL) Format

A Command Sequence List (CSL) contains up to 64 conversion commands. A user selectable number of successive conversion commands in the CSL can be grouped as a command sequence. This sequence of conversion commands is successively executed by the ADC at the occurrence of a Trigger Event. The commands of a sequence are successively executed until an “End Of Sequence” or “End Of List” command type identifier in a command is detected (command type is coded via bits CMD_SEL[1:0]). The number of successive conversion commands that belong to a command sequence and the number of command sequences inside the CSL can be freely defined by the user and is limited by the 64 conversion commands a CSL can contain. A CSL must contain at least one conversion command and one “end of list” command type identifier. The minimum number of command sequences inside a CSL is zero and the maximum number of command sequences is 63. A command sequence is defined with bits CMD_SEL[1:0] in the register ADCCMD_M by defining the end of a conversion sequence. The Figure 10-29 and Figure 10-30 provides examples of a CSL.

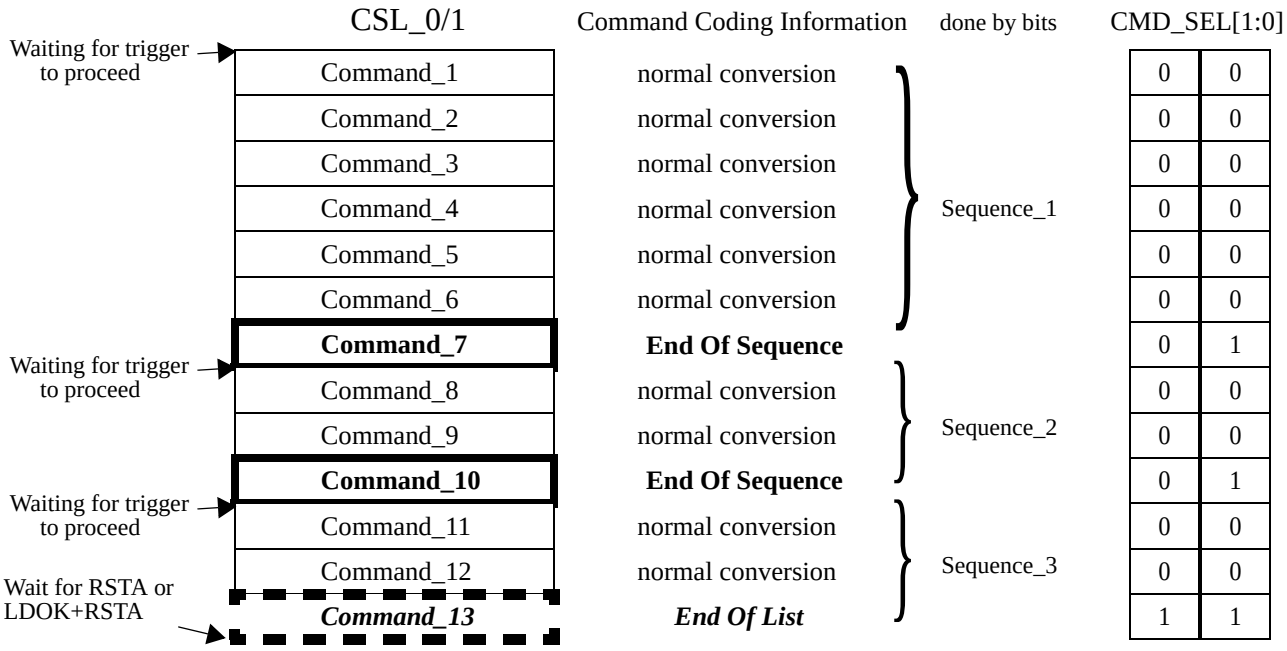


Figure 10-29. Example CSL with sequences and an “End Of List” command type identifier

Table 13-23. CANIDMR0–CANIDMR3 Register Field Descriptions

Field	Description
7-0 AM[7:0]	**Acceptance Mask Bits** — If a particular bit in this register is cleared, this indicates that the corresponding bit in the identifier acceptance register must be the same as its identifier bit before a match is detected. The message is accepted if all such bits match. If a bit is set, it indicates that the state of the corresponding bit in the identifier acceptance register does not affect whether or not the message is accepted. 0 Match corresponding acceptance code register and identifier bits 1 Ignore corresponding acceptance code register bit

Module Base + 0x001C to Module Base + 0x001F — Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
Reset	0	0	0	0	0	0	0	0

Figure 13-22. MSCAN Identifier Mask Registers (Second Bank) — CANIDMR4–CANIDMR7

1 Read: Anytime
Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 13-24. CANIDMR4–CANIDMR7 Register Field Descriptions

Field	Description
7-0 AM[7:0]	**Acceptance Mask Bits** — If a particular bit in this register is cleared, this indicates that the corresponding bit in the identifier acceptance register must be the same as its identifier bit before a match is detected. The message is accepted if all such bits match. If a bit is set, it indicates that the state of the corresponding bit in the identifier acceptance register does not affect whether or not the message is accepted. 0 Match corresponding acceptance code register and identifier bits 1 Ignore corresponding acceptance code register bit

13.3.3 Programmer's Model of Message Storage

The following section details the organization of the receive and transmit message buffers and the associated control registers.

To simplify the programmer interface, the receive and transmit message buffers have the same outline. Each message buffer allocates 16 bytes in the memory map containing a 13 byte data structure.

An additional transmit buffer priority register (TBPR) is defined for the transmit buffers. Within the last two bytes of this memory map, the MSCAN stores a special 16-bit time stamp, which is sampled from an internal timer after successful transmission or reception of a message. This feature is only available for transmit and receiver buffers, if the TIME bit is set (see Section 13.3.2.1, "MSCAN Control Register 0 (CANCTL0)").

The time stamp register is written by the MSCAN. The CPU can only read these registers.

16.3.2.6 Timer Control Register 1/Timer Control Register 2 (TCTL1/TCTL2)

Module Base + 0x0008

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Figure 16-10. Timer Control Register 1 (TCTL1)

Module Base + 0x0009

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	OM1	OL1	OM0	OL0
Reset	0	0	0	0	0	0	0	0

Figure 16-11. Timer Control Register 2 (TCTL2)

Read: Anytime

Write: Anytime

Table 16-6. TCTL1/TCTL2 Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero

Field	Description
1:0 OMx	**Output Mode** — These two pairs of control bits are encoded to specify the output action to be taken as a result of a successful OCx compare. When either OMx or OLx is 1, the pin associated with OCx becomes an output tied to OCx. **Note:** For an output line to be driven by an OCx the OCPDx must be cleared.
1:0 OLx	**Output Level** — These two pairs of control bits are encoded to specify the output action to be taken as a result of a successful OCx compare. When either OMx or OLx is 1, the pin associated with OCx becomes an output tied to OCx. **Note:** For an output line to be driven by an OCx the OCPDx must be cleared.

Table 16-7. Compare Result Output Action

OMx	OLx	Action
0	0	No output compare action on the timer output signal
0	1	Toggle OCx output line
1	0	Clear OCx output line to zero
1	1	Set OCx output line to one

Table 19-2. SPICR1 Field Descriptions (continued)

Field	Description
3 CPOL	**SPI Clock Polarity Bit** — This bit selects an inverted or non-inverted SPI clock. To transmit data between SPI modules, the SPI modules must have identical CPOL values. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 Active-high clocks selected. In idle state SCK is low. 1 Active-low clocks selected. In idle state SCK is high.
2 CPHA	**SPI Clock Phase Bit** — This bit is used to select the SPI clock format. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 Sampling of data occurs at odd edges (1,3,5,...) of the SCK clock. 1 Sampling of data occurs at even edges (2,4,6,...) of the SCK clock.
1 SSOE	**Slave Select Output Enable** — The $\overline{SS}$ output feature is enabled only in master mode, if MODFEN is set, by asserting the SSOE as shown in Table 19-3. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state.
0 LSBFE	**LSB-First Enable** — This bit does not affect the position of the MSB and LSB in the data register. Reads and writes of the data register always have the MSB in the highest bit position. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 Data is transferred most significant bit first. 1 Data is transferred least significant bit first.

Table 19-3. $\overline{SS}$ Input / Output Selection

MODFEN	SSOE	Master Mode	Slave Mode
0	0	$\overline{SS}$ not used by SPI	$\overline{SS}$ input
0	1	$\overline{SS}$ not used by SPI	$\overline{SS}$ input
1	0	$\overline{SS}$ input with MODF feature	$\overline{SS}$ input
1	1	$\overline{SS}$ is slave select output	$\overline{SS}$ input

19.3.2.2 SPI Control Register 2 (SPICR2)

Module Base +0x0001

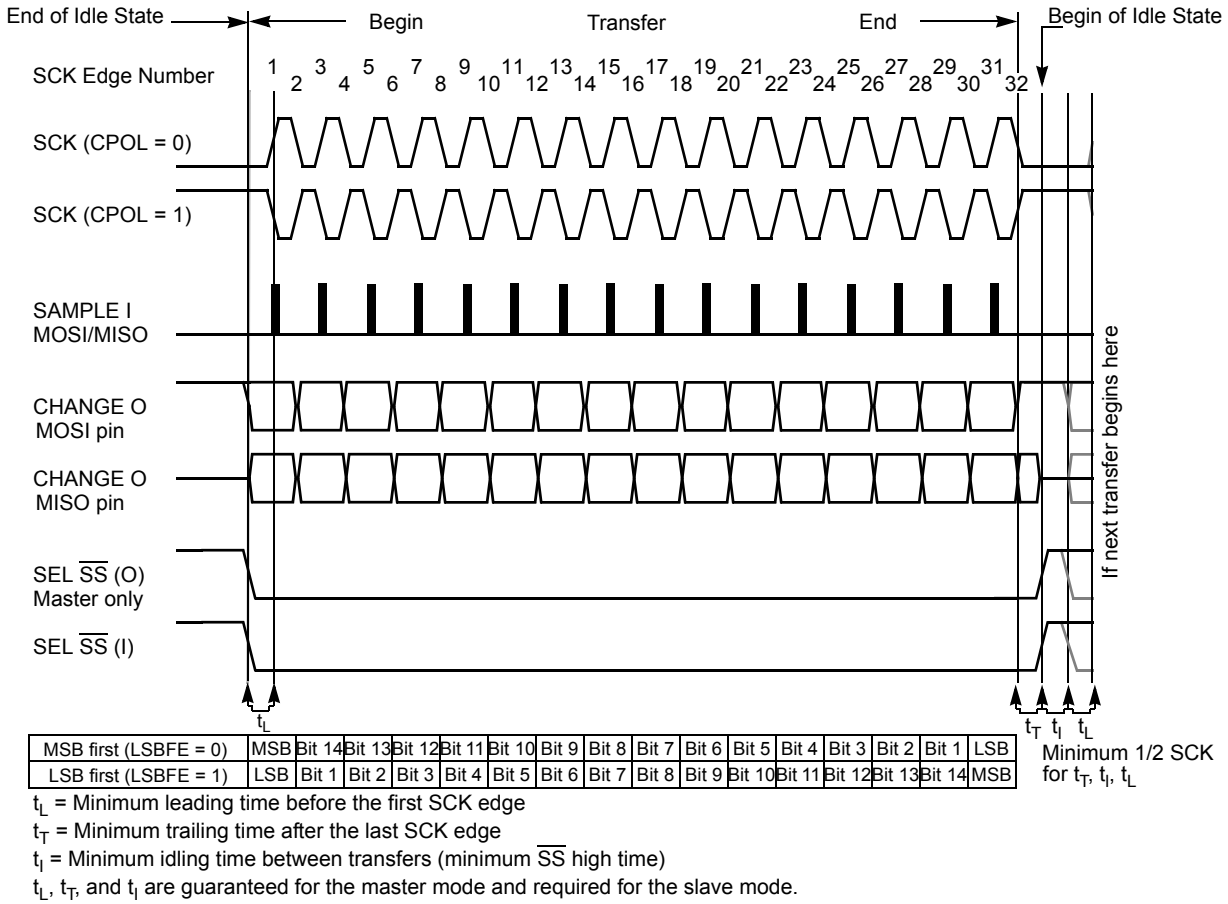
	7	6	5	4	3	2	1	0
R	0	XFRW	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 19-4. SPI Control Register 2 (SPICR2)

Read: Anytime

Write: Anytime; writes to the reserved bits have no effect



t_L = Minimum leading time before the first SCK edge
t_T = Minimum trailing time after the last SCK edge
t_I = Minimum idling time between transfers (minimum $\overline{SS}$ high time)
t_L, t_T, and t_I are guaranteed for the master mode and required for the slave mode.

Figure 19-13. SPI Clock Format 0 (CPHA = 0), with 16-Bit Transfer Width selected (XFRW = 1)

In slave mode, if the $\overline{SS}$ line is not deasserted between the successive transmissions then the content of the SPI data register is not transmitted; instead the last received data is transmitted. If the $\overline{SS}$ line is deasserted for at least minimum idle time (half SCK cycle) between successive transmissions, then the content of the SPI data register is transmitted.

In master mode, with slave select output enabled the $\overline{SS}$ line is always deasserted and reasserted between successive transfers for at least minimum idle time.

19.4.3.3 CPHA = 1 Transfer Format

Some peripherals require the first SCK edge before the first data bit becomes available at the data out pin, the second edge clocks data into the system. In this format, the first SCK edge is issued by setting the CPHA bit at the beginning of the n[1]-cycle transfer operation.

The first edge of SCK occurs immediately after the half SCK clock cycle synchronization delay. This first edge commands the slave to transfer its first data bit to the serial data input pin of the master.

A half SCK cycle later, the second edge appears on the SCK pin. This is the latching edge for both the master and slave.

1. n depends on the selected transfer width, please refer to Section 19.3.2.2, “SPI Control Register 2 (SPICR2)

Table 22-48. Erase Flash Block Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 22-28)
		Set if an invalid global address [23:0] is supplied
		Set if the supplied P-Flash address is not phrase-aligned or if the EEPROM address is not word-aligned
	FPVIOL	Set if an area of the selected Flash block is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

22.4.7.9 Erase P-Flash Sector Command

The Erase P-Flash Sector operation will erase all addresses in a P-Flash sector.

Table 22-49. Erase P-Flash Sector Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x0A	Global address [23:16] to identify P-Flash block to be erased
FCCOB1	Global address [15:0] anywhere within the sector to be erased. Refer to Section 22.1.2.1 for the P-Flash sector size.	

Upon clearing CCIF to launch the Erase P-Flash Sector command, the Memory Controller will erase the selected Flash sector and then verify that it is erased. The CCIF flag will be set after the Erase P-Flash Sector operation has completed.

Table 22-50. Erase P-Flash Sector Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 001 at command launch
		Set if command not available in current mode (see Table 22-28)
		Set if an invalid global address [23:0] is supplied see Table 22-2)
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
	FPVIOL	Set if the selected P-Flash sector is protected
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

Table A-1. Revision History Table

Revision Number	Revision Date	Description Of Changes
0.50	14 March 2016	• added the latest characterization data, updated: Table A-11, Table A-19 • change voltage specification for MC9S12ZVL128/96/64 analog modules to VDDX ±3%:
0.60	31 March 2016	• update V_{BG} output voltage and V_{BG} voltage distribution specification: Table B-1
0.70	18 April 2016	• correct min V_{DDX} specification for MC9S12ZVL128/96/64 device: Table B-1
0.80	20 June 2016	• update Table A-19, add missing stop current for 85°C and 105°C, correct stop value for 125°C • update Table I-2, set ACMP input offset to 25mV
0.90	08 August 2017	• added 175°C parameters • update current injection consideration, section **Section C.1.1.4 Current Injection**
1.0	12 September 2017	• added 175°C Run and Wait current parameters
1.1	10 October 2017	• added Pin input leakage values for Pins PAD0 and PAD1 at 150°C < T_J < 175°C, Table A-10 • added Pin input leakage values for Pins PP1,PP3,PP5 and PP7 at 150°C < T_J < 175°C, Table A-10 • changed typical Reduced Performance Mode V_{DDX} Voltage to 5.0V, Table B-1
1.2	19 October 2017	• correct max value for Input leakage current on PP1, PP3, PP5 and PP7 for 150°C < T_J < 175°C on Table A-10
1.21	24 October 2017	• fixed minor bug in this revision history to make sure all updates are correct documented

A.1 General

This supplement contains the most accurate electrical information for the MC9S12ZVL-Family available at the time of publication.

This introduction is intended to give an overview on several common topics like power supply, current injection etc.

Table A-2. Power Supplies

Mnemonic	Nominal Voltage	Description
VSS	0V	Ground pin for 1.8V core supply voltage generated by on chip voltage regulator
VDDX	5.0 V	5V power supply output for I/O drivers generated by on chip voltage regulator if VREG5VEN is set
VDDX	3.3 V	3.3V power supply output for I/O drivers generated by on chip voltage regulator if VREG5VEN is cleared
VSSX1	0V	Ground pin for I/O drivers

Table B-1. Voltage Regulator Electrical Characteristics

-40°C ≤T_J ≤ 175°C unless noted otherwise, V_{DDA} and V_{DDX} must be shorted on the application board.						
Num	**Characteristic**	**Symbol**	**Min**	**Typical**	**Max**	**Unit**
19a	V_{BG} voltage Distribution over temperature T_J V_{SUP} = 12V, -40°C ≤ T_J ≤ 150°C, VDDX = 5V	Δ_{VBGV5V}	-20		20	mV
19b	V_{BG} voltage Distribution over temperature T_J V_{SUP} = 12V, -40°C ≤ T_J ≤ 150°C, VDDX= 3.3V	$\Delta_{VBGV3V3}$	-25		25	mV
20	Base Current For External PNP (V_{DDX})[10] -40°C ≤ T_J ≤ 150°C 150°C <T_J < 175°C	$I_{BCTLMAX}$	 2.3 1.5	 — —	 — —	mA
21	Recovery time from STOP	t_{STP_REC}	—	23	—	µs

1 3% Vreg tolerance

2 Please note that the core current is derived from V_{DDX}

3 Further limitation may apply due to maximum allowable T_J

4 2% Vreg tolerance, MC9S12ZVLA device only

5 LVI is monitored on the V_{DDA} supply domain

6 LVRX is monitored on the V_{DDX} supply domain only active during full performance mode. During reduced performance mode (stopmode) voltage supervision is solely performed by the POR block monitoring core V_{DD}.

7 the ACLK is not factory trimmed, the customer can use the CPMUACLKTR register to trim the ACLK, see also 9.3.2.19, “Autonomous Clock Trimming Register (CPMUACLKTR)

8 The ACLK trimming must be set that the minimum period equals to 0.2ms

9 CPMUHTTR=0x88

10 This is the minimum base current that can be guaranteed when the external PNP is delivering maximum current.

NOTE

The LVR monitors the voltages VDD, VDDF and VDDX. If the voltage drops on these supplies to a level which could prohibit the correct function (e.g. code execution) of the micro controller, the LVR triggers.

Table B-2. Recommended Capacitor Values

V_{DDA} and V_{DDX} must be shorted on the application board.				
Num	**Characteristic**	**Symbol**	**Typical[1]**	**Unit**
1	VDDX capacitor[2]	C_{VDDX}	100-220	nF
2	VDDA capacitor[3]	C_{VDDA}	100-220	nF
3	Stability capacitor[4,5]	C_{VDD5}	4.7-10	µF

[1]Values are nominal component values

[2]X7R ceramics

[3]X7R ceramics

[4]Can be placed anywhere on the 5V supply node (VDDA, VDDX)

[5]4.7µF X7R ceramics or 10µF tantalum

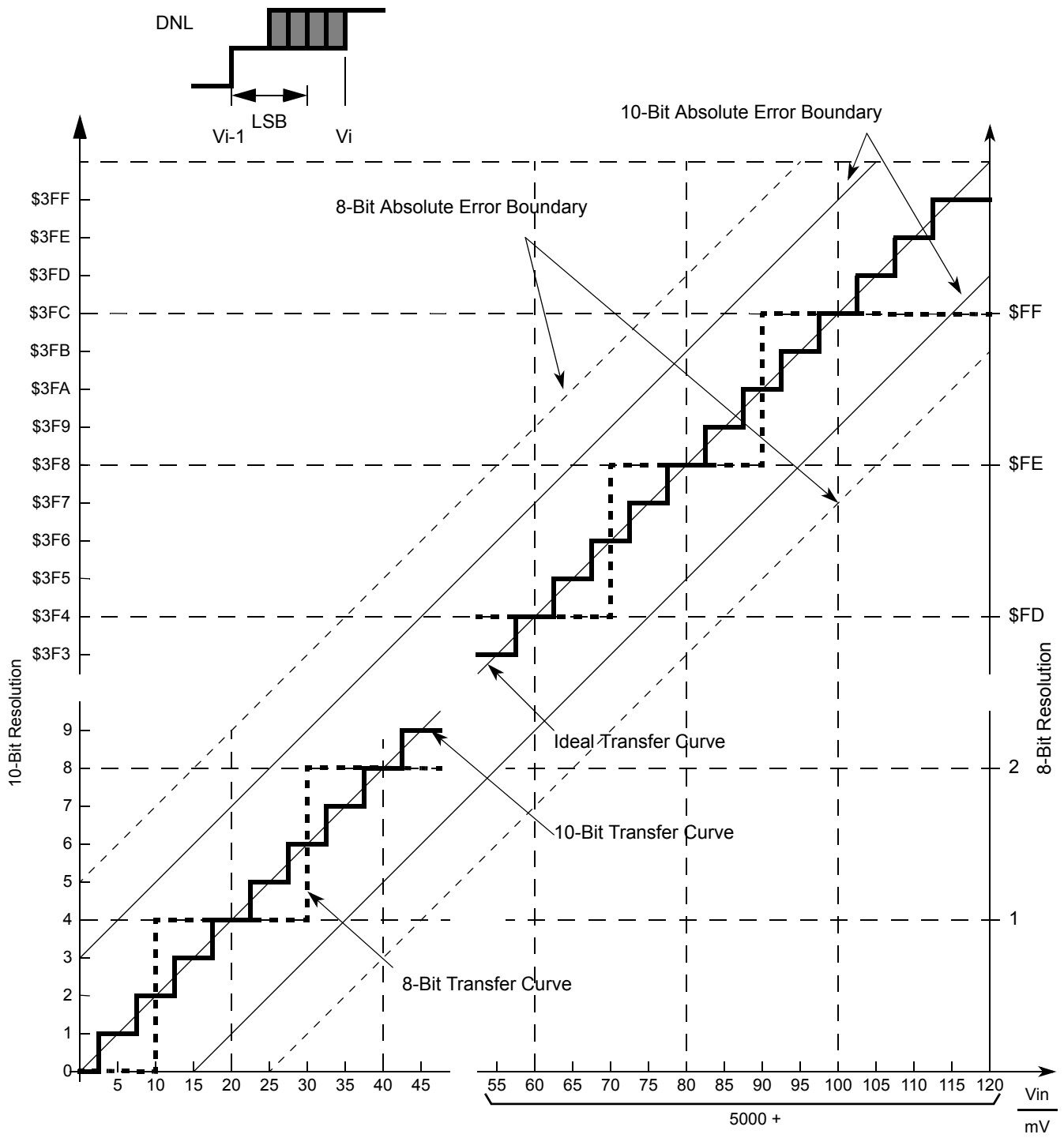


Figure C-2. ADC Accuracy Definitions

NOTE

Figure C-2 shows only definitions, for specification values refer to Table C-3 and Table C-4.

O.19 0x0780-0x0787 SPI0

Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0780	SPI0CR1	R	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
		W								
0x0781	SPI0CR2	R	0	XFRW	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
		W								
0x0782	SPI0BR	R	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
		W								
0x0783	SPI0SR	R	SPIF	0	SPTEF	MODF	0	0	0	0
		W								
0x0784	SPI0DRH	R	R15	R14	R13	R12	R11	R10	R9	R8
		W	T15	T14	T13	T12	T11	T10	T9	T8
0x0785	SPI0DRL	R	R7	R6	R5	R4	R3	R2	R1	R0
		W	T7	T6	T5	T4	T3	T2	T1	T0
0x0786	Reserved	R								
		W								
0x0787	Reserved	R								
		W								