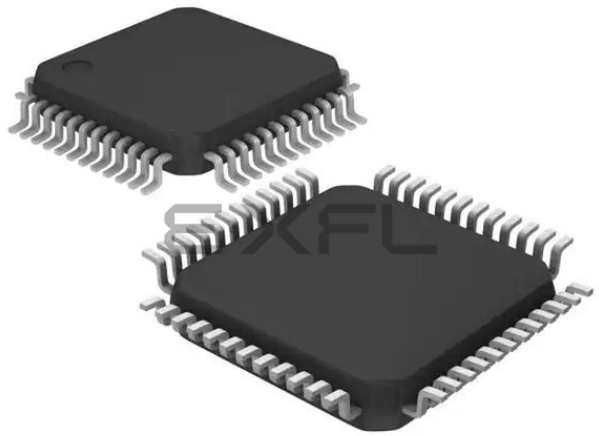

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Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SCI, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	5.5V ~ 18V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvl64f0clfr

1.4.2.2 Flash

On-chip flash memory on the MC9S12ZVL-Family

- Up to 128 KB of program flash memory
  - Automated program and erase algorithm
  - Protection scheme to prevent accidental program or erase

1.4.2.3 EEPROM

- Up to 2048 bytes EEPROM
  - 16 data bits plus 6 syndrome ECC (error correction code) bits allow single bit error correction and double fault detection
  - Erase sector size 4 bytes
  - Automated program and erase algorithm
  - User margin level setting for reads

1.4.2.4 SRAM

- Up to 8 KB of general-purpose RAM with ECC
  - Single bit error correction and double bit error detection code based on 16-bit data words

1.4.3 Clocks, Reset & Power Management Unit (CPMU)

- Real time interrupt (RTI)
- Clock monitor, supervising the correct function of the oscillator (CM)
- Computer operating properly (COP) watchdog
  - Configurable as window COP for enhanced failure detection
  - Can be initialized out of reset using option bits located in flash memory
- System reset generation
- Autonomous periodic interrupt (API) (combination with cyclic, watchdog)
- Low Power Operation
  - RUN mode is the main full performance operating mode with the entire device clocked.
  - WAIT mode when the internal CPU clock is switched off, so the CPU does not execute instructions.
  - Pseudo STOP - system clocks are stopped but the oscillator the RTI, the COP, and API modules can be enabled
  - STOP - the oscillator is stopped in this mode, all clocks are switched off and all counters and dividers remain frozen, with the exception of the COP and API which can optionally run from ACLK.

1.4.3.1 Internal Phase-Locked Loop (IPLL)

- Phase-locked-loop clock frequency multiplier

1.7.2.24 BDC and Debug Signals

1.7.2.24.1 BKGD — Background Debug signal

The BKGD signal is used as a pseudo-open-drain signal for the background debug communication. The BKGD signal has an internal pull-up device.

1.7.2.24.2 DBGEEV — External Event Input

This signal is the DBG external event input. It is input only. Within the DBG module, it allows an external event to force a state sequencer transition. A falling edge at the external event signal constitutes an event. Rising edges have no effect. The maximum frequency of events is half the internal core bus frequency.

1.7.2.25 CAN0 Signals

1.7.2.25.1 RXCAN0 Signal

This signal is associated with the receive functionality of the scalable controller area network controller (MSCAN0).

1.7.2.25.2 TXCAN0 Signal

This signal is associated with the transmit functionality of the scalable controller area network controller (MSCAN0).

1.7.2.26 LIN Physical Layer Signals

1.7.2.26.1 LIN

This pad is connected to the single-wire LIN data bus.

1.7.2.26.2 LPTXD

This is the LIN physical layer transmitter input signal.

1.7.2.26.3 LPRXD

This is the LIN physical layer receiver output signal.

1.7.2.26.4 LPDR1

This is the LIN LP0DR1 register bit, visible at the designated pin for debug purposes.

1.7.2.27 BCTL

BCTL is the ballast connection for the on chip voltage regulator. It provides the base current of an external PNP transistor of the VDDX and VDDA supplies.

Port	Pin	Pin Function & Priority	I/O	Description	Routing Register Bit	Pin Function after Reset
S	PS3	ECLK	O	Free-running clock	—	GPIO
		(IOC0_5)	I/O	TIM0 channel 5	T0C5RR	
		$\overline{SS0}$	I/O	SPI0 slave select	—	
		PTS[3]/ KWS[3]	I/O	General-purpose; with interrupt and key-wakeup	—	
	PS2	DBGEEV	I	DBG external event	—	
		TXCAN0	O	MSCAN0 transmit	CAN0RR	
		(IOC0_4)	I/O	TIM0 channel 4	T0C4RR	
		SCK0	I/O	SPI0 serial clock	—	
		PTS[2]/ KWS[2]	I/O	General-purpose; with interrupt and key-wakeup	—	
	PS1	(IOC0_3[2])	I/O	TIM0 channel 3	T0C3RR, T0IC3RR1-0	
		(TXD0)/ (LPDC0)	O	SCI0 transmit/ LPTXD0 direct control by LP0DR[LP0DR1]	S0L0RR2-0	
		(PWM6)	O	PWM option 6	PWM6RR	
		MOSI0	I/O	SPI0 master out/slave in	—	
		PTS[1]/ KWS[1]	I/O	General-purpose; with interrupt and key-wakeup	—	
	PS0	RXCAN0	I	MSCAN0 receive	CAN0RR	
		(IOC0_2)	I/O	TIM0 channel 2	T0C2RR	
		(RXD0)	I	SCI0 receive	S0L0RR2-0	
		(PWM4)	O	PWM option 4	PWM4RR	
		MISO0	I/O	SPI0 master in/slave out	—	
		PTS[0]/ KWS[0]	I/O	General-purpose; with interrupt and key-wakeup	—	

Global Address	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x033F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0340–0x037F	Reserved	R	0	0	0	0	0	0	0	0
		W								

2.3.2 PIM Registers 0x0200-0x020F

This section details the specific purposes of register implemented in address range 0x0200-0x020F. These registers serve for specific PIM related functions not part of the generic port registers.

- If not stated differently, writing to reserved bits has no effect and read returns zero.
- All register read accesses are synchronous to internal clocks.
- Register bits can be written at any time if not stated differently.

2.3.2.1 Module Routing Register 0 (MODRR0)

Address 0x0200 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	CAN0RR	IIC0RR	SCI1RR	S0L0RR2-0		
W								
	—	—	TXCAN0 RXCAN0	SDA0 SCL0	TXD1 RXD1	SCI0-LINPHY0 (see Figure 2-2)		
Reset	0	0	0	0	0	0	0	0

Figure 2-1. Module Routing Register 0 (MODRR0)

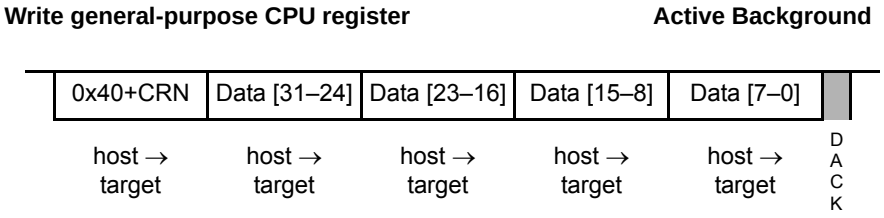
[1] Read: Anytime
Write: Once in normal, anytime in special mode

Table 2-2. MODRR0 Routing Register Field Descriptions

Field	Description
5 CAN0RR	**Module Routing Register** — CAN0 routing 1 RXCAN0 on PJ0; TXCAN0 on PJ1 0 RXCAN0 on PS0; TXCAN0 on PS2
4 IIC0RR	**Module Routing Register** — IIC0 routing 1 SDA0 on PT0; SCL0 on PT1 0 SDA0 on PJ0; SCL0 on PJ1

The hardware forces low-order address bits to zero longword accesses to ensure these accesses are on 0-modulo-size alignments. Byte alignment details are described in Section 5.4.5.2, “BDC Access Of Device Memory Mapped Resources”.

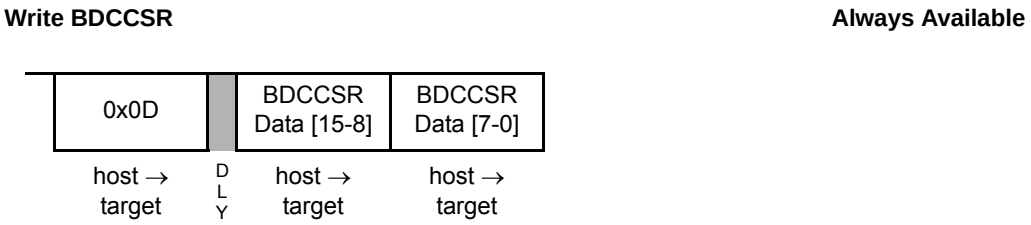
5.4.4.17 WRITE_Rn



If the device is in active BDM, this command writes the 32-bit operand to the selected CPU general-purpose register. See Section 5.4.5.1, “BDC Access Of CPU Registers for the CRN details. Accesses to CPU registers are always 32-bits wide, regardless of implemented register width. If enabled an ACK pulse is generated after the internal write access has been completed or aborted.

If the device is not in active BDM, this command is rejected as an illegal operation, the ILLCMD bit is set and no operation is performed.

5.4.4.18 WRITE_BDCCSR



16-bit write to the BDCCSR register. No ACK pulse is generated. Writing to this register can be used to configure control bits or clear flag bits. Refer to the register bit descriptions.

5.4.4.19 ERASE_FLASH

Mass erase the internal flash. This command can always be issued. On receiving this command twice in succession, the BDC sets the ERASE bit in BDCCSR and requests a flash mass erase. Any other BDC command following a single ERASE_FLASH initializes the sequence, such that thereafter the ERASE_FLASH must be applied twice in succession to request a mass erase. If 512 BDCSI clock cycles

NOTE

Register Address = Module Base Address + Address Offset, where the Module Base Address is defined at the MCU level and the Address Offset is defined at the module level.

Address Offset / Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 ECCSTAT	R	0	0	0	0	0	0	0	RDY
	W								
0x0001 ECCIE	R	0	0	0	0	0	0	0	SBEEIE
	W								
0x0002 ECCIF	R	0	0	0	0	0	0	0	SBEEIF
	W								
0x0003 - 0x0006 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0007 ECCDPTRH	R	DPTR[23:16]							
	W								
0x0008 ECCDPTRM	R	DPTR[15:8]							
	W								
0x0009 ECCDPTRL	R	DPTR[7:1]							0
	W								
0x000A - 0x000B Reserved	R	0	0	0	0	0	0	0	0
	W								
0x000C ECCDDH	R	DDATA[15:8]							
	W								
0x000D ECCDDL	R	DDATA[7:0]							
	W								
0x000E ECCDE	R	0	0	DECC[5:0]					
	W								
0x000F ECCDCMD	R	ECCDRR	0	0	0	0	0	ECCDW	ECCDR
	W								

= Unimplemented, Reserved, Read as zero

Figure 8-1. SRAM_ECC Register Summary

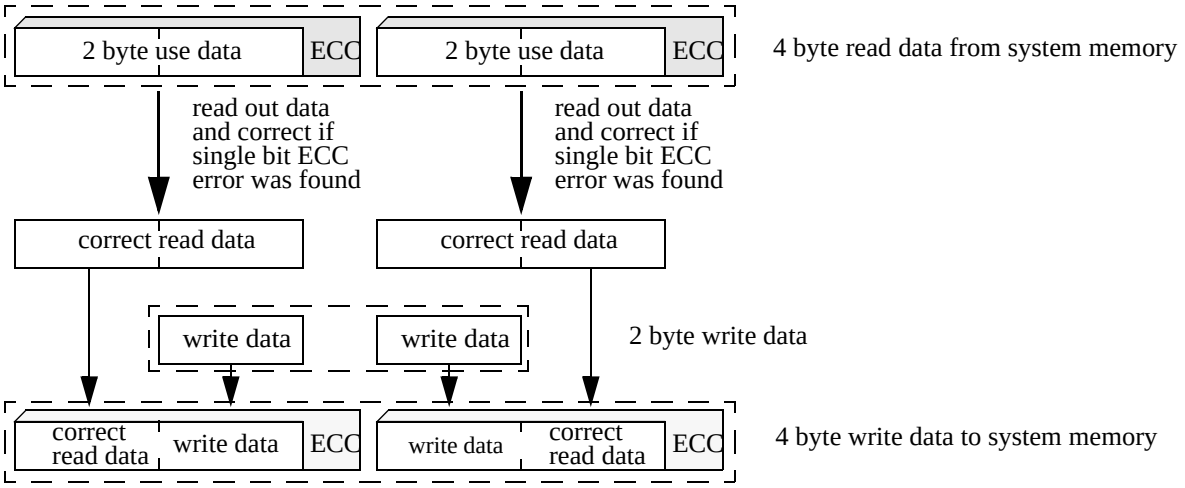


Figure 8-9. 2 byte non-aligned write access

8.3.3 Memory Read Access

During each memory read access an ECC check is performed. If the logic detects a single bit ECC error, then the module corrects the data, so that the access initiator module receives correct data. In parallel, the logic writes the corrected data back to the memory, so that this read access repairs the single bit ECC error. This automatic ECC read repair function is disabled by setting the ECCDRR bit.

If a single bit ECC error was detected, then the SBEEIF flag is set.

If the logic detects a double bit ECC error, then the data word is flagged as invalid, so that the access initiator module can ignore the data.

8.3.4 Memory Initialization

To avoid spurious ECC error reporting, memory operations that allow a read before a first write (like the read-modify-write operation of the non-aligned access) require that the memory contains valid ECC values before the first read-modify-write access is performed. The ECC module provides logic to initialize the complete memory content with zero during the power up phase. During the initialization process the access to the SRAM is disabled and the RDY status bit is cleared. If the initialization process is done, SRAM access is possible and the RDY status bit is set.

8.3.5 Interrupt Handling

This section describes the interrupts generated by the SRAM_ECC module and their individual sources. Vector addresses and interrupt priority are defined at the MCU level.

Table 9-23. Selectable Autonomous Periodical Interrupt Periods

APICLK	APIR[15:0]	Selected Period
0	0000	0.2 ms[1]
0	0001	0.4 ms[1]
0	0002	0.6 ms[1]
0	0003	0.8 ms[1]
0	0004	1.0 ms[1]
0	0005	1.2 ms[1]
0	.....	.....
0	FFFD	13106.8 ms[1]
0	FFFE	13107.0 ms[1]
0	FFFF	13107.2 ms[1]
1	0000	2 * Bus Clock period
1	0001	4 * Bus Clock period
1	0002	6 * Bus Clock period
1	0003	8 * Bus Clock period
1	0004	10 * Bus Clock period
1	0005	12 * Bus Clock period
1	.....	.....
1	FFFD	131068 * Bus Clock period
1	FFFE	131070 * Bus Clock period
1	FFFF	131072 * Bus Clock period

[1] When f_{ACLK} is trimmed to 20KHz.

Table 10-24. Analog Input Channel Select

CH_SEL[5]	CH_SEL[4]	CH_SEL[3]	CH_SEL[2]	CH_SEL[1]	CH_SEL[0]	Analog Input Channel
0	0	0	0	0	0	VRL_0/1 (V1, V2, see Table 10-2) VRL_0 (V3, see Table 10-2)
0	0	0	0	0	1	VRH_0/1 (V1, V2, see Table 10-2) VRH_0/1/2 (V3, see Table 10-2)
0	0	0	0	1	0	(VRH_0/1 + VRL_0/1) / 2 (V1, V2, see Table 10-2) (VRH_0/1/2 + VRL_0) / 2 (V3, see Table 10-2)
0	0	0	0	1	1	Reserved
0	0	0	1	0	0	Reserved
0	0	0	1	0	1	Reserved
0	0	0	1	1	0	Reserved
0	0	0	1	1	1	Reserved
0	0	1	0	0	0	Internal_0 (ADC temperature sense)
0	0	1	0	0	1	Internal_1
0	0	1	0	1	0	Internal_2
0	0	1	0	1	1	Internal_3
0	0	1	1	0	0	Internal_4
0	0	1	1	0	1	Internal_5
0	0	1	1	1	0	Internal_6
0	0	1	1	1	1	Internal_7
0	1	0	0	0	0	AN0
0	1	0	0	0	1	AN1
0	1	0	0	1	0	AN2
0	1	0	0	1	1	AN3
0	1	0	1	0	0	AN4
0	1	x	x	x	x	ANx
1	x	x	x	x	x	Reserved

NOTE

ANx in Table 10-24 is the maximum number of implemented analog input channels on the device. Please refer to the device overview of the reference manual for details regarding number of analog input channels.

[1] Read: Anytime
Write: Anytime when not in initialization mode, except RSTAT[1:0] and TSTAT[1:0] flags which are read-only; write of 1 clears flag; write of 0 is ignored

NOTE

The CANRFLG register is held in the reset state[1] when the initialization mode is active (INITRQ = 1 and INITAK = 1). This register is writable again as soon as the initialization mode is exited (INITRQ = 0 and INITAK = 0).

Table 13-11. CANRFLG Register Field Descriptions

Field	Description
7 WUPIF	**Wake-Up Interrupt Flag** — If the MSCAN detects CAN bus activity while in sleep mode (see Section 13.4.5.5, "MSCAN Sleep Mode,") and WUPE = 1 in CANTCTL0 (see Section 13.3.2.1, "MSCAN Control Register 0 (CANCTL0)"), the module will set WUPIF. If not masked, a wake-up interrupt is pending while this flag is set. 0 No wake-up activity observed while in sleep mode 1 MSCAN detected activity on the CAN bus and requested wake-up
6 CSCIF	**CAN Status Change Interrupt Flag** — This flag is set when the MSCAN changes its current CAN bus status due to the actual value of the transmit error counter (TEC) and the receive error counter (REC). An additional 4-bit (RSTAT[1:0], TSTAT[1:0]) status register, which is split into separate sections for TEC/REC, informs the system on the actual CAN bus status (see Section 13.3.2.6, "MSCAN Receiver Interrupt Enable Register (CANRIER)"). If not masked, an error interrupt is pending while this flag is set. CSCIF provides a blocking interrupt. That guarantees that the receiver/transmitter status bits (RSTAT/TSTAT) are only updated when no CAN status change interrupt is pending. If the TECs/RECs change their current value after the CSCIF is asserted, which would cause an additional state change in the RSTAT/TSTAT bits, these bits keep their status until the current CSCIF interrupt is cleared again. 0 No change in CAN bus status occurred since last interrupt 1 MSCAN changed current CAN bus status
5-4 RSTAT[1:0]	**Receiver Status Bits** — The values of the error counters control the actual CAN bus status of the MSCAN. As soon as the status change interrupt flag (CSCIF) is set, these bits indicate the appropriate receiver related CAN bus status of the MSCAN. The coding for the bits RSTAT1, RSTAT0 is: 00 RxOK: $0 \le$ receive error counter < 96 01 RxWRN: $96 \le$ receive error counter < 128 10 RxERR: $128 \le$ receive error counter *11 Bus-off[1]: 256 ≤ transmit error counter*
3-2 TSTAT[1:0]	**Transmitter Status Bits** — The values of the error counters control the actual CAN bus status of the MSCAN. As soon as the status change interrupt flag (CSCIF) is set, these bits indicate the appropriate transmitter related CAN bus status of the MSCAN. The coding for the bits TSTAT1, TSTAT0 is: 00 TxOK: $0 \le$ transmit error counter < 96 01 TxWRN: $96 \le$ transmit error counter < 128 10 TxERR: $128 \le$ transmit error counter < 256 11 Bus-Off: $256 \le$ transmit error counter

1. The RSTAT[1:0], TSTAT[1:0] bits are not affected by initialization mode.

18.4.5 Transmitter

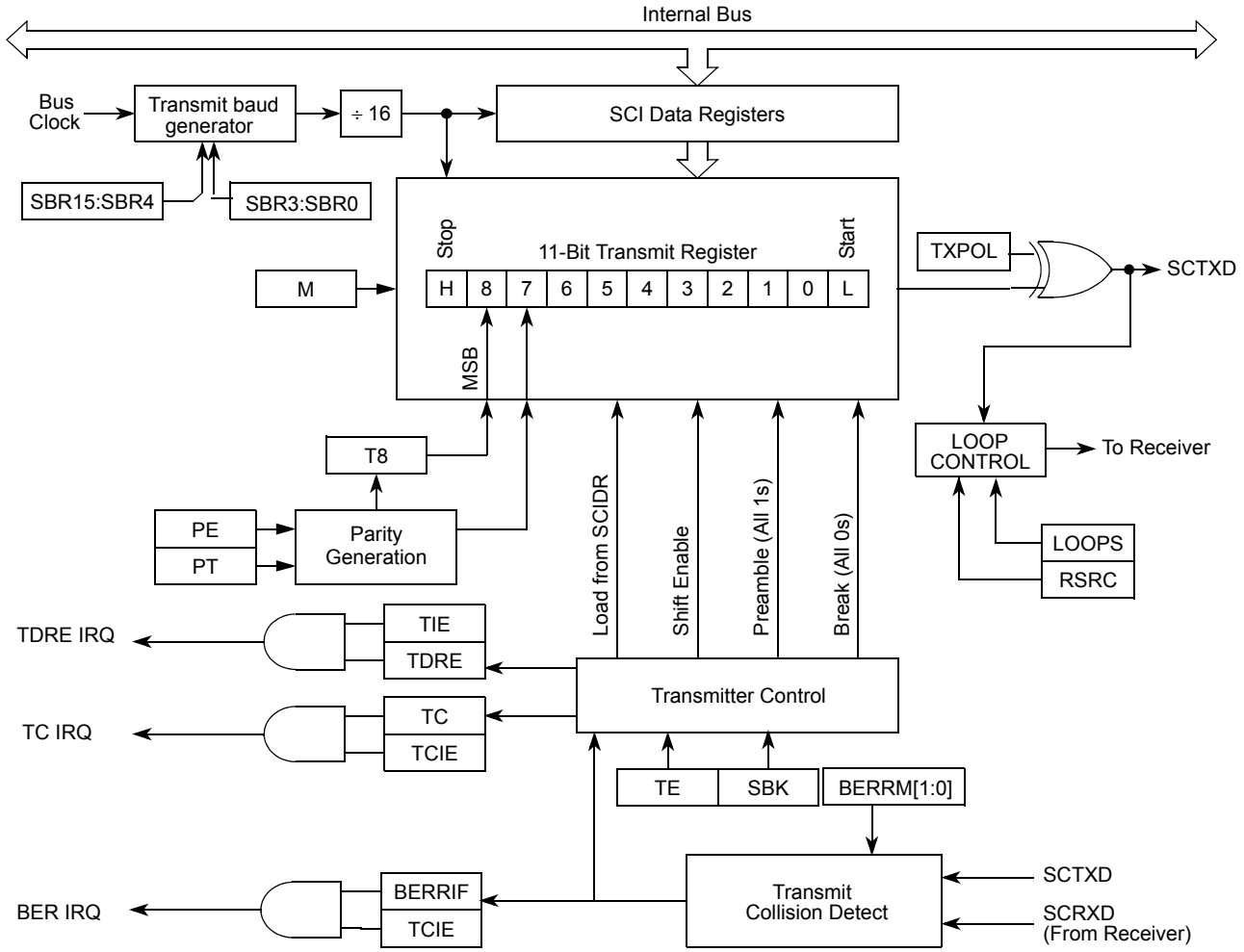


Figure 18-16. Transmitter Block Diagram

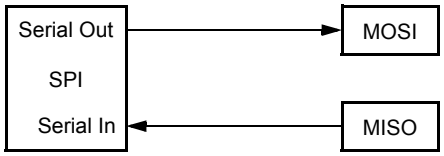
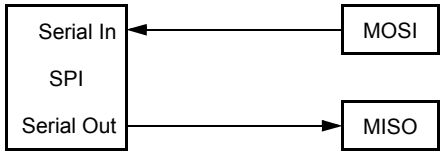
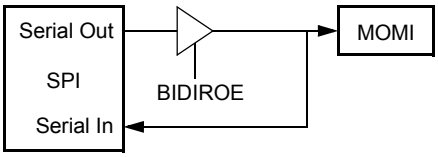
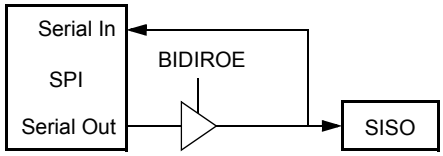
18.4.5.1 Transmitter Character Length

The SCI transmitter can accommodate either 8-bit or 9-bit data characters. The state of the M bit in SCI control register 1 (SCICR1) determines the length of data characters. When transmitting 9-bit data, bit T8 in SCI data register high (SCIDRH) is the ninth bit (bit 8).

18.4.5.2 Character Transmission

To transmit data, the MCU writes the data bits to the SCI data registers (SCIDRH/SCIDRL), which in turn are transferred to the transmitter shift register. The transmit shift register then shifts a frame out through the TXD pin, after it has prefaced them with a start bit and appended them with a stop bit. The SCI data registers (SCIDRH and SCIDRL) are the write-only buffers between the internal data bus and the transmit shift register.

Table 19-11. Normal Mode and Bidirectional Mode

When SPE = 1	Master Mode MSTR = 1	Slave Mode MSTR = 0
Normal Mode SPC0 = 0		
Bidirectional Mode SPC0 = 1		

The direction of each serial I/O pin depends on the BIDIROE bit. If the pin is configured as an output, serial data from the shift register is driven out on the pin. The same pin is also the serial input to the shift register.

- The SCK is output for the master mode and input for the slave mode.
- The $\overline{SS}$ is the input or output for the master mode, and it is always the input for the slave mode.
- The bidirectional mode does not affect SCK and $\overline{SS}$ functions.

NOTE

In bidirectional master mode, with mode fault enabled, both data pins MISO and MOSI can be occupied by the SPI, though MOSI is normally used for transmissions in bidirectional mode and MISO is not used by the SPI. If a mode fault occurs, the SPI is automatically switched to slave mode. In this case MISO becomes occupied by the SPI and MOSI is not used. This must be considered, if the MISO pin is used for another purpose.

19.4.6 Error Conditions

The SPI has one error condition:

- Mode fault error

19.4.6.1 Mode Fault Error

If the $\overline{SS}$ input becomes low while the SPI is configured as a master, it indicates a system error where more than one master may be trying to drive the MOSI and SCK lines simultaneously. This condition is not permitted in normal operation, the MODF bit in the SPI status register is set automatically, provided the MODFEN bit is set.

In the special case where the SPI is in master mode and MODFEN bit is cleared, the $\overline{SS}$ pin is not used by the SPI. In this special case, the mode fault error function is inhibited and MODF remains cleared. In case

Table 22-56. Valid Set User Margin Level Settings

FCCOB2	Level Description
0x0000	Return to Normal Level
0x0001	User Margin-1 Level[1]
0x0002	User Margin-0 Level[2]

1 Read margin to the erased state

2 Read margin to the programmed state

Table 22-57. Set User Margin Level Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command not available in current mode (see Table 22-28)
		Set if an invalid global address [23:0] is supplied see Table 22-2)
		Set if an invalid margin level setting is supplied
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

NOTE

User margin levels can be used to check that Flash memory contents have adequate margin for normal level read operations. If unexpected results are encountered when checking Flash memory contents at user margin levels, a potential loss of information has been detected.

22.4.7.13 Set Field Margin Level Command

The Set Field Margin Level command, valid in special modes only, causes the Memory Controller to set the margin level specified for future read operations of the P-Flash or EEPROM block.

Table 22-58. Set Field Margin Level Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x0E	Global address [23:16] to identify Flash block
FCCOB1	Global address [15:0] to identify Flash block	
FCCOB2	Margin level setting.	

Upon clearing CCIF to launch the Set Field Margin Level command, the Memory Controller will set the field margin level for the targeted block and then set the CCIF flag.

Table A-8. Thermal Package Characteristics for ZVL(S)32/16/8[1]

Num	Rating	Symbol	Min	Typ	Max	Unit
48LQFP						
1	Thermal resistance 48LQFP, single sided PCB[1] Natural Convection	θ_{JA}	—	80	—	°C/W
2	Thermal resistance 48LQFP, double sided PCB with 2 internal planes[2]. Natural Convection.	θ_{JA}	—	56	—	°C/W
3	Thermal resistance 48LQFP, single sided PCB[1] (@200 ft/min)	θ_{JA}	—	67	—	°C/W
4	Thermal resistance 48LQFP, double sided PCB with 2 internal planes[2] (@200 ft/min).	θ_{JA}	—	50	—	°C/W
5	Junction to Board 48LQFP[3]	θ_{JB}	—	34	—	°C/W
6	Junction to Case Top 48LQFP[4]	θ_{JCtop}	—	24	—	°C/W
7	Junction to Package Top 48LQFP[5]	Ψ_{JT}	—	6	—	°C/W
32LQFP						
8	Thermal resistance 32LQFP, single sided PCB[1] Natural Convection	θ_{JA}	—	84	—	°C/W
9	Thermal resistance 32LQFP, double sided PCB with 2 internal planes[2]. Natural Convection	θ_{JA}	—	56	—	°C/W
10	Thermal resistance 32LQFP, single sided PCB[1] (@200 ft/min)	θ_{JA}	—	71	—	°C/W
11	Thermal resistance 32LQFP, double sided PCB with 2 internal planes[2] (@200 ft/min).	θ_{JA}	—	49	—	°C/W
12	Junction to Board 32LQFP[3]	θ_{JB}	—	32	—	°C/W
13	Junction to Case Top 32LQFP[4]	θ_{JCtop}	—	23	—	°C/W
14	Junction to Package Top 32LQFP[5]	Ψ_{JT}	—	6	—	°C/W
32QFN-EP						
15	Thermal resistance 32QFN-EP, single sided PCB[1] Natural Convection	θ_{JA}	—	96	—	°C/W
16	Thermal resistance 32QFN-EP, double sided PCB with 2 internal planes[2]. Natural Convection	θ_{JA}	—	33	—	°C/W
17	Thermal resistance 32QFN-EP, single sided PCB[1] (@200 ft/min)	θ_{JA}	—	80	—	°C/W
18	Thermal resistance 32QFN-EP, double sided PCB with 2 internal planes[2] (@200 ft/min).	θ_{JA}	—	28	—	°C/W
19	Junction to Board 32QFN-EP[3]	θ_{JB}	—	13	—	°C/W
20	Junction to Case Top 32QFN-EP[4]	θ_{JCtop}	—	25	—	°C/W
21	Junction to Case Bottom 32QFN-EP[5]	$\theta_{JCbottom}$	—	2.22	—	°C/W
22	Junction to Package Top 32QFN-EP[5]	Ψ_{JT}	—	3	—	°C/W

[1] Junction to ambient thermal resistance, θ_{JA} was simulated to be equivalent to JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.

Table B-1. Voltage Regulator Electrical Characteristics

-40°C ≤T_J ≤ 175°C unless noted otherwise, V_{DDA} and V_{DDX} must be shorted on the application board.						
Num	**Characteristic**	**Symbol**	**Min**	**Typical**	**Max**	**Unit**
VDDX=3.3V, VREG5VEN = 1'b0, ZVL(A)128/96/64 only						
6a	Output Voltage V_{DDX}, with external PNP Full Performance Mode V_{SUP} >5.5V[1] Full Performance Mode V_{SUP} >5.5V[4] Full Performance Mode 3.5V <= V_{SUP} <=5.5V Reduced Performance Mode (stopmode) V_{SUP} > =3.5V	V_{DDX}	 3.2 3.23 3.13 2.2	 3.3 3.3 - 3.3	 3.39 3.36 3.39 3.6	V
6b	Output Voltage V_{DDX}, without PNP Full Performance Mode V_{SUP} >5.5V[1] Full Performance Mode V_{SUP} >5.5V[4] Full Performance Mode 3.5V <= V_{SUP} <=5.5V Reduced Performance Mode (stopmode) V_{SUP} > =3.5V	V_{DDX}	 3.18 3.21 3.13 2.2	 3.28 3.28 - 3.3	 3.37 3.35 3.37 3.6	V
7	Load Current V_{DDX}[2,3] without external PNP Full Performance Mode V_{SUP} > 5.5V Full Performance Mode 3.5V <= V_{SUP} <=5.5V Reduced Performance Mode (stopmode)	I_{DDX}	 0 0 0	 - - -	 70 25 5	mA
8	Short Circuit V_{DDX} fall back current V_{DDX} <= 0.5V	I_{DDX}	—	100	—	mA
9	Low Voltage Interrupt Assert Level[5] Low Voltage Interrupt Deassert Level	V_{LVIA} V_{LVID}	4.04 4.19	4.23 4.38	4.40 4.49	V
10a	V_{DDX} Low Voltage Reset deassert[6]	V_{LVRXD}	—	—	3.13	V
10b	V_{DDX} Low Voltage Reset assert	V_{LVRXA}	2.95	3.02	—	V
11	Trimmed ACLK output frequency[7]	f_{ACLK}	—	20	—	KHz
12	Trimmed ACLK internal clock Δf / $f_{nominal}$ [8]	df_{ACLK}	- 6%	—	+ 6%	—
13	The first period after enabling the counter by APIFE might be reduced by API start up delay	t_{sdel}	—	—	100	µs
14	Temperature Sensor Slope	dV_{HT}	5.05	5.25	5.45	mV/°C
15	Temperature Sensor Output Voltage (T_j=150°C)	V_{HT}	—	2.4	—	V
16	High Temperature Interrupt Assert[9] High Temperature Interrupt Deassert	T_{HTIA} T_{HTID}	120 110	132 122	144 134	°C °C
17	Bandgap output voltage	V_{BG}	1.14	1.20	1.28	V
18	V_{BG} voltage variation over input voltage V_{SUP} 3.5V ≤ V_{SUP} ≤ 18V, T_J = 125°C	Δ_{VBGV}	-5		5	mV

Appendix E
NVM Electrical Parameters

E.1 NVM Timing Parameters

The time base for all NVM program or erase operations is derived from the bus clock using the FCLKDIV register. The frequency of this derived clock must be set within the limits specified as f_{NVMOP}. The NVM module does not have any means to monitor the frequency and will not prevent program or erase operation at frequencies above or below the specified minimum. When attempting to program or erase the NVM module at a lower frequency, a full program or erase transition is not assured.

The device bus frequency f_{WSTAT}, below which the flash wait states can be disabled, is specified in the device operating conditions Table A-6.

The following sections provide equations which can be used to determine the time required to execute specific flash commands. All timing parameters are a function of the bus clock frequency, f_{NVMBUS}. All program and erase times are also a function of the NVM operating frequency, f_{NVMOP}. A summary of key timing parameters can be found in Table E-1 and Table E-2.

Table E-2. NVM Timing Characteristics ZVL(A)128/96/64

Num	Command	f_{NVMOP} cycle	f_{NVMBUS} cycle	Symbol	Min[1]	Typ[2]	Max[3]	Lfmax[4]	Unit
1	Bus frequency	1	—	f_{NVMBUS}	1	32	32		MHz
2	NVM Operating frequency	—	1	f_{NVMOP}	0.8	1	1.05		MHz
3	Erase Verify All Blocks[5,6]	0	34528	t_{RD1ALL}	1.08	1.08	2.16	69.06	ms
4	Erase Verify Block (Pflash)[5]	0	33323	t_{RD1BLK_P}	1.04	1.04	2.08	66.65	ms
5	Erase Verify Block (EEPROM)[6]	0	1591	t_{RD1BLK_D}	0.05	0.05	0.10	3.18	ms
6	Erase Verify P-Flash Section	0	508	t_{RD1SEC}	0.02	0.02	0.03	1.02	ms
7	Read Once	0	481	t_{RDONCE}	15.03	15.03	15.03	481.00	us
8	Program P-Flash (4 Word)	164	3133	t_{PGM_4}	0.25	0.26	0.56	12.74	ms
9	Program Once	164	3107	$t_{PGMONCE}$	0.25	0.26	0.26	3.31	ms
10	Erase All Blocks[5,6]	100066	34991	t_{ERSALL}	96.39	101.16	102.25	195.06	ms
11	Erase Flash Block (Pflash)[5]	100060	33692	t_{ERSBLK_P}	96.35	101.11	102.17	192.46	ms
12	Erase Flash Block (EEPROM)[6]	100060	1930	t_{ERSBLK_D}	95.36	100.12	100.18	128.94	ms
13	Erase P-Flash Sector	20015	924	t_{ERSPG}	19.09	20.04	20.07	26.87	ms
14	Unsecure Flash	100066	35069	t_{UNSECU}	96.40	101.16	102.26	195.22	ms
15	Verify Backdoor Access Key	0	493	t_{VFYKEY}	15.41	15.41	15.41	493.00	us
16	Set User Margin Level	0	436	t_{MLOADU}	13.63	13.63	13.63	436.00	us
17	Set Factory Margin Level	0	445	t_{MLOADF}	13.91	13.91	13.91	445.00	us
18	Erase Verify EEPROM Section	0	583	$t_{DRD1SEC}$	0.02	0.02	0.04	1.17	ms
19	Program EEPROM (1 Word)	68	1678	t_{DPGM_1}	0.12	0.12	0.28	6.80	ms
20	Program EEPROM (2 Word)	136	2702	t_{DPGM_2}	0.21	0.22	0.47	10.98	ms
21	Program EEPROM (3 Word)	204	3726	t_{DPGM_3}	0.31	0.32	0.67	15.16	ms
22	Program EEPROM (4 Word)	272	4750	t_{DPGM_4}	0.41	0.42	0.87	19.34	ms
23	Erase EEPROM Sector	5015	817	t_{DERSPG}	4.80	5.04	20.49	38.96	ms
24	Protection Override	0	475	$t_{PRTOVRD}$	14.84	14.84	14.84	475.00	us

1 Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}

2 Typical times are based on typical f_{NVMOP} and typical f_{NVMBUS}

3 Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging

4 Lowest-frequency max times are based on minimum f_{NVMOP} and minimum f_{NVMBUS} plus aging

5 Affected by Pflash size

6 Affected by EEPROM size

E.2 NVM Reliability Parameters

The reliability of the NVM blocks is guaranteed by stress test during qualification, constant process monitors and burn-in to screen early life failures.

Appendix J
PIM Electrical Specifications

J.1 High-Voltage Inputs (HVI) Electrical Characteristics

Table J-1. Static Electrical Characteristics - High Voltage Input Pins - Port L

Characteristics are $5.5V \le V_{SUP} \le 18V$, $-40°C \le T_J \le 175°C$[1] unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25°C$[2] under nominal conditions unless otherwise noted.						
Num	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	Digital Input Threshold • $V_{SUP} > 6.5V$, V_{DDX}=5V selected • $5.5V \le V_{SUP} \le 6.5V$, V_{DDX}=5V selected • $V_{SUP} > 5.5V$, V_{DDX}=3.3V selected	V_{TH_HVI}	 2.8 2.0 0.8	 3.5 2.5 1.8	 4.5 3.8 2.7	 V V V
2	Input Hysteresis	V_{HYS_HVI}	_	250	_	mV
3	Pin Input Divider Ratio with external series R_{EXT_HVI} Ratio = V_{HVI} / $V_{Internal(ADC)}$	 $Ratio_{L\_HVI}$ $Ratio_{H\_HVI}$ $Ratio_{12\_HVI}$	 – – –	 2 6 12	 – – –	
4	Analog Input Matching Absolute Error on V_{ADC}[3] • Compared to V_{HVI} / $Ratio_{L\_HVI}$ ($1V < V_{HVI} < 7V$), V_{DDX}=5V selected ($1V < V_{HVI} < 2.8V$), V_{DDX}=3.3V selected • Compared to V_{HVI} / $Ratio_{H\_HVI}$ ($3V < V_{HVI} < 21V$), V_{DDX}=5V selected ($5V < V_{HVI} < 18V$), V_{DDX}=5V selected ($3V < V_{HVI} < 8.4V$), V_{DDX}=3.3V selected • Compared to V_{HVI} / $Ratio_{12\_HVI}$ ($6V < V_{HVI} < 28V$), V_{DDX}=5V selected ($6V < V_{HVI} < 14.8V$), V_{DDX}=3.3V selected • Direct Mode (PTADIRL=1) ($0.5V < V_{HVI} < 3.5V$),V_{DDX}=5V selected ($0.5V < V_{HVI} < 1.4V$),V_{DDX}=3.3V selected	 AIM_{L_HVI} AIM_{H_HVI} AIM_{12_HVI} AIM_{D_HVI} 	 – – – – – – – – –	 ± 2 ± 3 ± 2 ± 2 ± 3 ± 3 ± 3 ± 2 ± 2	 ± 5 ± 7 ± 5 ± 3 ± 7 ± 7 ± 7 ± 5 ± 5	 % % % % % % % % %
5	High Voltage Input Series Resistor **Note:** Always required externally at HVI pins.	R_{EXT_HVI}	–	10	–	kΩ
6	Enable Uncertainty Time	t_{UNC_HVI}	–	1	–	µs
7	Input capacitance	C_{IN_HVI}	–	8	–	pF
8	Current Injection	I_{IC_HVI}	see Footnote[4]			–

1 T_J: Junction Temperature

2 T_A: Ambient Temperature

3 Outside of the given V_{HVI} range the error is significant. The ratio can be changed, if outside of the given range

O.11 0x05C0-0x05FF TIM0 (continued)

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x05D7	TIM0TC3L	R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05D8	TIM0TC4H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x05D9	TIM0TC4L	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x05DA	TIM0TC5H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x05DB	TIM0TC5L	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x05DC– 0x05EB	Reserved	R W								
0x05EC	TIM0OCPD	R W	RESERVED	RESERVED	OCPD5	OCPD4	OCPD3	OCPD2	OCPD1	OCPD0
0x05ED	Reserved	R W								
0x05EE	TIM0PTPSR	R W	PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0
0x05EF	Reserved	R W								

O.12 0x0600-0x063F ADC0

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0600	ADC0CTL_0	R W	ADC_EN	ADC_SR	FRZ_MOD	SWAI	ACC_CFG[1:0]		STR_SEQA	MOD_CFG
0x0601	ADC0CTL_1	R W	CSL_BMOD	RVL_BMOD	SMOD_ACC	AUT_RSTA	0	0	0	0
0x0602	ADC0STS	R W	CSL_SEL	RVL_SEL	DBECC_ERR	Reserved	READY	0	0	0
0x0603	ADC0TIM	R W	0	PRS[6:0]						
0x0604	ADC0FMT	R W	DJM	0	0	0	0	SRES[2:0]		
0x0605	ADC0FLWCTL	R W	SEQA	TRIG	RSTA	LDOK	0	0	0	0
0x0606	ADC0EIE	R W	IA_EIE	CMD_EIE	EOL_EIE	Reserved	TRIG_EIE	RSTAR_EIE	LDOK_EIE	0
0x0607	ADC0IE	R W	SEQAD_IE	CONIF_OIE	Reserved	0	0	0	0	0