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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SCI, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	19
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	5.5V ~ 18V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount, Wettable Flank
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN-EP (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvl64f0mfmr

Chapter 6
Interrupt (S12ZINTV0)

Chapter 7
S12Z DebugLite (S12ZDBGV3)

in system wait mode. For further power consumption the peripherals can individually turn off their local clocks. Asserting $\overline{\text{RESET}}$, $\overline{\text{XIRQ}}$, $\overline{\text{IRQ}}$, or any other interrupt that is not masked, either locally or globally by a CCR bit, ends system wait mode.

- Static power modes:
  Static power (Stop) modes are entered following the CPU STOP instruction unless an NVM command is active. When no NVM commands are active, the Stop request is acknowledged and the device enters either Stop or Pseudo Stop mode.
  - Pseudo-stop: In this mode the system clocks are stopped but the oscillator is still running and the real time interrupt (RTI), watchdog (COP) and Autonomous Periodic Interrupt (API) may be enabled. Other peripherals are turned off. This mode consumes more current than system STOP mode but, as the oscillator continues to run, the full speed wake up time from this mode is significantly shorter.
  - Stop: In this mode the oscillator is stopped and clocks are switched off. The counters and dividers remain frozen. The autonomous periodic interrupt (API) may remain active but has a very low power consumption. If the BDC is enabled in Stop mode, the VREG remains in full performance mode and the CPMU continues operation as in run mode. With BDC enabled and BDCCIS bit set, then all clocks remain active to allow BDC access to internal peripherals. If the BDC is enabled and BDCCIS is clear, then the BDCSI clock remains active, but bus and core clocks are disabled.

1.11 Security

The MCU security mechanism prevents unauthorized access to the flash memory. It must be emphasized that part of the security must lie with the application code. An extreme example would be application code that dumps the contents of the internal memory. This would defeat the purpose of security. Also, if an application has the capability of downloading code through a serial port and then executing that code (e.g. an application containing bootloader code), then this capability could potentially be used to read the EEPROM and Flash memory contents even when the microcontroller is in the secure state. In this example, the security of the application could be enhanced by requiring a response authentication before any code can be downloaded.

Device security details are also described in the flash block description.

1.11.1 Features

The security features of the S12Z chip family are:

- Prevent external access of the non-volatile memories (Flash, EEPROM) content
- Restrict execution of NVM commands

1.11.2 Securing the Microcontroller

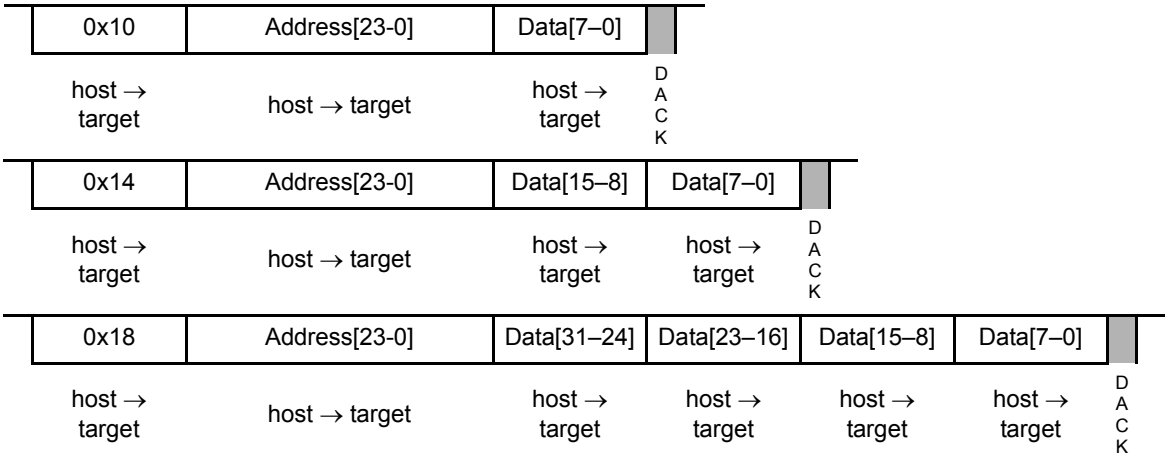
The chip can be secured by programming the security bits located in the options/security byte in the Flash memory array. These non-volatile bits keep the device secured through reset and power-down.

returns the address of the next instruction to be executed on returning from active BDM. Thus following a write to the PC in active BDM, a SYNC_PC returns that written value.

5.4.4.16 WRITE_MEM.sz, WRITE_MEM.sz_WS

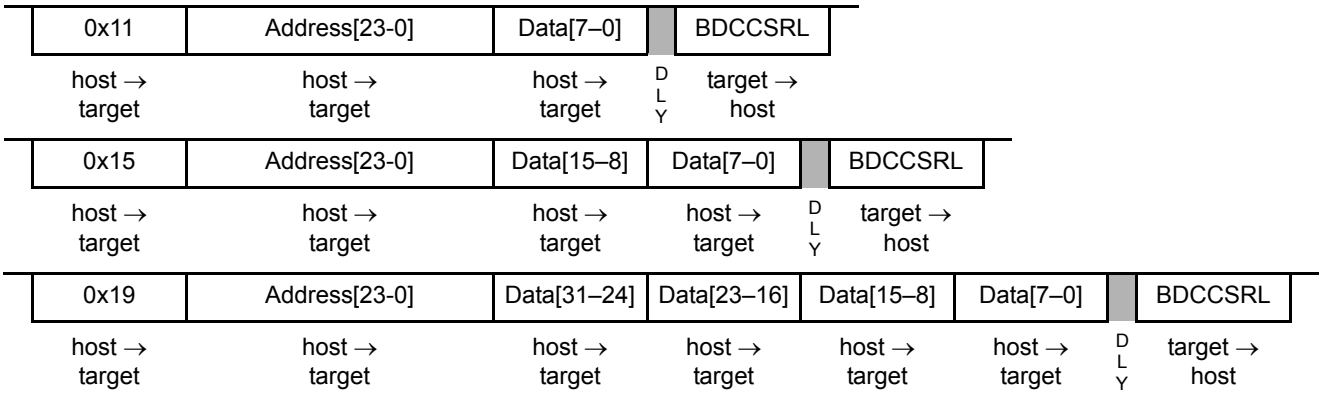
WRITE_MEM.sz

Write memory at the specified address **Non-intrusive**



WRITE_MEM.sz_WS

Write memory at the specified address with status **Non-intrusive**



Write data to the specified memory address. The address is transmitted as three 8-bit packets (msb to lsb) immediately after the command.

If the with-status option is specified, the status byte contained in BDCCSRL is returned after the write data. This status byte reflects the state after the memory write was performed. The examples show the WRITE_MEM.B{_WS}, WRITE_MEM.W{_WS}, and WRITE_MEM.L{_WS} commands. If enabled an ACK pulse is generated after the internal write access has been completed or aborted.

Table 5-10. Field Location to Byte Access Mapping

Address[1:0]	Access Size	00	01	10	11	Note
00	32-bit	Data[31:24]	Data[23:16]	Data [15:8]	Data [7:0]	
01	32-bit	Data[31:24]	Data[23:16]	Data [15:8]	Data [7:0]	Realigned
10	32-bit	Data[31:24]	Data[23:16]	Data [15:8]	Data [7:0]	Realigned
11	32-bit	Data[31:24]	Data[23:16]	Data [15:8]	Data [7:0]	Realigned
00	16-bit	Data [15:8]	Data [7:0]			
01	16-bit		Data [15:8]	Data [7:0]		
10	16-bit			Data [15:8]	Data [7:0]	
11	16-bit			Data [15:8]	Data [7:0]	Realigned
00	8-bit	Data [7:0]				
01	8-bit		Data [7:0]			
10	8-bit			Data [7:0]		
11	8-bit				Data [7:0]	
			Denotes byte that is not transmitted			

5.4.5.2.1 FILL_MEM and DUMP_MEM Increments and Alignment

FILL_MEM and DUMP_MEM increment the previously accessed address by the previous access size to calculate the address of the current access. On misaligned longword accesses, the address bits [1:0] are forced to zero, therefore the following FILL_MEM or DUMP_MEM increment to the first address in the next 4-byte field. This is shown in Table 5-11, the address of the first DUMP_MEM.32 following READ_MEM.32 being calculated from 0x004000+4.

When misaligned word accesses are realigned, then the original address (not the realigned address) is incremented for the following FILL_MEM, DUMP_MEM command.

Misaligned word accesses can cause the same locations to be read twice as shown in rows 6 and 7. The hardware ensures alignment at an attempted misaligned word access across a 4-byte boundary, as shown in row 7. The following word access in row 8 continues from the realigned address of row 7.

Table 5-11. Consecutive Accesses With Variable Size

Row	Command	Address	Address[1:0]	00	01	10	11
1	READ_MEM.32	0x004003	11	Accessed	Accessed	Accessed	Accessed
2	DUMP_MEM.32	0x004004	00	Accessed	Accessed	Accessed	Accessed
3	DUMP_MEM.16	0x004008	00	Accessed	Accessed		
4	DUMP_MEM.16	0x00400A	10			Accessed	Accessed
5	DUMP_MEM.08	0x00400C	00	Accessed			
6	DUMP_MEM.16	0x00400D	01		Accessed	Accessed	
7	DUMP_MEM.16	0x00400E	10			Accessed	Accessed
8	DUMP_MEM.16	0x004010	01	Accessed	Accessed		

Table 9-34. Reset Summary

Reset Source	Local Enable
Oscillator Clock Monitor Reset	OSCE Bit in CPMUOSC register and OMRE Bit in CPMUOSC2 register
COP Reset	CR[2:0] in CPMUCOP register

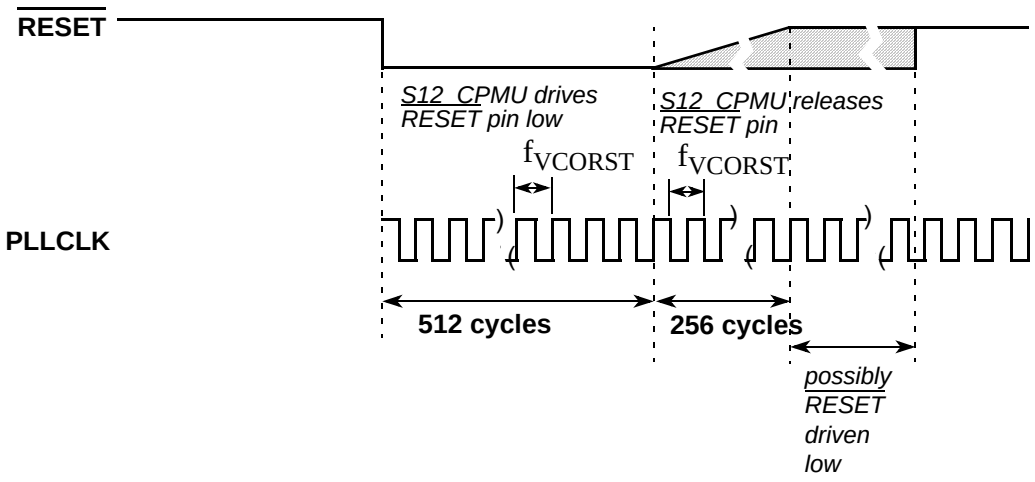
9.5.2 Description of Reset Operation

Upon detection of any reset of Table 9-34, an internal circuit drives the $\overline{\text{RESET}}$ pin low for 512 PLLCLK cycles. After 512 PLLCLK cycles the $\overline{\text{RESET}}$ pin is released. The internal reset of the MCU remains asserted while the reset generator completes the 768 PLLCLK cycles long reset sequence.In case the $\overline{\text{RESET}}$ pin is externally driven low for more than these 768 PLLCLK cycles (External Reset), the internal reset remains asserted longer.

NOTE

While System Reset is asserted the PLLCLK runs with the frequency f_{VCORST}.

Figure 9-42. RESET Timing



9.5.3 Oscillator Clock Monitor Reset

If the external oscillator is enabled (OSCE=1)and the oscillator clock monitor reset is enabled (OMRE=1), then in case of loss of oscillation or the oscillator frequency drops below the failure assert frequency f_{CMFA} (see device electrical characteristics for values), the S12CPMU_UHV generates an Oscillator Clock Monitor Reset. In Full Stop Mode the external oscillator and the oscillator clock monitor are disabled.

10.3 Key Features

- Programmer’s Model with List Based Architecture for conversion command and result value organization
- Selectable resolution of 8-bit, 10-bit, or 12-bit
- Channel select control for n external analog input channels
- Provides up to eight device internal channels (please see the device reference manual for connectivity information and Figure 10-2)
- Programmable sample time
- A sample buffer amplifier for channel sampling (improved performance in view to influence of channel input path resistance versus conversion accuracy)
- Left/right justified result data
- Individual selectable VRH_0/1 and VRL_0/1 inputs (ADC12B_LBA V1 and V2) or VRH_0/1/2 inputs (ADC12B_LBA V3) on a conversion command basis (please see Figure 10-2, Table 10-2)
- Special conversions for selected VRH_0/1 (V1 and V2) or VRH_0/1/2 (V3), VRL_0/1 (V1 and V2) or VRL_0 (V3), (VRL_0/1 + VRH_0/1) / 2 (V1 and V2) or (VRL_0 + VRH_0/1/2) / 2 (V3) (please see Table 10-2)
- 15 conversion interrupts with flexible interrupt organization per conversion result
- One dedicated interrupt for “End Of List” type commands
- Command Sequence List (CSL) with a maximum number of 64 command entries
- Provides conversion sequence abort
- Restart from top of active Command Sequence List (CSL)
- The Command Sequence List and Result Value List are implemented in double buffered manner (two lists in parallel for each function)
- Conversion Command (CSL) loading possible from System RAM or NVM
- Single conversion flow control register with software selectable access path
- Two conversion flow control modes optimized to different application use cases
- Four option bits in the conversion command for top level SoC specific feature/function implementation option (Please refer to the device reference manual for details of the top level feature/function if implemented)

10.5.2.7 ADC Error Interrupt Enable Register (ADCEIE)

Module Base + 0x0006

	7	6	5	4	3	2	1	0
R	IA_EIE	CMD_EIE	EOL_EIE	Reserved	TRIG_EIE	RSTAR_EIE	LDOK_EIE	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 10-10. ADC Error Interrupt Enable Register (ADCEIE)

Read: Anytime

Write: Anytime

Table 10-12. ADCEIE Field Descriptions

Field	Description
7 IA_EIE	**Illegal Access Error Interrupt Enable Bit** — This bit enables the illegal access error interrupt. 0 Illegal access error interrupt disabled. 1 Illegal access error interrupt enabled.
6 CMD_EIE	**Command Value Error Interrupt Enable Bit** — This bit enables the command value error interrupt. 0 Command value interrupt disabled. 1 Command value interrupt enabled.
5 EOL_EIE	**"End Of List" Error Interrupt Enable Bit** — This bit enables the "End Of List" error interrupt. 0 "End Of List" error interrupt disabled. 1 "End Of List" error interrupt enabled.
3 TRIG_EIE	**Conversion Sequence Trigger Error Interrupt Enable Bit** — This bit enables the conversion sequence trigger error interrupt. 0 Conversion sequence trigger error interrupt disabled. 1 Conversion sequence trigger error interrupt enabled.
2 RSTAR_EIE	**Restart Request Error Interrupt Enable Bit**— This bit enables the restart request error interrupt. 0 Restart Request error interrupt disabled. 1 Restart Request error interrupt enabled.
1 LDOK_EIE	**Load OK Error Interrupt Enable Bit** — This bit enables the Load OK error interrupt. 0 Load OK error interrupt disabled. 1 Load OK error interrupt enabled.

Table 10-22. Conversion Interrupt Flag Select

CON_IF[15:1]	INTFLG_SEL[3]	INTFLG_SEL[2]	INTFLG_SEL[1]	INTFLG_SEL[0]	Comment
0x0000	0	0	0	0	No flag set
0x0001	0	0	0	1	Only one flag can be set (one hot coding)
0x0002	0	0	1	0	
0x0004	0	0	1	1	
0x0008	0	1	0	0	
0x0010	0	1	0	1	
....	...	...	...	...	
0x0800	1	1	0	0	
0x1000	1	1	0	1	
0x2000	1	1	1	0	
0x4000	1	1	1	1	

mode “Trigger Mode” only a Restart Event is necessary if ADC is idle to restart Conversion Sequence List execution (the Trigger Event occurs automatically).

It is possible to set bit RSTA and SEQA simultaneously, causing a Sequence Abort Event followed by a Restart Event. In this case the error flags behave differently depending on the selected conversion flow control mode:

- Setting both flow control bits simultaneously in conversion flow control mode “Restart Mode” prevents the error flags RSTA_EIF and LDOK_EIF from occurring.
- Setting both flow control bits simultaneously in conversion flow control mode “Trigger Mode” prevents the error flag RSTA_EIF from occurring.

If only a Restart Event occurs while ADC is not idle and bit SEQA is not set already (Sequence Abort Event in progress) a Sequence Abort Event is issued automatically and bit RSTAR_EIF is set.

Please see also the detailed conversion flow control bit mandatory requirements and execution information for bit RSTA and SEQA described in Section 10.6.3.2.5, “The four ADC conversion flow control bits.

10.9.7.3 Restart CSL execution with new/other CSL (alternative CSL becomes active CSL) — CSL swapping

After all alternative conversion command list entries are finished the bit LDOK can be set simultaneously with the next Restart Event to swap command buffers.

To start conversion command list execution it is mandatory that the ADC is idle (no conversion or conversion sequence is ongoing).

If necessary, a possible ongoing conversion sequence can be aborted by the Sequence Abort Event (setting bit SEQA). As soon as bit SEQA is cleared by the ADC, the current conversion sequence has been aborted and the ADC is idle (no conversion sequence or conversion ongoing).

After a conversion sequence abort is executed it is mandatory to request a Restart Event (bit RSTA set) and simultaneously set bit LDOK to swap the CSL buffer. After the Restart Event is finished (bit RSTA and LDOK are cleared), the ADC accepts a new Trigger Event (bit TRIG can be set) and begins conversion from the top of the newly selected CSL buffer. In conversion flow control mode “Trigger Mode” only a Restart Event (simultaneously with bit LDOK being set) is necessary to restart conversion command list execution with the newly selected CSL buffer (the Trigger Event occurs automatically).

It is possible to set bits RSTA, LDOK and SEQA simultaneously, causing a Sequence Abort Event followed by a Restart Event. In this case the error flags behave differently depending on the selected conversion flow control mode:

- Setting these three flow control bits simultaneously in “Restart Mode” prevents the error flags RSTA_EIF and LDOK_EIF from occurring.
- Setting these three flow control bits simultaneously in “Trigger Mode” prevents the error flag RSTA_EIF from occurring.

If only a Restart Event occurs while ADC is not idle and bit SEQA is not set already (Sequence Abort Event in progress) a Sequence Abort Event is issued automatically and bit RSTAR_EIF is set.

11.4.2.2 Analog Output Voltage Level Register (DACVOL)

Module Base + 0x0002 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	VOLTAGE[7:0]							
Reset	0	0	0	0	0	0	0	0

Figure 11-4. Analog Output Voltage Level Register (DACVOL)

1 Read: Anytime
Write: Anytime

Table 11-4. DACVOL Field Description

Field	Description
7:0 VOLTAGE[7:0]	**VOLTAGE** — This register defines (together with the FVR bit) the analog output voltage. For more detail see Equation 11-1 and Equation 11-2.

11.4.2.3 Reserved Register

Module Base + 0x0007 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
W								
Reset	0	0	0	0	0	0	0	0

Figure 11-5. Reserved Registerfv_dac_8b5v_RESERVED

1 Read: Anytime
Write: Only in special mode

NOTE

This reserved register bits are designed for factory test purposes only and are not intended for general user access. Writing to this register when in special modes can alter the modules functionality.

The comparator outputs BVLC and BVHC are forced to zero if the comparator is disabled (configuration bit BSUSE is cleared). If the software disables the comparator during a high or low Voltage condition (BVHC or BVLC active), then an additional interrupt is generated. To avoid this behavior the software must disable the interrupt generation before disabling the comparator.

The BATS interrupt vector is named in Table 14-6. Vector addresses and interrupt priorities are defined at MCU level.

The module internal interrupt sources are combined into one module interrupt signal.

Table 14-6. BATSV3 Interrupt Sources

Module Interrupt Source	Module Internal Interrupt Source	Local Enable
BATSV3 Interrupt (BATI)	BATS Voltage Low Condition Interrupt (BVLI)	BVLIE = 1
	BATS Voltage High Condition Interrupt (BVHI)	BVHIE = 1

14.4.2.1 BATS Voltage Low Condition Interrupt (BVLI)

To use the Voltage Low Interrupt the Level Sensing must be enabled (BSUSE =1).

If measured when

a) V_{LBI1} selected with BVLS[1:0] = 0x0
$V_{measure} < V_{LBI1\_A}$ (falling edge) or $V_{measure} < V_{LBI1\_D}$ (rising edge)

or when

b) V_{LBI2} selected with BVLS[1:0] = 0x1 at pin VSUP
$V_{measure} < V_{LBI2\_A}$ (falling edge) or $V_{measure} < V_{LBI2\_D}$ (rising edge)

or when

c) V_{LBI3} selected with BVLS[1:0] = 0x2
$V_{measure} < V_{LBI3\_A}$ (falling edge) or $V_{measure} < V_{LBI3\_D}$ (rising edge)

or when

d) V_{LBI4} selected with BVLS[1:0] = 0x3
$V_{measure} < V_{LBI4\_A}$ (falling edge) or $V_{measure} < V_{LBI4\_D}$ (rising edge)

then BVLC is set. BVLC status bit indicates that a low voltage at pin VSUP is present. The Low Voltage Interrupt flag (BVLIF) is set to 1 when the Voltage Low Condition (BVLC) changes state . The Interrupt flag BVLIF can only be cleared by writing a 1. If the interrupt is enabled by bit BVLIE the module requests an interrupt to MCU (BATI).

14.4.2.2 BATS Voltage High Condition Interrupt (BVHI)

To use the Voltage High Interrupt the Level Sensing must be enabled (BSUSE=1).

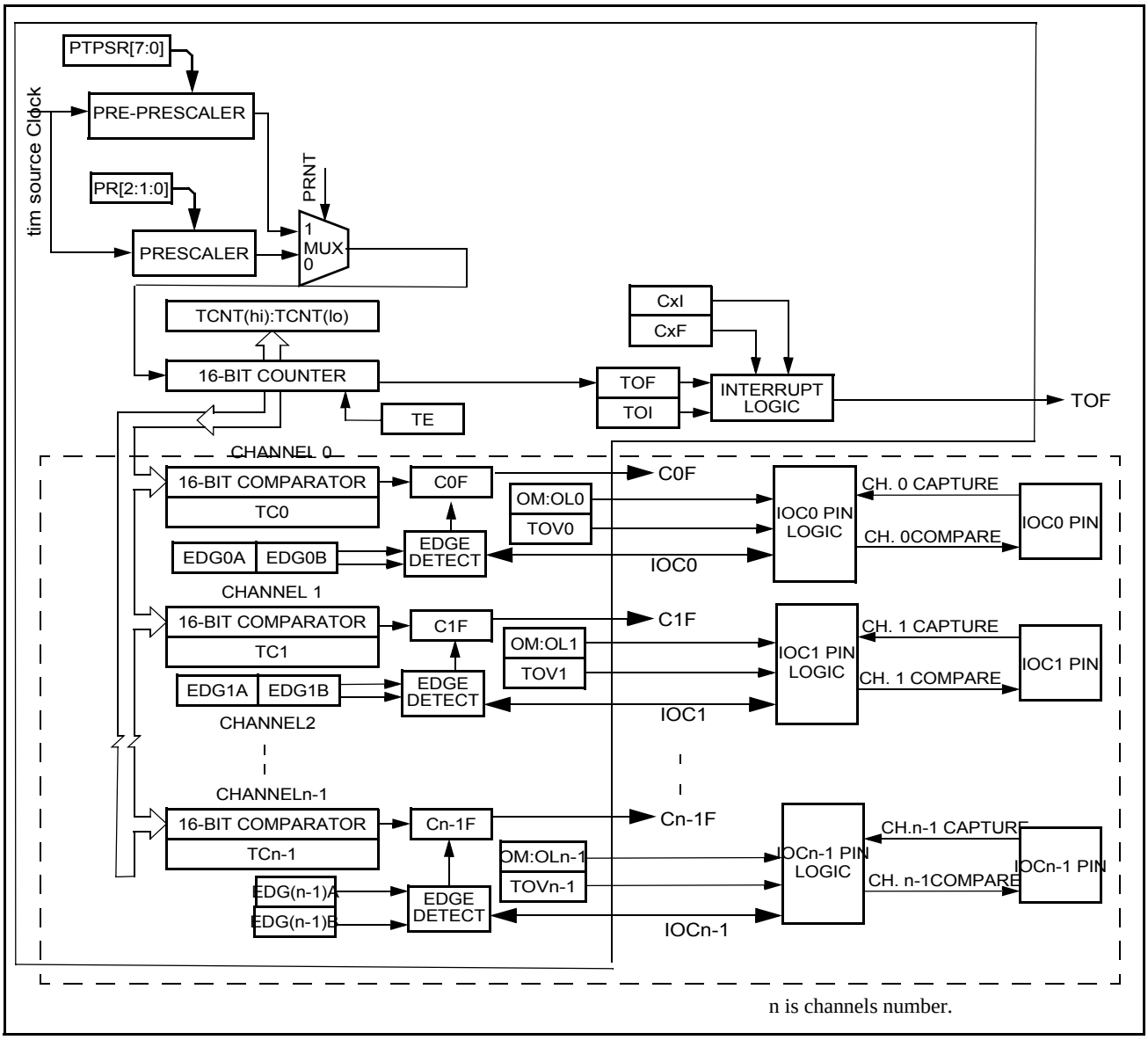


Figure 15-22. Detailed Timer Block Diagram

15.4.1 Prescaler

The prescaler divides the Bus clock by 1, 2, 4, 8, 16, 32, 64 or 128. The prescaler select bits, PR[2:0], select the prescaler divisor. PR[2:0] are in timer system control register 2 (TSCR2).

The prescaler divides the Bus clock by a prescalar value. Prescaler select bits PR[2:0] of in timer system control register 2 (TSCR2) are set to define a prescalar value that generates a divide by 1, 2, 4, 8, 16, 32, 64 and 128 when the PRNT bit in TSCR1 is disabled.

Module Base + 0x0001

	7	6	5	4	3	2	1	0
R W	PPOL7	PPOL6	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0
Reset	0	0	0	0	0	0	0	0

Figure 17-4. PWM Polarity Register (PWMPOL)

Read: Anytime

Write: Anytime

NOTE

PPOLx register bits can be written anytime. If the polarity is changed while a PWM signal is being generated, a truncated or stretched pulse can occur during the transition

Table 17-3. PWMPOL Field Descriptions

Note: Bits related to available channels have functional significance. Writing to unavailable bits has no effect. Read from unavailable bits return a zero

Field	Description
7–0 PPOL[7:0]	**Pulse Width Channel 7–0 Polarity Bits** 0 PWM channel 7–0 outputs are low at the beginning of the period, then go high when the duty count is reached. 1 PWM channel 7–0 outputs are high at the beginning of the period, then go low when the duty count is reached.

17.3.2.3 PWM Clock Select Register (PWMCLK)

Each PWM channel has a choice of four clocks to use as the clock source for that channel as described below.

Module Base + 0x0002

	7	6	5	4	3	2	1	0
R W	PCLK7	PCLKL6	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0
Reset	0	0	0	0	0	0	0	0

Figure 17-5. PWM Clock Select Register (PWMCLK)

Read: Anytime

Write: Anytime

NOTE

Register bits PCLK0 to PCLK7 can be written anytime. If a clock select is changed while a PWM signal is being generated, a truncated or stretched pulse can occur during the transition.

Table 18-3. SCICR1 Field Descriptions (continued)

Field	Description
5 RSRC	**Receiver Source Bit** — When LOOPS = 1, the RSRC bit determines the source for the receiver shift register input. See Table 18-4. 0 Receiver input internally connected to transmitter output 1 Receiver input connected externally to transmitter
4 M	**Data Format Mode Bit** — MODE determines whether data characters are eight or nine bits long. 0 One start bit, eight data bits, one stop bit 1 One start bit, nine data bits, one stop bit
3 WAKE	**Wakeup Condition Bit** — WAKE determines which condition wakes up the SCI: a logic 1 (address mark) in the most significant bit position of a received data character or an idle condition on the RXD pin. 0 Idle line wakeup 1 Address mark wakeup
2 ILT	**Idle Line Type Bit** — ILT determines when the receiver starts counting logic 1s as idle character bits. The counting begins either after the start bit or after the stop bit. If the count begins after the start bit, then a string of logic 1s preceding the stop bit may cause false recognition of an idle character. Beginning the count after the stop bit avoids false idle character recognition, but requires properly synchronized transmissions. 0 Idle character bit count begins after start bit 1 Idle character bit count begins after stop bit
1 PE	**Parity Enable Bit** — PE enables the parity function. When enabled, the parity function inserts a parity bit in the most significant bit position. 0 Parity function disabled 1 Parity function enabled
0 PT	**Parity Type Bit** — PT determines whether the SCI generates and checks for even parity or odd parity. With even parity, an even number of 1s clears the parity bit and an odd number of 1s sets the parity bit. With odd parity, an odd number of 1s clears the parity bit and an even number of 1s sets the parity bit. 0 Even parity 1 Odd parity

Table 18-4. Loop Functions

LOOPS	RSRC	Function
0	x	Normal operation
1	0	Loop mode with transmitter output internally connected to receiver input
1	1	Single-wire mode with TXD pin connected to receiver input

18.3.2.3 SCI Alternative Status Register 1 (SCIASR1)

Module Base + 0x0000

	7	6	5	4	3	2	1	0
R	RXEDGIF	0	0	0	0	BERRV	BERRIF	BKDIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 18-6. SCI Alternative Status Register 1 (SCIASR1)

Read: Anytime, if AMAP = 1

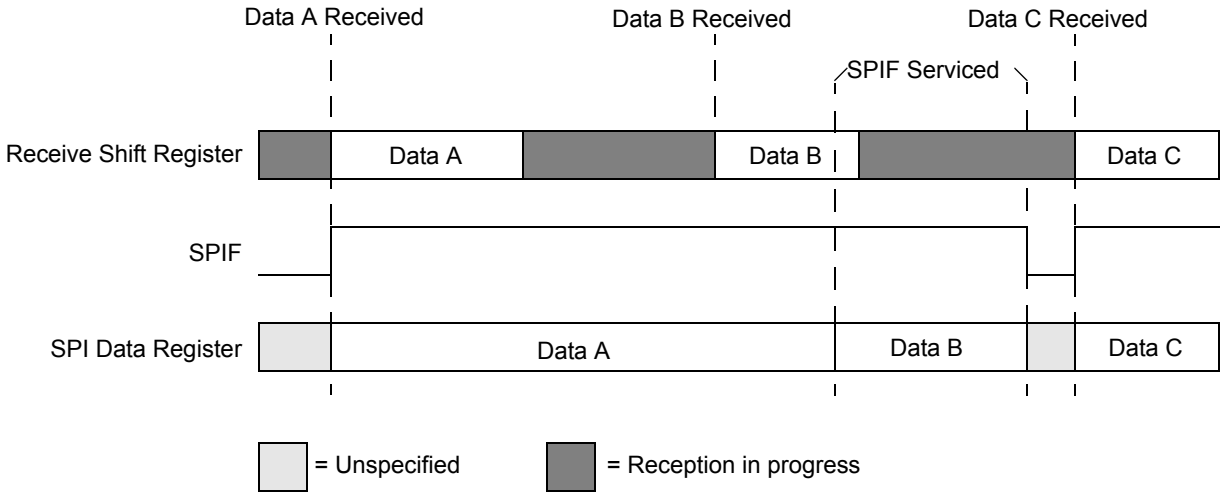


Figure 19-9. Reception with SPIF serviced in Time

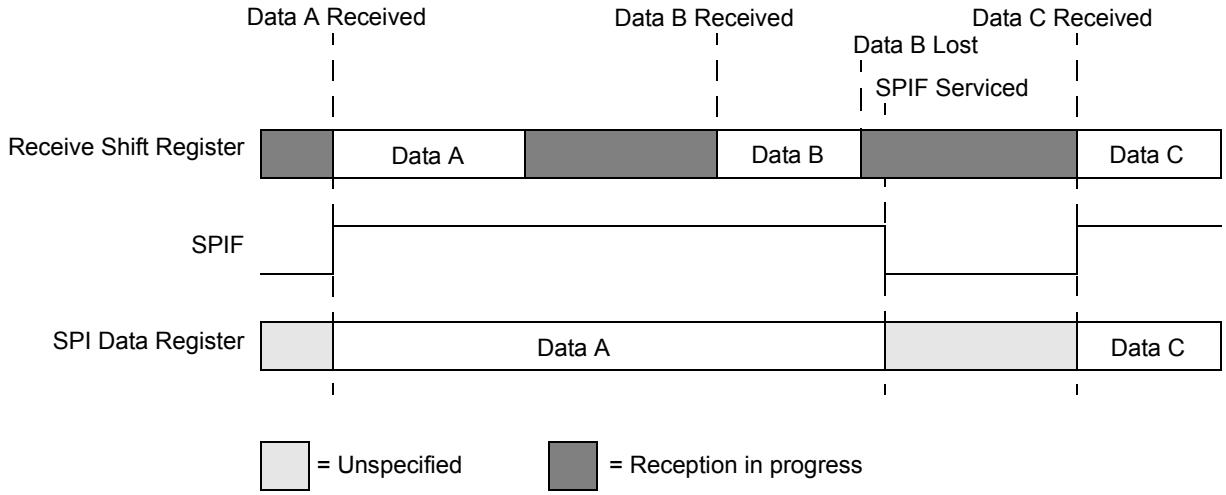


Figure 19-10. Reception with SPIF serviced too late

19.4 Functional Description

The SPI module allows a duplex, synchronous, serial communication between the MCU and peripheral devices. Software can poll the SPI status flags or SPI operation can be interrupt driven.

The SPI system is enabled by setting the SPI enable (SPE) bit in SPI control register 1. While SPE is set, the four associated SPI port pins are dedicated to the SPI function as:

- Slave select ($\overline{SS}$)
- Serial clock (SCK)
- Master out/slave in (MOSI)
- Master in/slave out (MISO)

Table 21-5. LPSLRM Field Description

Field	Description
7 LPDTDIS	TxD-dominant timeout disable Bit — This bit disables the TxD-dominant timeout feature. Disabling this feature is only recommended for using the LIN Physical Layer for other applications than LIN protocol. It is only writable in shutdown mode (LPE=0). 0 TxD-dominant timeout feature is enabled. 1 TxD-dominant timeout feature is disabled.
1-0 LPSLR[1:0]	Slew-Rate Bits — Please see section Section 21.4.2, “Slew Rate and LIN Mode Selection for details on how the slew rate control works. These bits are only writable in shutdown mode (LPE=0). 00 Normal Slew Rate (optimized for 20 kbit/s). 01 Slow Slew Rate (optimized for 10.4 kbit/s). 10 Fast Mode Slew Rate (up to 250 kbit/s). This mode is not compliant with the LIN Protocol (LIN electrical characteristics like duty cycles, reference levels, etc. are not fulfilled). It is only meant to be used for fast data transmission. Please refer to section Section 21.4.2.2, “Fast Mode (not LIN compliant) for more details on fast mode.Please note that an external pullup resistor stronger than 1 kΩ might be necessary for the range 100 kbit/s to 250 kbit/s. 11 Reserved .

21.3.2.5 Reserved Register

Module Base + Address 0x0004 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset	x	x	x	x	x	x	x	x

= Unimplemented

Figure 21-7. Reserved Register

[1] Read: Anytime
Write: Only in special mode

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in special mode can alter the module’s functionality.

Table 21-6. Reserved Register Field Description

Field	Description
7-0 Reserved	These reserved bits are used for test purposes. Writing to these bits can alter the module functionality.

Table 22-26. FCCOB - NVM Command Mode (Typical Usage)

CCOBIX[2:0]	Register	Byte	FCCOB Parameter Fields (NVM Command Mode)
011	FCCOB3	HI	Data 1 [15:8]
		LO	Data 1 [7:0]
100	FCCOB4	HI	Data 2 [15:8]
		LO	Data 2 [7:0]
101	FCCOB5	HI	Data 3 [15:8]
		LO	Data 3 [7:0]

22.4 Functional Description

22.4.1 Modes of Operation

The module provides the modes of operation normal and special. The operating mode is determined by module-level inputs and affects the FCLKDIV, FCNFG, and DFPROT registers (see Table 22-28).

22.4.2 IFR Version ID Word

The version ID word is stored in the IFR at address 0x1F_C0B6. The contents of the word are defined in Table 22-27.

Table 22-27. IFR Version ID Fields

[15:4]	[3:0]
Reserved	VERNUM

- VERNUM: Version number. The first version is number 0b_0001 with both 0b_0000 and 0b_1111 meaning ‘none’.

22.4.3 Flash Block Read Access

If data read from the Flash block results in a double-bit fault ECC error (meaning that data is detected to be in error and cannot be corrected), the read data will be tagged as invalid during that access (please look into the Reference Manual for details). Forcing the DFDF status bit by setting FDFD (see Section 22.3.2.5) has effect only on the DFDF status bit value and does not result in an invalid access.

To guarantee the proper read timing from the Flash array, the Flash will control (i.e. pause) the S12Z core accesses, considering that the MCU can be configured to fetch data at a faster frequency than the Flash

maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level.

Table A-3. Absolute Maximum Ratings[1]

Num	Rating	Symbol	Min	Max	Unit
1	Voltage regulator and LINPHY supply voltage	V_{SUP}	-0.3	42	V
2	DC voltage on LIN	V_{LIN}	-32	42	V
3	Voltage Regulator Ballast Connection	V_{BCTL}	-0.3	42	V
4	Supplies VDDA, VDDX	V_{VDDACX}	-0.3	6	V
5	Voltage difference V_{DDX} to V_{DDA}[2]	Δ_{VDDX}	–0.3	0.3	V
6	Voltage difference V_{SSX} to V_{SSA}	Δ_{VSSX}	–0.3	0.3	V
7	Digital I/O input voltage	V_{IN}	–0.3	6.0	V
8	HVI PL0 input voltage	V_{Lx}	–27	42.0	V
9	EXTAL, XTAL [3]	V_{ILV}	–0.3	2.16	V
10	TEST input	V_{TEST}	–0.3	10.0	V
11	Instantaneous maximum current Single pin limit for all digital I/O pins[4]	I_D	–25	+25	mA
12	Continuous current on LIN	I_{LIN}		± 200 [5]	mA
13	Instantaneous maximum current on PP7	I_{PP7}	–80	+25	mA
14	Instantaneous maximum current on PP1, PP3[6] and PP5[6]	I_{PP135}	–30	+80	mA
15	Instantaneous maximum current Single pin limit for EXTAL, XTAL	I_{DL}	–25	+25	mA
16	Storage temperature range	T_{stg}	–65	155	°C

1 Beyond absolute maximum ratings device might be damaged.

2 VDDX and VDDA must be shorted

3 EXTAL, XTAL pins configured for external oscillator operation only

4 All digital I/O pins are internally clamped to V_{SSX} and V_{DDX}, or V_{SSA} and V_{DDA}.

5 The current on the LIN pin is internally limited. Therefore, it should not be possible to reach the 200mA anyway.

6 only applicable for PP3 and PP5 if pin VSSX2 is available

A.1.4 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 stress test qualification for automotive grade integrated circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM) and the Charged-Device Model.

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table C-3. ADC Conversion Performance 5V range

Supply voltage:
MC9S12ZVL(S)32\16\8: 4.5V ≤ V_{DDX} ≤ 5.5V, 4.5V ≤ V_{REF} ≤ 5.5V,
MC9S12ZVL(A)128\96\64: 4.85V ≤ V_{DDX} ≤ 5.15V, 4.85V ≤ V_{REF} ≤ 5.15V,
-40°C < T_J < 175°C, V_{REF} = V_{RH} - V_{RL}, f_{ADCCLK} = 8.0MHz
The values are tested to be valid with no port AD output drivers switching simultaneous with conversions.

Num	Rating[1]		Symbol	Min	Typ	Max	Unit
1	Resolution	12-Bit	LSB		1.25		mV
2	Differential Nonlinearity	12-Bit	DNL	-4	±2	4	counts
3	Integral Nonlinearity	12-Bit	INL	-5	±2.5	5	counts
4	Absolute Error[2]	12-Bit	AE	-7	±4	7	counts
5	Resolution	10-Bit	LSB		5		mV
6	Differential Nonlinearity	10-Bit	DNL	-1	±0.5	1	counts
7	Integral Nonlinearity	10-Bit	INL	-2	±1	2	counts
8	Absolute Error[2]	10-Bit	AE	-3	±2	3	counts
9	Resolution	8-Bit	LSB		20		mV
10	Differential Nonlinearity	8-Bit	DNL	-0.5	±0.3	0.5	counts
11	Integral Nonlinearity	8-Bit	INL	-1	±0.5	1	counts
12	Absolute Error[2]	8-Bit	AE	-1.5	±1	1.5	counts

1 The 8-bit and 10-bit mode operation is structurally tested in production test. Absolute values are tested in 12-bit mode.

2 These values include the quantization error which is inherently 1/2 count for any A/D converter.

Table C-4. DC Conversion Performance 3.3V range

Supply voltage MC9S12ZVL(A)128\96\64: 3.20V ≤ V_{DDA} ≤ 3.39V, -40°C < T_J < 175°C. 3.20V ≤ V_{REF} ≤ 3.39V = V_{RH} - V_{RL}.
f_{ADCCLK} = 8.0MHz
The values are tested to be valid with no port AD output drivers switching simultaneous with conversions.

Num	Rating[1]		Symbol	Min	Typ	Max	Unit
1	Resolution	12-Bit	LSB		0.80		mV
2	Differential Nonlinearity	12-Bit	DNL	-6	±3	6	counts
3	Integral Nonlinearity	12-Bit	INL	-7	±3	7	counts
4	Absolute Error[2]	12-Bit	AE	-8	±4	8	counts
5	Resolution	10-Bit	LSB		3.22		mV
6	Differential Nonlinearity	10-Bit	DNL	-1.5	±1	1.5	counts
7	Integral Nonlinearity	10-Bit	INL	-2	±1	2	counts
8	Absolute Error[2]	10-Bit	AE	-3	±2	3	counts
9	Resolution	8-Bit	LSB		12.89		mV
10	Differential Nonlinearity	8-Bit	DNL	-0.5	±0.3	0.5	counts
11	Integral Nonlinearity	8-Bit	INL	-1	±0.5	1	counts
12	Absolute Error[2]	8-Bit	AE	-1.5	±1	1.5	counts

[4] The structure of the HVI pins does not include diode structures shown in Figure A-1 that inject current when the input voltage goes outside the supply-ground range. Thus the HVI pin current injection is limited to below 200uA within the absolute maximum pin voltage range. However if the HVI impedance converter bypass is enabled, then even currents in this range can corrupt ADC results from simultaneous conversions on other channels. This can be prevented by disabling the bypass, either by clearing the PTAENLx or PTABYPLx bit. Similarly when the ADC is converting a HVI pin voltage then the impedance converter bypass must be disabled to ensure that current injection on PADx pins does not impact the HVI ADC conversion result.