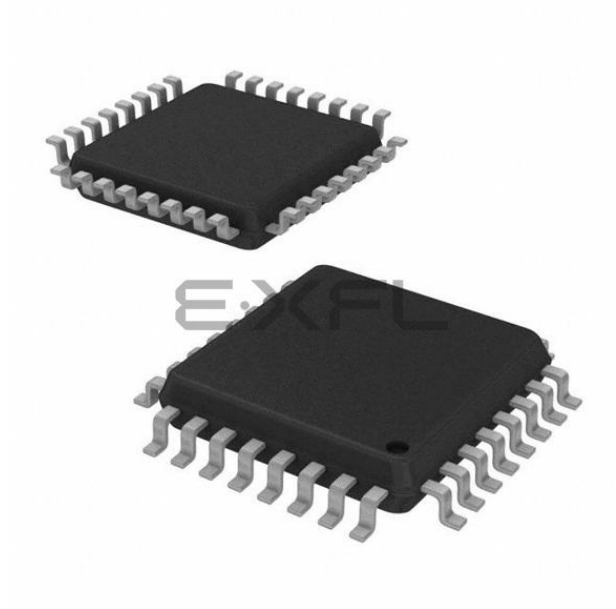

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SCI, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	19
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	5.5V ~ 18V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvl64f0mlc

- Instructions and Addressing modes optimized for C-Programming & Compiler
  - MAC unit 32bit += 32bit*32bit
  - Hardware divider
  - Single cycle multi-bit shifts (Barrel shifter)
  - Special instructions for fixed point math
- Unimplemented opcode traps
- Unprogrammed byte value (0xFF) defaults to SWI instruction

1.4.1.1 Background Debug Controller (BDC)

- Background debug controller (BDC) with single-wire interface
  - Non-intrusive memory access commands
  - Supports in-circuit programming of on-chip nonvolatile memory

1.4.1.2 Debugger (DBG)

- Three comparators (A, B and D)
  - Comparator A compares the full address bus and full 32-bit data bus
  - Comparators B and D compare the full address bus only
  - Each comparator can be configured to monitor PC addresses or addresses of data accesses
  - Each comparator can select either read or write access cycles
  - Comparator matches can force state sequencer state transitions
- Three comparator modes
  - Simple address/data comparator match mode
  - Inside address range mode, Addmin ≤ Address ≤ Addmax
  - Outside address range match mode, Address < Addmin or Address > Addmax
- State sequencer control
  - State transitions forced by comparator matches
  - State transitions forced by software write to TRIG
  - State transitions forced by an external event
- The following types of breakpoints
  - CPU breakpoint entering active BDM on breakpoint (BDM)
  - CPU breakpoint executing SWI on breakpoint (SWI)

1.4.2 Embedded Memory

1.4.2.1 Memory Access Integrity

- Illegal address detection
- ECC support on embedded NVM and system RAM

1.9.6.2 DAC Connectivity

DAC reference Voltage signal VRH is mapped to VDDA and VRL is mapped to VSSA. The DACU pin is not connected on the MC9S12ZVLA device.

1.9.7 PWM channel mapping

The table below shows the mapping of the available PWM module channels to the PIM module.

1.9.7.1 PWM channel mapping for MC9S12ZVL(S)32/16/8

See below the PWM0 channel mapping for MC9S12ZVL(S)32/16/8 devices.

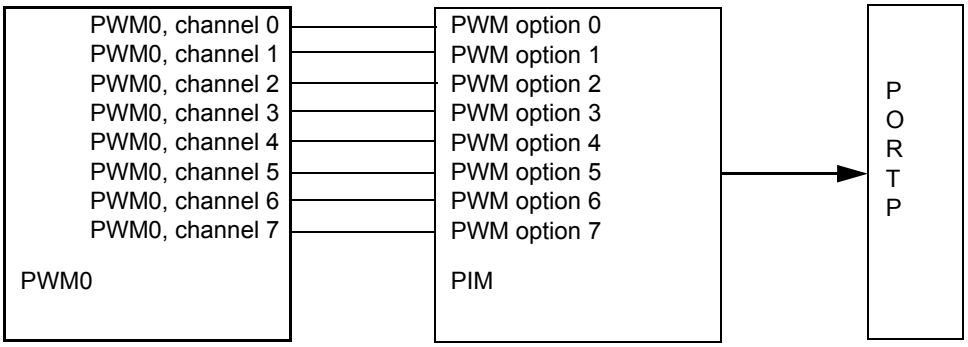


Figure 1-7. PWM Channel mapping MC9S12ZVL(S)32/16/8

1.9.7.2 PWM channel mapping for MC9S12ZVL(A)128/96/64

See below the PWM0 and PWM1 channel mapping for MC9S12ZVL(A)128/96/64 devices.

5.1.1 Glossary

Table 5-2. Glossary Of Terms

Term	Definition
DBG	On chip Debug Module
BDM	Active Background Debug Mode
CPU	S12Z CPU
SSC	Special Single Chip Mode (device operating mode
NSC	Normal Single Chip Mode (device operating mode)
BDCSI	Background Debug Controller Serial Interface. This refers to the single pin BKGD serial interface.
EWAIT	Optional S12 feature which allows external devices to delay external accesses until deassertion of EWAIT

5.1.2 Features

The BDC includes these distinctive features:

- Single-wire communication with host development system
- SYNC command to determine communication rate
- Genuine non-intrusive handshake protocol
- Enhanced handshake protocol for error detection and stop mode recognition
- Active out of reset in special single chip mode
- Most commands not requiring active BDM, for minimal CPU intervention
- Full global memory map access without paging
- Simple flash mass erase capability

5.1.3 Modes of Operation

S12 devices feature power modes (run, wait, and stop) and operating modes (normal single chip, special single chip). Furthermore, the operation of the BDC is dependent on the device security status.

5.1.3.1 BDC Modes

The BDC features module specific modes, namely disabled, enabled and active. These modes are dependent on the device security and operating mode. In active BDM the CPU ceases execution, to allow BDC system access to all internal resources including CPU internal registers.

5.1.3.2 Security and Operating mode Dependency

In device run mode the BDC dependency is as follows

- Normal modes, unsecure device

  General BDC operation available. The BDC is disabled out of reset.

- Through comparator matches via Final State.
- Through software writing to the TRIG bit in the DBGC1 register via Final State.
- Through the external event input (DBGEEV) via Final State.

Breakpoints are not generated by software writes to DBGC1 that clear the ARM bit.

7.4.5.1 Breakpoints From Comparator Matches or External Events

Breakpoints can be generated when the state sequencer transitions to State0 following a comparator match or an external event.

7.4.5.2 Breakpoints Generated Via The TRIG Bit

When TRIG is written to “1”, the Final State is entered. In the next cycle TRIG breakpoints are possible even if the DBG module is disarmed.

7.4.5.3 DBG Breakpoint Priorities

7.4.5.3.1 DBG Breakpoint Priorities And BDC Interfacing

Breakpoint operation is dependent on the state of the S12ZBDC module. BDM cannot be entered from a breakpoint unless the BDC is enabled (ENBDC bit is set in the BDC). If BDM is already active, breakpoints are disabled. In addition, while executing a BDC STEP1 command, breakpoints are disabled.

When the DBG breakpoints are mapped to BDM (BDMBP set), then if a breakpoint request, either from a BDC BACKGROUND command or a DBG event, coincides with an SWI instruction in application code, (i.e. the DBG requests a breakpoint at the next instruction boundary and the next instruction is an SWI) then the CPU gives priority to the BDM request over the SWI request.

On returning from BDM, the SWI from user code gets executed. Breakpoint generation control is summarized in Table 7-32.

Table 7-32. Breakpoint Mapping Summary

BRKCPU	BDMBP Bit (DBGC1[4])	BDC Enabled	BDM Active	Breakpoint Mapping
0	X	X	X	No Breakpoint
1	0	X	0	Breakpoint to SWI
1	0	1	1	No Breakpoint
1	1	0	X	No Breakpoint
1	1	1	0	Breakpoint to BDM
1	1	1	1	No Breakpoint

– Enable the external oscillator (OSCE bit).
– Wait for oscillator to start up (UPOSC=1).
– Select the Oscillator Clock (OSCCLK) as source of the Bus Clock (PLLSEL=0).

— The PLLCLK is on and used to qualify the external oscillator clock.

9.1.2.2 Wait Mode

For S12CPMU_UHV Wait Mode is the same as Run Mode.

9.1.2.3 Stop Mode

Stop mode can be entered by executing the CPU STOP instruction. See device level specification for more details.

The voltage regulator is in Reduced Performance Mode (RPM).

NOTE

The voltage regulator output voltage may degrade to a lower value than in Full Performance Mode (FPM), additionally the current sourcing capability is substantially reduced (see also Appendix for VREG electrical parameters). Only clock source ACLK is available and the Power On Reset (POR) circuitry is functional. The Low Voltage Interrupt (LVI) and Low Voltage Reset (LVR) are disabled.

The API is available.

The Phase Locked Loop (PLL) is off.

The Internal Reference Clock (IRC1M) is off.

Core Clock and Bus Clock are stopped.

Depending on the setting of the PSTP and the OSCE bit, Stop Mode can be differentiated between Full Stop Mode (PSTP = 0 or OSCE=0) and Pseudo Stop Mode (PSTP = 1 and OSCE=1). In addition, the behavior of the COP in each mode will change based on the clocking method selected by COPOSCSEL[1:0].

- **Full Stop Mode (PSTP = 0 or OSCE=0)**
  External oscillator (XOSCLCP) is disabled.
  — If COPOSCSEL1=0:
  The COP and RTI counters halt during Full Stop Mode.
  After wake-up from Full Stop Mode the Core Clock and Bus Clock are running on PLLCLK (PLLSEL=1). COP and RTI are running on IRCCLK (COPOSCSEL0=0, RTIOSCSEL=0).
  — If COPOSCSEL1=1:
  The clock for the COP is derived from ACLK (trimmable internal RC-Oscillator clock). During Full Stop Mode the ACLK for the COP can be stopped (COP static) or running (COP active) depending on the setting of bit CSAD. When bit CSAD is set the ACLK clock source for the

NOTE

Each conversion flow control bit (SEQA, RSTA, TRIG, LDOK) must be controlled by software or internal interface according to the requirements described in Section 10.6.3.2.4, “The two conversion flow control Mode Configurations and overview summary in Table 10-11.

10.9.9 Triggered Conversion — Single CSL

Applications that require the conversion of one or more groups of different channels in a periodic and timed manner can make use of a configuration in “Trigger Mode” with a single CSL containing a list of sequences. This means the CSL consists of several sequences each separated by an “End of Sequence” command. The last command of the CSL uses the “End Of List” command with wrap to top of CSL and waiting for a Trigger (CMD_SEL[1:0] =2’b11). Hence after the initial Restart Event each sequence can be launched via a Trigger Event and repetition of the CSL can be launched via a Trigger after execution of the “End Of List” command.

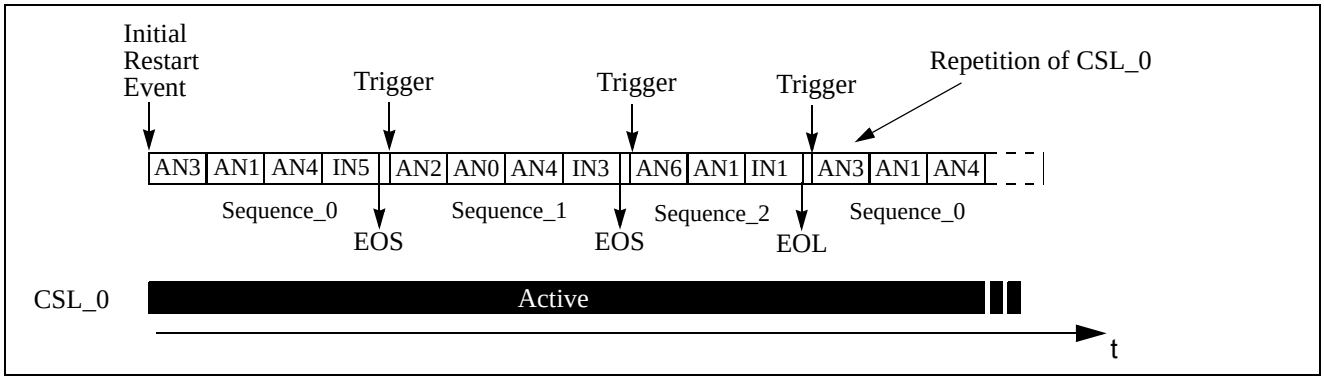


Figure 10-42. Conversion Flow Control Diagram — Triggered Conversion (CSL Repetition)

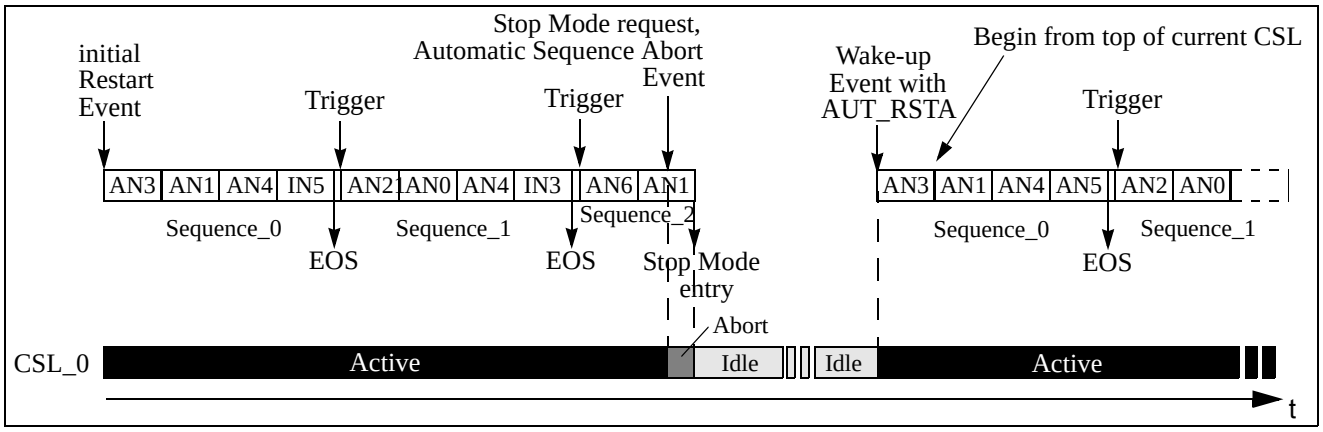


Figure 10-43. Conversion Flow Control Diagram — Triggered Conversion (with Stop Mode)

In case a Low Power Mode is used:
If bit AUT_RSTA is set before Low Power Mode is entered, the conversion continues automatically as soon as a low power mode (Stop Mode or Wait Mode with bit SWAI set) is exited.

13.3.2.10 MSCAN Transmitter Message Abort Acknowledge Register (CANTAAK)

The CANTAAK register indicates the successful abort of a queued message, if requested by the appropriate bits in the CANTARQ register.

Module Base + 0x0009 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 13-13. MSCAN Transmitter Message Abort Acknowledge Register (CANTAAK)

1 Read: Anytime
Write: Unimplemented

NOTE

The CANTAAK register is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK = 1).

Table 13-16. CANTAAK Register Field Descriptions

Field	Description
2-0 ABTAK[2:0]	**Abort Acknowledge** — This flag acknowledges that a message was aborted due to a pending abort request from the CPU. After a particular message buffer is flagged empty, this flag can be used by the application software to identify whether the message was aborted successfully or was sent anyway. The ABTAKx flag is cleared whenever the corresponding TXE flag is cleared. 0 The message was not aborted. 1 The message was aborted.

13.3.2.11 MSCAN Transmit Buffer Selection Register (CANTBSEL)

The CANTBSEL register allows the selection of the actual transmit message buffer, which then will be accessible in the CANTXFG register space.

Module Base + 0x000A Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	TX2	TX1	TX0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 13-14. MSCAN Transmit Buffer Selection Register (CANTBSEL)

1 Read: Find the lowest ordered bit set to 1, all other bits will be read as 0
Write: Anytime when not in initialization mode

16.2 External Signal Description

The TIM16B2CV3 module has a selected number of external pins. Refer to device specification for exact number.

16.2.1 IOC1 - IOC0 — Input Capture and Output Compare Channel 1-0

Those pins serve as input capture or output compare for TIM16B2CV3 channel .

NOTE

For the description of interrupts see Section 16.6, “Interrupts”.

16.3 Memory Map and Register Definition

This section provides a detailed description of all memory and registers.

16.3.1 Module Memory Map

The memory map for the TIM16B2CV3 module is given below in Figure 16-3. The address listed for each register is the address offset. The total address for each register is the sum of the base address for the TIM16B2CV3 module and the address offset for each register.

16.3.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

Only bits related to implemented channels are valid.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 TIOS	R	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	IOS1	IOS0
	W								
0x0001 CFORC	R	0	0	0	0	0	0	0	0
	W	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	FOC1	FOC0
0x0004 TCNTH	R	TCNT15	TCNT14	TCNT13	TCNT12	TCNT11	TCNT10	TCNT9	TCNT8
	W								
0x0005 TCNTL	R	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0
	W								
0x0006 TSCR1	R	TEN	TSWAI	TSFRZ	TFFCA	PRNT	0	0	0
	W								
0x0007 TTOV	R	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	TOV1	TOV0
	W								
0x0008 TCTL1	R	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	W								

Figure 16-3. TIM16B2CV3 Register Summary (Sheet 1 of 2)

Table 17-2. PWME Field Descriptions

Note: Bits related to available channels have functional significance. Writing to unavailable bits has no effect. Read from unavailable bits return a zero

Field	Description
7 PWME7	Pulse Width Channel 7 Enable 0 Pulse width channel 7 is disabled. 1 Pulse width channel 7 is enabled. The pulse modulated signal becomes available at PWM output bit 7 when its clock source begins its next cycle.
6 PWME6	Pulse Width Channel 6 Enable 0 Pulse width channel 6 is disabled. 1 Pulse width channel 6 is enabled. The pulse modulated signal becomes available at PWM output bit 6 when its clock source begins its next cycle. If CON67=1, then bit has no effect and PWM output line 6 is disabled.
5 PWME5	Pulse Width Channel 5 Enable 0 Pulse width channel 5 is disabled. 1 Pulse width channel 5 is enabled. The pulse modulated signal becomes available at PWM output bit 5 when its clock source begins its next cycle.
4 PWME4	Pulse Width Channel 4 Enable 0 Pulse width channel 4 is disabled. 1 Pulse width channel 4 is enabled. The pulse modulated signal becomes available at PWM, output bit 4 when its clock source begins its next cycle. If CON45 = 1, then bit has no effect and PWM output line 4 is disabled.
3 PWME3	Pulse Width Channel 3 Enable 0 Pulse width channel 3 is disabled. 1 Pulse width channel 3 is enabled. The pulse modulated signal becomes available at PWM, output bit 3 when its clock source begins its next cycle.
2 PWME2	Pulse Width Channel 2 Enable 0 Pulse width channel 2 is disabled. 1 Pulse width channel 2 is enabled. The pulse modulated signal becomes available at PWM, output bit 2 when its clock source begins its next cycle. If CON23 = 1, then bit has no effect and PWM output line 2 is disabled.
1 PWME1	Pulse Width Channel 1 Enable 0 Pulse width channel 1 is disabled. 1 Pulse width channel 1 is enabled. The pulse modulated signal becomes available at PWM, output bit 1 when its clock source begins its next cycle.
0 PWME0	Pulse Width Channel 0 Enable 0 Pulse width channel 0 is disabled. 1 Pulse width channel 0 is enabled. The pulse modulated signal becomes available at PWM, output bit 0 when its clock source begins its next cycle. If CON01 = 1, then bit has no effect and PWM output line 0 is disabled.

17.3.2.2 PWM Polarity Register (PWMPOL)

The starting polarity of each PWM channel waveform is determined by the associated PPOLx bit in the PWMPOL register. If the polarity bit is one, the PWM channel output is high at the beginning of the cycle and then goes low when the duty count is reached. Conversely, if the polarity bit is zero, the output starts low and then goes high when the duty count is reached.

Write: Anytime, if AMAP = 1

Table 18-5. SCIASR1 Field Descriptions

Field	Description
7 RXEDGIF	**Receive Input Active Edge Interrupt Flag** — RXEDGIF is asserted, if an active edge (falling if RXPOL = 0, rising if RXPOL = 1) on the RXD input occurs. RXEDGIF bit is cleared by writing a “1” to it. 0 No active receive on the receive input has occurred 1 An active edge on the receive input has occurred
2 BERRV	**Bit Error Value** — BERRV reflects the state of the RXD input when the bit error detect circuitry is enabled and a mismatch to the expected value happened. The value is only meaningful, if BERRIF = 1. 0 A low input was sampled, when a high was expected 1 A high input reassembled, when a low was expected
1 BERRIF	**Bit Error Interrupt Flag** — BERRIF is asserted, when the bit error detect circuitry is enabled and if the value sampled at the RXD input does not match the transmitted value. If the BERRIE interrupt enable bit is set an interrupt will be generated. The BERRIF bit is cleared by writing a “1” to it. 0 No mismatch detected 1 A mismatch has occurred
0 BKDIF	**Break Detect Interrupt Flag** — BKDIF is asserted, if the break detect circuitry is enabled and a break signal is received. If the BKDIE interrupt enable bit is set an interrupt will be generated. The BKDIF bit is cleared by writing a “1” to it. 0 No break signal was received 1 A break signal was received

18.3.2.4 SCI Alternative Control Register 1 (SCIACR1)

Module Base + 0x0001

	7	6	5	4	3	2	1	0
R	RXEDGIE	0	0	0	0	0	BERRIE	BKDIE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 18-7. SCI Alternative Control Register 1 (SCIACR1)

Read: Anytime, if AMAP = 1

Write: Anytime, if AMAP = 1

Table 18-6. SCIACR1 Field Descriptions

Field	Description
7 RXEDGIE	**Receive Input Active Edge Interrupt Enable** — RXEDGIE enables the receive input active edge interrupt flag, RXEDGIF, to generate interrupt requests. 0 RXEDGIF interrupt requests disabled 1 RXEDGIF interrupt requests enabled

If MODFEN is set and SSOE is cleared, the $\overline{SS}$ pin is configured as input for detecting mode fault error. If the $\overline{SS}$ input becomes low this indicates a mode fault error where another master tries to drive the MOSI and SCK lines. In this case, the SPI immediately switches to slave mode, by clearing the MSTR bit and also disables the slave output buffer MISO (or SISO in bidirectional mode). So the result is that all outputs are disabled and SCK, MOSI, and MISO are inputs. If a transmission is in progress when the mode fault occurs, the transmission is aborted and the SPI is forced into idle state.

This mode fault error also sets the mode fault (MODF) flag in the SPI status register (SPISR). If the SPI interrupt enable bit (SPIE) is set when the MODF flag becomes set, then an SPI interrupt sequence is also requested.

When a write to the SPI data register in the master occurs, there is a half SCK-cycle delay. After the delay, SCK is started within the master. The rest of the transfer operation differs slightly, depending on the clock format specified by the SPI clock phase bit, CPHA, in SPI control register 1 (see Section 19.4.3, “Transmission Formats”).

NOTE

A change of the bits CPOL, CPHA, SSOE, LSBFE, XFRW, MODFEN, SPC0, or BIDIROE with SPC0 set, SPPR2-SPPR0 and SPR2-SPR0 in master mode will abort a transmission in progress and force the SPI into idle state. The remote slave cannot detect this, therefore the master must ensure that the remote slave is returned to idle state.

19.4.2 Slave Mode

The SPI operates in slave mode when the MSTR bit in SPI control register 1 is clear.

- Serial clock

  In slave mode, SCK is the SPI clock input from the master.

- MISO, MOSI pin

  In slave mode, the function of the serial data output pin (MISO) and serial data input pin (MOSI) is determined by the SPC0 bit and BIDIROE bit in SPI control register 2.

- $\overline{SS}$ pin

  The $\overline{SS}$ pin is the slave select input. Before a data transmission occurs, the $\overline{SS}$ pin of the slave SPI must be low. $\overline{SS}$ must remain low until the transmission is complete. If $\overline{SS}$ goes high, the SPI is forced into idle state.

  The $\overline{SS}$ input also controls the serial data output pin, if $\overline{SS}$ is high (not selected), the serial data output pin is high impedance, and, if $\overline{SS}$ is low, the first bit in the SPI data register is driven out of the serial data output pin. Also, if the slave is not selected ($\overline{SS}$ is high), then the SCK input is ignored and no internal shifting of the SPI shift register occurs.

  Although the SPI is capable of duplex operation, some SPI peripherals are capable of only receiving SPI data in a slave mode. For these simpler devices, there is no serial data out pin.

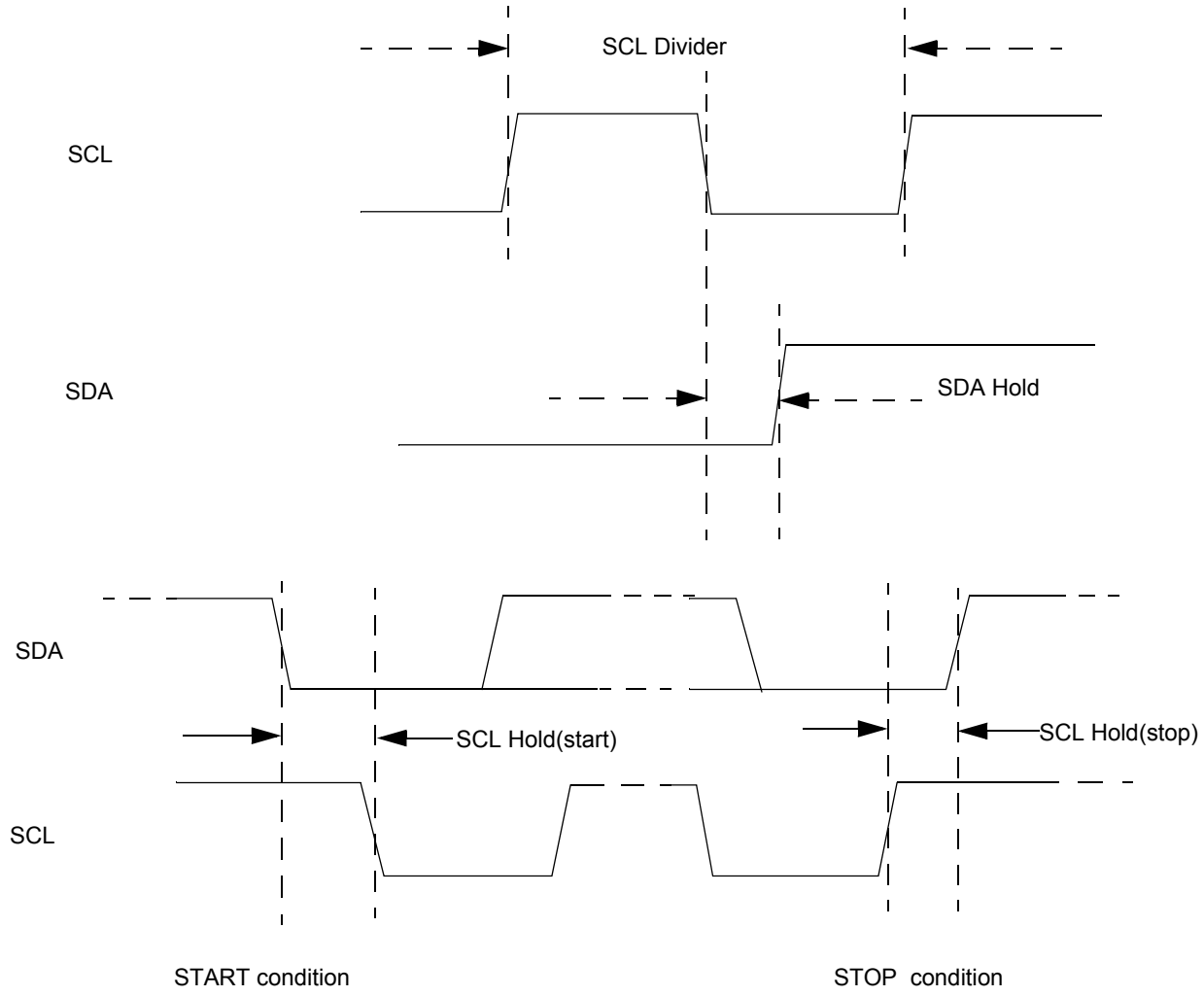


Figure 20-5. SCL Divider and SDA Hold

The equation used to generate the divider values from the IBFD bits is:

SCL Divider = MUL x {2 x (scl2tap + [(SCL_Tap -1) x tap2tap] + 2)}

The SDA hold delay is equal to the CPU clock period multiplied by the SDA Hold value shown in Table 20-7. The equation used to generate the SDA Hold value from the IBFD bits is:

SDA Hold = MUL x {scl2tap + [(SDA_Tap - 1) x tap2tap] + 3}

The equation for SCL Hold values to generate the start and stop conditions from the IBFD bits is:

SCL Hold(start) = MUL x [scl2start + (SCL_Tap - 1) x tap2tap]

SCL Hold(stop) = MUL x [scl2stop + (SCL_Tap - 1) x tap2tap]

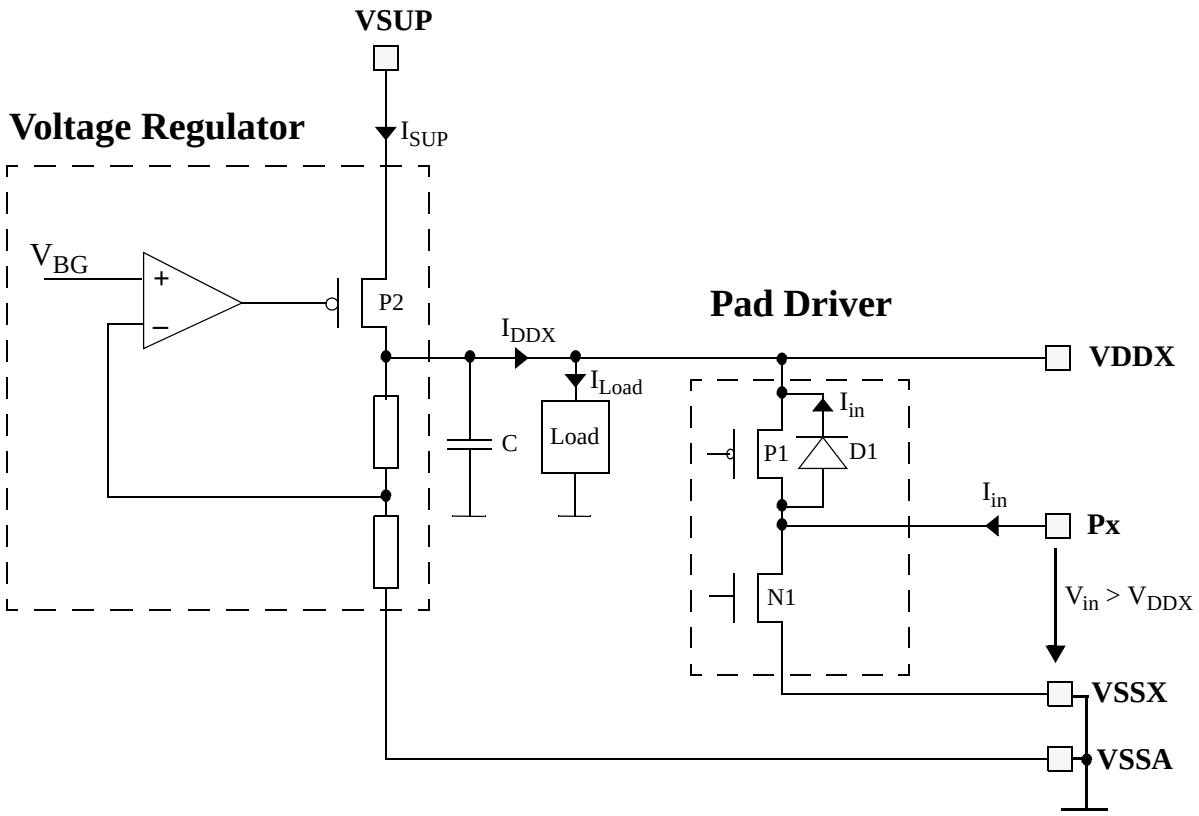
Table 20-7. IIC Divider and Hold Values (Sheet 1 of 6)

IBC[7:0] (hex)	SCL Divider (clocks)	SDA Hold (clocks)	SCL Hold (start)	SCL Hold (stop)
MUL=1				

A.1.2 Current Injection

Power supply must maintain regulation within operating V_{DDX} or V_{DD} range during instantaneous and operating maximum current conditions. Figure A-1 shows a 5V GPIO pad driver and the on chip voltage regulator with VDDX output. It shows also the power and ground pins VSUP, VDDX, VSSX and VSSA. Px represents any 5V GPIO pin. Assume Px is configured as an input. The pad driver transistors P1 and N1 are switched off (high impedance). If the voltage V_{in} on Px is greater than V_{DDX} a positive injection current I_{in} will flow through diode D1 into VDDX node. If this injection current I_{in} is greater than I_{Load}, the internal power supply VDDX may go out of regulation. Ensure the external V_{DDX} load will shunt current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power; e.g., if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

Figure A-1. Current Injection on GPIO Port if $V_{in} > V_{DDX}$



A.1.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. A functional operation outside these ranges is not guaranteed. Stress beyond these limits may affect the reliability or cause permanent damage of the device.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than

maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level.

Table A-3. Absolute Maximum Ratings[1]

Num	Rating	Symbol	Min	Max	Unit
1	Voltage regulator and LINPHY supply voltage	V_{SUP}	-0.3	42	V
2	DC voltage on LIN	V_{LIN}	-32	42	V
3	Voltage Regulator Ballast Connection	V_{BCTL}	-0.3	42	V
4	Supplies VDDA, VDDX	V_{VDDACX}	-0.3	6	V
5	Voltage difference V_{DDX} to V_{DDA}[2]	Δ_{VDDX}	–0.3	0.3	V
6	Voltage difference V_{SSX} to V_{SSA}	Δ_{VSSX}	–0.3	0.3	V
7	Digital I/O input voltage	V_{IN}	–0.3	6.0	V
8	HVI PL0 input voltage	V_{Lx}	–27	42.0	V
9	EXTAL, XTAL [3]	V_{ILV}	–0.3	2.16	V
10	TEST input	V_{TEST}	–0.3	10.0	V
11	Instantaneous maximum current Single pin limit for all digital I/O pins[4]	I_D	–25	+25	mA
12	Continuous current on LIN	I_{LIN}		± 200 [5]	mA
13	Instantaneous maximum current on PP7	I_{PP7}	–80	+25	mA
14	Instantaneous maximum current on PP1, PP3[6] and PP5[6]	I_{PP135}	–30	+80	mA
15	Instantaneous maximum current Single pin limit for EXTAL, XTAL	I_{DL}	–25	+25	mA
16	Storage temperature range	T_{stg}	–65	155	°C

1 Beyond absolute maximum ratings device might be damaged.

2 VDDX and VDDA must be shorted

3 EXTAL, XTAL pins configured for external oscillator operation only

4 All digital I/O pins are internally clamped to V_{SSX} and V_{DDX}, or V_{SSA} and V_{DDA}.

5 The current on the LIN pin is internally limited. Therefore, it should not be possible to reach the 200mA anyway.

6 only applicable for PP3 and PP5 if pin VSSX2 is available

A.1.4 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 stress test qualification for automotive grade integrated circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM) and the Charged-Device Model.

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table A-17. Run and Wait Current Characteristics for ZVL(A)128/96/64

Conditions are: V_{SUP} = 18V, see Table A-14 and Table A-15						
Num	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	Run Current, -40°C < T_J ≤150°C, f_{bus}=32MHz	I_{SUPR}	—	21	27	mA
2	Run Current, 150°C < T_J < 175°C, f_{bus}=25MHz	I_{SUPR}	—	21	27	mA
3	Wait Current, -40°C < T_J ≤ 150°C, f_{bus}=32MHz	I_{SUPW}	—	13	20	mA
4	Wait Current, 150°C < T_J < 175°C, f_{bus}=25MHz	I_{SUPW}	—	13	20	mA

Table A-18. Stop Current Characteristics for ZVL(S)32/16/8

Conditions are: V_{SUP} = 12V						
Num	**Rating**[1]	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Stop Current all modules off						
1	T_J= -40°C	I_{SUPS}	—	20	28	µA
2	T_J= 25°C	I_{SUPS}	—	23	33	µA
3	T_J= 85°C	I_{SUPS}	—	44	55	µA
4	T_J= 105°C	I_{SUPS}	—	63	85	µA
5	T_J= 125°C	I_{SUPS}	—	115	156	µA
Stop Current API enabled & LINPHY in standby						
6	T_J=25°C	I_{SUPS}	—	38	—	µA

1 If MCU is in STOP long enough then $T_A = T_J$. Die self heating due to stop current can be ignored.

Table A-19. Stop Current Characteristics for ZVL(A)128/96/64

Conditions are: V_{SUP} = 12V						
Num	**Rating**[1]	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Stop Current all modules off						
1	T_J= -40°C	I_{SUPS}	—	20	40	µA
2	T_J= 25°C	I_{SUPS}	—	25	50	µA
3	T_J= 85°C	I_{SUPS}	—	60	107	µA
4	T_J= 105°C	I_{SUPS}	—	78	176	µA
5	T_J= 125°C	I_{SUPS}	—	130	301	µA
Stop Current API enabled & LINPHY in standby						
6	T_J=25°C	I_{SUPS}	—	53	—	µA

1 If MCU is in STOP long enough then $T_A = T_J$. Die self heating due to stop current can be ignored.

Table A-20. Pseudo Stop Current Characteristics for ZVL(S)32/16/8

Conditions are: V_{SUP} = 12V, API, COP & RTI enabled						
Num	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	T_J = 25°C	I_{SUPPS}	—	155	350	µA

Appendix E
NVM Electrical Parameters

E.1 NVM Timing Parameters

The time base for all NVM program or erase operations is derived from the bus clock using the FCLKDIV register. The frequency of this derived clock must be set within the limits specified as f_{NVMOP}. The NVM module does not have any means to monitor the frequency and will not prevent program or erase operation at frequencies above or below the specified minimum. When attempting to program or erase the NVM module at a lower frequency, a full program or erase transition is not assured.

The device bus frequency f_{WSTAT}, below which the flash wait states can be disabled, is specified in the device operating conditions Table A-6.

The following sections provide equations which can be used to determine the time required to execute specific flash commands. All timing parameters are a function of the bus clock frequency, f_{NVMBUS}. All program and erase times are also a function of the NVM operating frequency, f_{NVMOP}. A summary of key timing parameters can be found in Table E-1 and Table E-2.