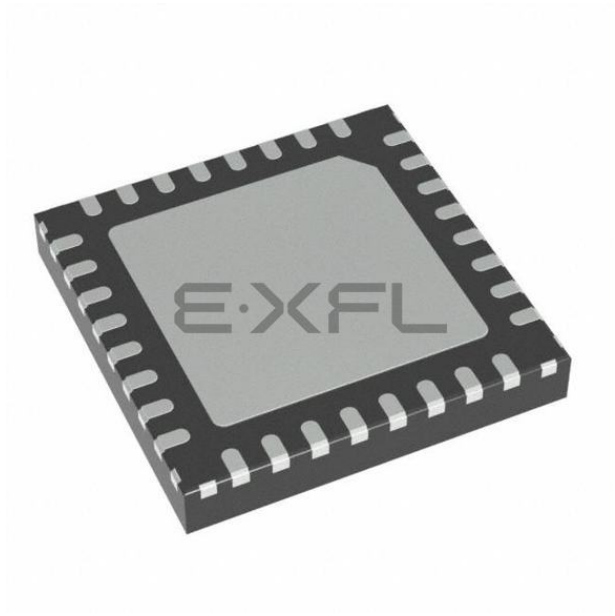

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Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SCI, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	19
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	5.5V ~ 18V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount, Wettable Flank
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN-EP (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvl64f0vfmr

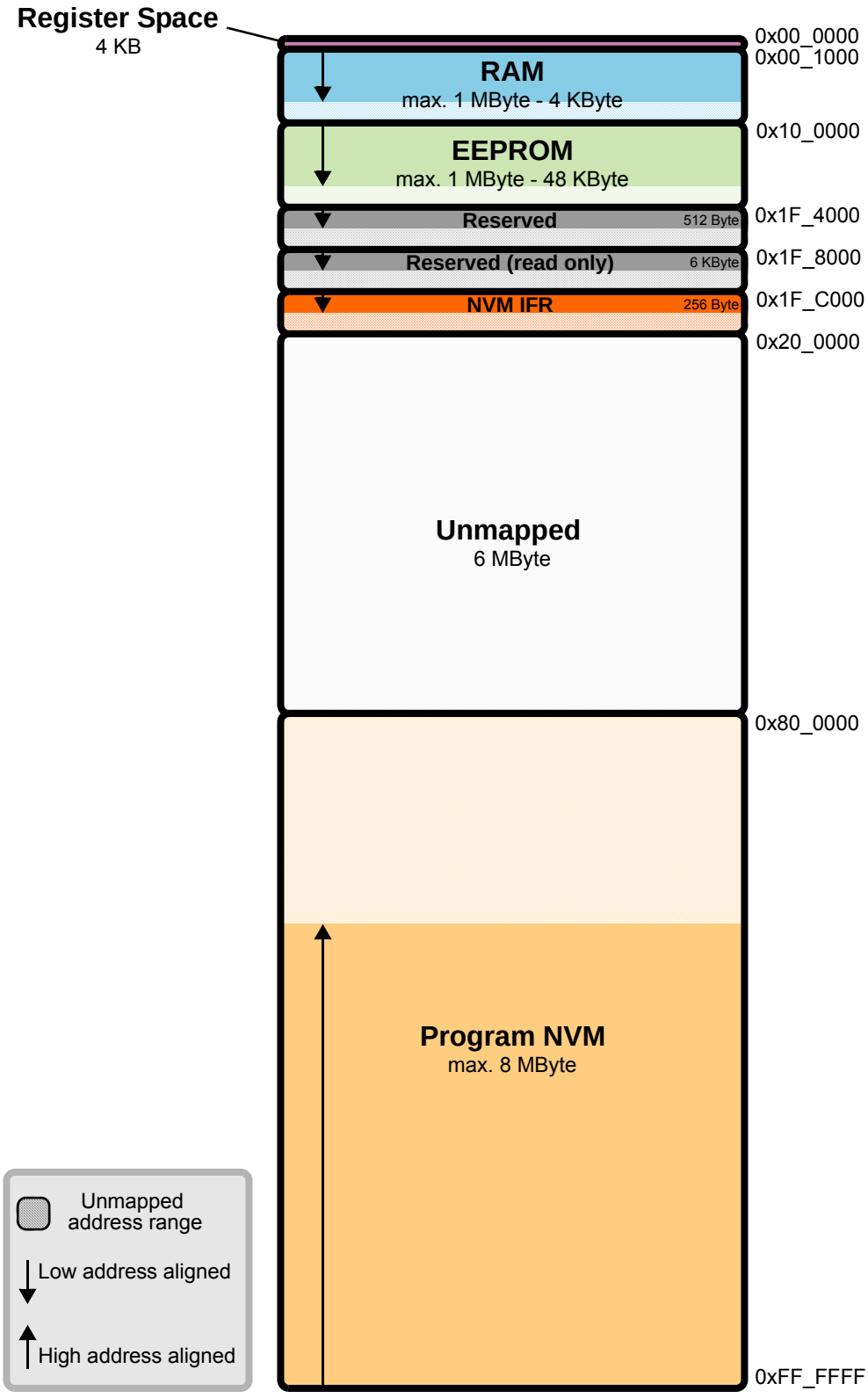


Figure 1-2. MC9S12ZVL-Family Global Memory Map. (See Table 1-2 for individual device details)

Table 1-12. Interrupt Vector Locations (Sheet 2 of 4)

Vector Address[1]	Interrupt Source	CCR Mask	Local Enable	Wake up from STOP	Wake up from WAIT
Vector base + 0x1CC	TIM0 timer channel 0	I bit	TIM0TIE (C0I)	No	Yes
Vector base + 0x1C8	TIM0 timer channel 1	I bit	TIM0TIE (C1I)	No	Yes
Vector base + 0x1C4	TIM0 timer channel 2	I bit	TIM0TIE (C2I)	No	Yes
Vector base + 0x1C0	TIM0 timer channel 3	I bit	TIM0TIE (C3I)	No	Yes
Vector base + 0x1BC	TIM0 timer channel 4	I bit	TIM0TIE (C4I)	No	Yes
Vector base + 0x1B8	TIM0 timer channel 5	I bit	TIM0TIE (C5I)	No	Yes
Vector base + 0x1B4 to Vector base + 0x1B0	Reserved				
Vector base + 0x1AC	TIM0 timer overflow	I bit	TIM0TSCR2(TOI)	No	Yes
Vector base + 0x1A8 to Vector base + 0x1A4	Reserved				
Vector base + 0x1A0	SPI0	I bit	SPI0CR1 (SPIE, SPTIE)	No	Yes
Vector base + 0x19C	SCI0	I bit	SCI0CR2 (TIE, TCIE, RIE, ILIE) SCI0ACR1 (RXEDGIE, BERRIE, BKDIE)	RXEDGIF only	Yes
Vector base + 0x198	SCI1	I bit	SCI1CR2 (TIE, TCIE, RIE, ILIE) SCI1ACR1 (RXEDGIE, BERRIE, BKDIE)	RXEDGIF only	Yes
Vector base + 0x194 to Vector base + 0x190	Reserved				
Vector base + 0x18C	ADC Error	I bit	ADCEIE (IA_EIE, CMD_EIE, EOL_EIE, TRIG_EIE, RSTAR_EIE, LDOK_EIE) ADCIE(CONIF_OIE)	No	Yes
Vector base + 0x188	ADC conversion sequence abort	I bit	ADCIE(SEQAD_IE)	No	Yes
Vector base + 0x184	ADC conversion complete	I bit	ADCCONIE[15:0]	No	Yes
Vector base + 0x180	Oscillator status interrupt	I bit	CPMUINT (OSCIE)	No	Yes
Vector base + 0x17C	PLL lock interrupt	I bit	CPMUINT (LOCKIE)	No	Yes
Vector base + 0x178	ACMP	I bit	ACMPC(ACIE)	No	Yes
Vector base + 0x174 to Vector base + 0x174	Reserved				
Vector base + 0x170	RAM error	I bit	EECIE (SBEEIE)	No	Yes

Chapter 2
Port Integration Module (S12ZVLPIMV2)

Revision History

Rev. No. (Item No.)	Date (Submitted By)	Sections Affected	Substantial Change(s)
V02.10	19 Nov 2014		• Corrected bit descriptions for MODRR1 (PWMn becomes PWM option n). • Removed redundant mention of over-current protection on PP7 in output configuration (already specified in footnote). • Added T0IC3RR1-0 to Routing Register Bits controlling (IOC0_3) on PS1.

2.1 Introduction

2.1.1 Overview

The S12ZVL-family port integration module establishes the interface between the peripheral modules and the I/O pins for all ports. It controls the electrical pin properties as well as the signal prioritization and multiplexing on shared pins.

This document covers:

- 2-pin port E associated with the external oscillator
- 10-pin port AD with pin interrupts and key-wakeup function; associated with 10 ADC channels
- 8-pin port T associated with 8 TIM channels, 1 routed SCI, 1 routed IIC, 2 routed PWM options and 1 ACMP output
- 4-pin port S with pin interrupts and key-wakeup function; associated with 1 SPI, ECLK, 4 routed TIM channels, 2 routed PWM channels, 1 MSCAN and 1 routed SCI
- 8-pin port P with pin interrupts and key-wakeup function or IRQ, XIRQ interrupt inputs; associated with 8 PWM channels and 2 routed TIM channels
- 2-pin port J associated with 1 IIC, 1 routed MSCAN or 2 routed PWM channels
- 1-pin port L with pin interrupts and key-wakeup function; associated with 1 high voltage input (HVI)

Most I/O pins can be configured by register bits to select data direction and to enable and select pull-up or pull-down devices.

Accesses to the internal memory map are not possible when the internal device clocks are disabled. Thus attempted accesses to memory mapped resources are suppressed and the NORESP flag is set. Resources can be accessed again by the next command received following exit from Stop mode.

A BACKGROUND command issued whilst in stop mode remains pending internally until the device leaves stop mode. This means that subsequent active BDM commands, issued whilst BACKGROUND is pending, set the ILLCMD flag because the device is not yet in active BDM.

If ACK handshaking is enabled, then the first ACK, following a stop mode entry is long to indicate a stop exception. The BDC indicates a stop mode occurrence by setting the BDCCSR bit STOP. If the host attempts further communication before the ACK pulse generation then the OVRUN bit is set.

STOP Mode With BDC Enabled And BDCCIS Set

If the BDC is enabled and BDCCIS is set, then the BDC prevents core clocks being disabled in stop mode. This allows BDC communication, for access of internal memory mapped resources, but not CPU registers, to continue throughout stop mode.

A BACKGROUND command issued whilst in stop mode remains pending internally until the device leaves stop mode. This means that subsequent active BDM commands, issued whilst BACKGROUND is pending, set the ILLCMD flag because the device is not yet in active BDM.

If ACK handshaking is enabled, then the first ACK, following a stop mode entry is long to indicate a stop exception. The BDC indicates a stop mode occurrence by setting the BDCCSR bit STOP. If the host attempts further communication before the ACK pulse generation then the OVRUN bit is set.

5.1.3.3.2 Wait Mode

The device enters wait mode when the CPU starts to execute the WAI instruction. The second part of the WAI instruction (return from wait mode) can only be performed when an interrupt occurs. Thus on entering wait mode the CPU is in the middle of the WAI instruction and cannot permit access to CPU internal resources, nor allow entry to active BDM. Thus only commands classified as Non-Intrusive or Always-Available are possible in wait mode.

On entering wait mode, the WAIT flag in BDCCSR is set. If the ACK handshake protocol is enabled then the first ACK generated after WAIT has been set is a long-ACK pulse. Thus the host can recognize a wait mode occurrence. The WAIT flag remains set and cannot be cleared whilst the device remains in wait mode. After the device leaves wait mode the WAIT flag can be cleared by writing a “1” to it.

A BACKGROUND command issued whilst in wait mode sets the NORESP bit and the BDM active request remains pending internally until the CPU leaves wait mode due to an interrupt. The device then enters BDM with the PC pointing to the address of the first instruction of the ISR.

With ACK disabled, further Non-Intrusive or Always-Available commands are possible, in this pending state, but attempted Active-Background commands set NORESP and ILLCMD because the BDC is not in active BDM state.

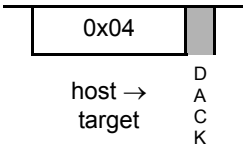
With ACK enabled, if the host attempts further communication before the ACK pulse generation then the OVRUN bit is set.

The ACK_ENABLE command is interpreted and executed in the BDC logic without the need to interface with the CPU. An ACK pulse is issued by the target device after this command is executed. This command can be used by the host to evaluate if the target supports the hardware handshake protocol. If the target supports the hardware handshake protocol, subsequent commands are enabled to execute the hardware handshake protocol, otherwise this command is ignored by the target. Table 5-8 indicates which commands support the ACK hardware handshake protocol.

For additional information about the hardware handshake protocol, refer to Section 5.4.7, “Serial Interface Hardware Handshake (ACK Pulse) Protocol,” and Section 5.4.8, “Hardware Handshake Abort Procedure.”

5.4.4.4 BACKGROUND

Enter active background mode (if enabled) **Non-intrusive**



Provided ENBDC is set, the BACKGROUND command causes the target MCU to enter active BDM as soon as the current CPU instruction finishes. If ENBDC is cleared, the BACKGROUND command is ignored.

A delay of 16 BDCSI clock cycles is required after the BACKGROUND command to allow the target MCU to finish its current CPU instruction and enter active background mode before a new BDC command can be accepted.

The host debugger must set ENBDC before attempting to send the BACKGROUND command the first time. Normally the host sets ENBDC once at the beginning of a debug session or after a target system reset. During debugging, the host uses GO commands to move from active BDM to application program execution and uses the BACKGROUND command or DBG breakpoints to return to active BDM.

A BACKGROUND command issued during stop or wait modes cannot immediately force active BDM because the WAI instruction does not end until an interrupt occurs. For the detailed mode dependency description refer to Section 5.1.3.3, “Low-Power Modes.

The host can recognize this pending BDM request condition because both NORESP and WAIT are set, but BDMACT is clear. Whilst in wait mode, with the pending BDM request, non-intrusive BDC commands are allowed.

5.4.4.5 DUMP_MEM.sz, DUMP_MEM.sz_WS

DUMP_MEM.sz

Read memory specified by debug address register, then increment address **Non-intrusive**

Table 7-8. State1 Match State Sequencer Transitions

CxSC[1:0]	Function
00	Match has no effect
01	Match forces sequencer to State2
10	Match forces sequencer to State3
11	Match forces sequencer to Final State

In the case of simultaneous matches, the match on the higher channel number (3...0) has priority.

7.3.2.4 Debug State Control Register 2 (DBGSCR2)

Address: 0x0108

	7	6	5	4	3	2	1	0
R	C3SC1	C3SC0	0	0	C1SC1	C1SC0	C0SC1	C0SC0
W								
Reset	0	0	0	0	0	0	0	0

Figure 7-7. Debug State Control Register 2 (DBGSCR2)

Read: Anytime.

Write: If DBG is not armed

The state control register 2 selects the targeted next state whilst in State2. The matches refer to the outputs of the comparator match control logic as depicted in Figure 7-1 and described in Section 7.3.2.8, “Debug Comparator A Control Register (DBGACTL)”. Comparators must be enabled by setting the comparator enable bit in the associated DBGXCTL control register.

Table 7-9. DBGSCR2 Field Descriptions

Field	Description
1–0 C0SC[1:0]	Channel 0 State Control. These bits select the targeted next state whilst in State2 following a match0.
3–2 C1SC[1:0]	Channel 1 State Control. These bits select the targeted next state whilst in State2 following a match1.
7–6 C3SC[1:0]	Channel 3 State Control. If EEVE !=10, these bits select the targeted next state whilst in State2 following a match3. If EEVE =10, these bits select the targeted next state whilst in State2 following an external event.

Table 7-10. State2 Match State Sequencer Transitions

CxSC[1:0]	Function
00	Match has no effect
01	Match forces sequencer to State1
10	Match forces sequencer to State3
11	Match forces sequencer to Final State

In the case of simultaneous matches, the match on the higher channel number (3...0) has priority.

Table 9-14. CPMUCOP Field Descriptions

Field	Description
7 WCOP	**Window COP Mode Bit** — When set, a write to the CPMUARMCOP register must occur in the last 25% of the selected period. A write during the first 75% of the selected period generates a COP reset. As long as all writes occur during this window, $55 can be written as often as desired. Once $AA is written after the $55, the time-out logic restarts and the user must wait until the next window before writing to CPMUARMCOP. Table 9-15 shows the duration of this window for the seven available COP rates. 0 Normal COP operation 1 Window COP operation
6 RSBCK	**COP and RTI Stop in Active BDM Mode Bit** 0 Allows the COP and RTI to keep running in Active BDM mode. 1 Stops the COP and RTI counters whenever the part is in Active BDM mode.
5 WRTMASK	**Write Mask for WCOP and CR[2:0] Bit** — This write-only bit serves as a mask for the WCOP and CR[2:0] bits while writing the CPMUCOP register. It is intended for BDM writing the RSBCK without changing the content of WCOP and CR[2:0]. 0 Write of WCOP and CR[2:0] has an effect with this write of CPMUCOP 1 Write of WCOP and CR[2:0] has no effect with this write of CPMUCOP. (Does not count for “write once”.)
2–0 CR[2:0]	**COP Watchdog Timer Rate Select** — These bits select the COP time-out rate (see Table 9-15 and Table 9-16). Writing a nonzero value to CR[2:0] enables the COP counter and starts the time-out period. A COP counter time-out causes a System Reset. This can be avoided by periodically (before time-out) initializing the COP counter via the CPMUARMCOP register. While all of the following four conditions are true the CR[2:0], WCOP bits are ignored and the COP operates at highest time-out period (2^{24} cycles) in normal COP mode (Window COP mode disabled): 1) COP is enabled (CR[2:0] is not 000) 2) BDM mode active 3) RSBCK = 0 4) Operation in Special Mode

Table 9-15. COP Watchdog Rates if COPOSCSEL1=0. (default out of reset)

CR2	CR1	CR0	COPCLK Cycles to time-out (COPCLK is either IRCCLK or OSCCLK depending on the COPOSCSEL0 bit)
0	0	0	COP disabled
0	0	1	2^{14}
0	1	0	2^{16}
0	1	1	2^{18}
1	0	0	2^{20}
1	0	1	2^{22}
1	1	0	2^{23}
1	1	1	2^{24}

10.5.2.3 ADC Status Register (ADCSTS)

It is important to note that if flag DBECC_ERR is set the ADC ceases operation. In order to make the ADC operational again an ADC Soft-Reset must be issued. An ADC Soft-Reset clears bits CSL_SEL and RVL_SEL.

Module Base + 0x0002

	7	6	5	4	3	2	1	0
R	CSL_SEL	RVL_SEL	DBECC_ERR	Reserved	READY	0	0	0
W								
Reset	0	0	0	0	1	0	0	0

= Unimplemented or Reserved

Figure 10-6. ADC Status Register (ADCSTS)

Read: Anytime

Write:

- Bits CSL_SEL and RVL_SEL anytime if bit ADC_EN is clear or bit SMOD_ACC is set
- Bits DBECC_ERR and READY not writable

Table 10-6. ADCSTS Field Descriptions

Field	Description
7 CSL_SEL	**Command Sequence List Select bit** — This bit controls and indicates which ADC Command List is active. This bit can only be written if ADC_EN bit is clear. This bit toggles in CSL double buffer mode when no conversion or conversion sequence is ongoing and bit LDOK is set and bit RSTA is set. In CSL single buffer mode this bit is forced to 1'b0 by bit CSL_BMOD. 0 ADC Command List 0 is active. 1 ADC Command List 1 is active.
6 RVL_SEL	**Result Value List Select Bit** — This bit controls and indicates which ADC Result List is active. This bit can only be written if bit ADC_EN is clear. After storage of the initial Result Value List this bit toggles in RVL double buffer mode whenever the conversion result of the first conversion of the current CSL is stored or a CSL got aborted. In RVL single buffer mode this bit is forced to 1'b0 by bit RVL_BMOD. Please see also Section 10.3.1.2, "MCU Operating Modes for information regarding Result List usage in case of Stop or Wait Mode. 0 ADC Result List 0 is active. 1 ADC Result List 1 is active.
5 DBECC_ERR	**Double Bit ECC Error Flag** — This flag indicates that a double bit ECC error occurred during conversion command load or result storage and ADC ceases operation. In order to make the ADC operational again an ADC Soft-Reset must be issued. This bit is cleared if bit ADC_EN is clear. 0 No double bit ECC error occurred. 1 A double bit ECC error occurred.
3 READY	**Ready For Restart Event Flag** — This flag indicates that ADC is in its idle state and ready for a Restart Event. It can be used to verify after exit from Wait Mode if a Restart Event can be issued and processed immediately without any latency time due to an ongoing Sequence Abort Event after exit from MCU Wait Mode (see also the Note in Section 10.3.1.2, "MCU Operating Modes). 0 ADC not in idle state. 1 ADC is in idle state.

Table 10-11. Summary of Conversion Flow Control Bit Scenarios

RSTA	TRIG	SEQA	LDOK	Conversion Flow Control Mode	Conversion Flow Control Scenario
0	0	0	0	Both Modes	Valid
0	0	0	1	Both Modes	Can Not Occur
0	0	1	0	Both Modes	Valid[5]
0	0	1	1	Both Modes	Can Not Occur
0	1	0	0	Both Modes	Valid[2]
0	1	0	1	Both Modes	Can Not Occur
0	1	1	0	Both Modes	Can Not Occur
0	1	1	1	Both Modes	Can Not Occur
1	0	0	0	Both Modes	Valid[4]
1	0	0	1	Both Modes	Valid[1 4]
1	0	1	0	Both Modes	Valid[3 4 5]
1	0	1	1	Both Modes	Valid[1 3 4 5]
1	1	0	0	“Restart Mode”	Error flag TRIG_EIF set
				“Trigger Mode”	Valid[2 4 6]
1	1	0	1	“Restart Mode”	Error flag TRIG_EIF set
				“Trigger Mode”	Valid[1 2 4 6]
1	1	1	0	“Restart Mode”	Error flag TRIG_EIF set
				“Trigger Mode”	Valid[2 3 4 5 6]
1	1	1	1	“Restart Mode”	Error flag TRIG_EIF set
				“Trigger Mode”	Valid[1 2 3 4 5 6]

1 Swap CSL buffer
2 Start conversion sequence
3 Prevent RSTA_EIF and LDOK_EIF
4 Load conversion command from top of CSL
5 Abort any ongoing conversion, conversion sequence and CSL
6 Bit TRIG set automatically in Trigger Mode

For a detailed description of all conversion flow control bit scenarios please see also Section 10.6.3.2.4, “The two conversion flow control Mode Configurations, Section 10.6.3.2.5, “The four ADC conversion flow control bits and Section 10.6.3.2.6, “Conversion flow control in case of conversion sequence control bit overrun scenarios

Chapter 12
Programmable Gain Amplifier (PGAV1)

12.1 Revision History

Table 12-1. Revision History Table

Rev. No. (Item No.)	Data	Sections Affected	Substantial Change(s)
1.0	05-May.-15	Figure 12-8	updated Figure 12-8
1.1	13-May.-15	Figure 12-2	correct read values of reserved registers Figure 12-2

Glossary

Table 12-2. Terminology

Term	Meaning
PGA	Programmable Gain Amplifier

12.2 Introduction

The PGA module is programmable gain amplifier. Figure 12-1 shows the block diagram. Please refer to device specification for the mapping and connectivity of the PGA module pins.

12.2.1 Features

The PGA will be operated from the analog 5V power domain VDDA.

- Amplification of analog input signal with selectable gain of 10x, 20x, 40x, 80x
- Typical current consumption 1mA
- Offset compensation
- Internal V_{DDA} / 2 reference voltage generation or external signal as reference voltage (see top level connections)
- Amplifier output connected to ADC

12.2.2 Modes of Operation

The PGA module behaves as follows in the system power modes:

1. CPU run mode

   The functionality of the PGA module is available.

Address Offset / Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0002 PGAGAIN	R	0	0	0	0	PGAGAIN[3:0]			
	W								
0x0003 PGAOFFSET	R	0		PGAOFFSET[5:0]					
	W								
0x0004-0x0006 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0007 Reserved	R	0	0	0	0	0	Reserved	Reserved	Reserved
	W								

= Unimplemented

Figure 12-2. PGA Register Summary

12.3.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

12.3.2.1 PGA Enable Register (PGAEN)

Module Base + 0x0000 — Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0		PGAOFFSCEN	PGAEN
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 12-3. PGA Enable Register (PGAEN)

[1] Read: Anytime
Write: Anytime

16.3.2.12 Timer Input Capture/Output Compare Registers High and Low 0–1(TCxH and TCxL)

Module Base +	0x0010 = TC0H	0x0018=RESERVD
	0x0012 = TC1H	0x001A=RESERVD
	0x0014=RESERVD	0x001C=RESERVD
	0x0016=RESERVD	0x001E=RESERVD

	15	14	13	12	11	10	9	0
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset	0	0	0	0	0	0	0	0

Figure 16-18. Timer Input Capture/Output Compare Register x High (TCxH)

Module Base +	0x0011 = TC0L	0x0019 =RESERVD
	0x0013 = TC1L	0x001B=RESERVD
	0x0015 =RESERVD	0x001D=RESERVD
	0x0017=RESERVD	0x001F=RESERVD

	7	6	5	4	3	2	1	0
R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 16-19. Timer Input Capture/Output Compare Register x Low (TCxL)

[1] This register is available only when the corresponding channel exists and is reserved if that channel does not exist. Writes to a reserved register have no functional effect. Reads from a reserved register return zeroes.

Depending on the TIOS bit for the corresponding channel, these registers are used to latch the value of the free-running counter when a defined transition is sensed by the corresponding input capture edge detector or to trigger an output action for output compare.

Read: Anytime

Write: Anytime for output compare function.Writes to these registers have no meaning or effect during input capture. All timer input capture/output compare registers are reset to 0x0000.

NOTE

Read/Write access in byte mode for high byte should take place before low byte otherwise it will give a different result.

In this way, the output of the PWM will always be either the old waveform or the new waveform, not some variation in between. If the channel is not enabled, then writes to the period register will go directly to the latches as well as the buffer.

NOTE

Reads of this register return the most recent value written. Reads do not necessarily return the value of the currently active period due to the double buffering scheme.

See Section 17.4.2.3, “PWM Period and Duty” for more information.

To calculate the output period, take the selected clock source period for the channel of interest (A, B, SA, or SB) and multiply it by the value in the period register for that channel:

- Left aligned output (CAEx = 0)

  PWMx Period = Channel Clock Period * PWMPERx
- Center Aligned Output (CAEx = 1)

  PWMx Period = Channel Clock Period * (2 * PWMPERx)

For boundary case programming values, please refer to Section 17.4.2.8, “PWM Boundary Cases”.

Module Base + 0x0014 = PWMPER0, 0x0015 = PWMPER1, 0x0016 = PWMPER2, 0x0017 = PWMPER3
Module Base + 0x0018 = PWMPER4, 0x0019 = PWMPER5, 0x001A = PWMPER6, 0x001B = PWMPER7

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	1	1	1	1	1	1	1	1

Figure 17-13. PWM Channel Period Registers (PWMPERx)

[1] This register is available only when the corresponding channel exists and is reserved if that channel does not exist. Writes to a reserved register have no functional effect. Reads from a reserved register return zeroes.

Read: Anytime

Write: Anytime

17.3.2.12 PWM Channel Duty Registers (PWMDTYx)

There is a dedicated duty register for each channel. The value in this register determines the duty of the associated PWM channel. The duty value is compared to the counter and if it is equal to the counter value a match occurs and the output changes state.

The duty registers for each channel are double buffered so that if they change while the channel is enabled, the change will NOT take effect until one of the following occurs:

- The effective period ends
- The counter is written (counter resets to $00)
- The channel is disabled

The SCI also sets a flag, the transmit data register empty flag (TDRE), every time it transfers data from the buffer (SCIDRH/L) to the transmitter shift register.The transmit driver routine may respond to this flag by writing another byte to the Transmitter buffer (SCIDRH/SCIDRL), while the shift register is still shifting out the first byte.

To initiate an SCI transmission:

1. Configure the SCI:
   a) Select a baud rate. Write this value to the SCI baud registers (SCIBDH/L) to begin the baud rate generator. Remember that the baud rate generator is disabled when the baud rate is zero. Writing to the SCIBDH has no effect without also writing to SCIBDL.
   b) Write to SCICR1 to configure word length, parity, and other configuration bits (LOOPS,RSRC,M,WAKE,ILT,PE,PT).
   c) Enable the transmitter, interrupts, receive, and wake up as required, by writing to the SCICR2 register bits (TIE,TCIE,RIE,ILIE,TE,RE,RWU,SBK). A preamble or idle character will now be shifted out of the transmitter shift register.
2. Transmit Procedure for each byte:
   a) Poll the TDRE flag by reading the SCISR1 or responding to the TDRE interrupt. Keep in mind that the TDRE bit resets to one.
   b) If the TDRE flag is set, write the data to be transmitted to SCIDRH/L, where the ninth bit is written to the T8 bit in SCIDRH if the SCI is in 9-bit data format. A new transmission will not result until the TDRE flag has been cleared.
3. Repeat step 2 for each subsequent transmission.

NOTE

The TDRE flag is set when the shift register is loaded with the next data to be transmitted from SCIDRH/L, which happens, generally speaking, a little over half-way through the stop bit of the previous frame. Specifically, this transfer occurs 9/16ths of a bit time AFTER the start of the stop bit of the previous frame.

Writing the TE bit from 0 to a 1 automatically loads the transmit shift register with a preamble of 10 logic 1s (if M = 0) or 11 logic 1s (if M = 1). After the preamble shifts out, control logic transfers the data from the SCI data register into the transmit shift register. A logic 0 start bit automatically goes into the least significant bit position of the transmit shift register. A logic 1 stop bit goes into the most significant bit position.

Hardware supports odd or even parity. When parity is enabled, the most significant bit (MSB) of the data character is the parity bit.

The transmit data register empty flag, TDRE, in SCI status register 1 (SCISR1) becomes set when the SCI data register transfers a byte to the transmit shift register. The TDRE flag indicates that the SCI data register can accept new data from the internal data bus. If the transmit interrupt enable bit, TIE, in SCI control register 2 (SCICR2) is also set, the TDRE flag generates a transmitter interrupt request.

To determine the value of a data bit and to detect noise, recovery logic takes samples at RT8, RT9, and RT10. Table 18-18 summarizes the results of the data bit samples.

Table 18-18. Data Bit Recovery

RT8, RT9, and RT10 Samples	Data Bit Determination	Noise Flag
000	0	0
001	0	1
010	0	1
011	1	1
100	0	1
101	1	1
110	1	1
111	1	0

NOTE

The RT8, RT9, and RT10 samples do not affect start bit verification. If any or all of the RT8, RT9, and RT10 start bit samples are logic 1s following a successful start bit verification, the noise flag (NF) is set and the receiver assumes that the bit is a start bit (logic 0).

To verify a stop bit and to detect noise, recovery logic takes samples at RT8, RT9, and RT10. Table 18-19 summarizes the results of the stop bit samples.

Table 18-19. Stop Bit Recovery

RT8, RT9, and RT10 Samples	Framing Error Flag	Noise Flag
000	1	0
001	1	1
010	1	1
011	0	1
100	1	1
101	0	1
110	0	1
111	0	0

In Figure 18-22 the verification samples RT3 and RT5 determine that the first low detected was noise and not the beginning of a start bit. The RT clock is reset and the start bit search begins again. The noise flag is not set because the noise occurred before the start bit was found.

Offset Module Base + 0x0016

	7	6	5	4	3	2	1	0
R W	CCOB[15:8]							
Reset	0	0	0	0	0	0	0	0

Figure 22-28. Flash Common Command Object 5 High Register (FCCOB5HI)

Offset Module Base + 0x0017

	7	6	5	4	3	2	1	0
R W	CCOB[7:0]							
Reset	0	0	0	0	0	0	0	0

Figure 22-29. Flash Common Command Object 5 Low Register (FCCOB5LO)

22.3.2.13.1 FCCOB - NVM Command Mode

NVM command mode uses the FCCOB registers to provide a command code and its relevant parameters to the Memory Controller. The user first sets up all required FCCOB fields and then initiates the command's execution by writing a 1 to the CCIF bit in the FSTAT register (a 1 written by the user clears the CCIF command completion flag to 0). When the user clears the CCIF bit in the FSTAT register all FCCOB parameter fields are locked and cannot be changed by the user until the command completes (as evidenced by the Memory Controller returning CCIF to 1). Some commands return information to the FCCOB register array.

The generic format for the FCCOB parameter fields in NVM command mode is shown in Table 22-26. The return values are available for reading after the CCIF flag in the FSTAT register has been returned to 1 by the Memory Controller. The value written to the FCCOBIX field must reflect the amount of CCOB words loaded for command execution.

Table 22-26 shows the generic Flash command format. The high byte of the first word in the CCOB array contains the command code, followed by the parameters for this specific Flash command. For details on the FCCOB settings required by each command, see the Flash command descriptions in Section 22.4.7.

Table 22-26. FCCOB - NVM Command Mode (Typical Usage)

CCOBIX[2:0]	Register	Byte	FCCOB Parameter Fields (NVM Command Mode)
000	FCCOB0	HI	FCMD[7:0] defining Flash command
		LO	Global address [23:16]
001	FCCOB1	HI	Global address [15:8]
		LO	Global address [7:0]
010	FCCOB2	HI	Data 0 [15:8]
		LO	Data 0 [7:0]

Table B-1. Voltage Regulator Electrical Characteristics

-40°C ≤T_J ≤ 175°C unless noted otherwise, V_{DDA} and V_{DDX} must be shorted on the application board.						
Num	**Characteristic**	**Symbol**	**Min**	**Typical**	**Max**	**Unit**
VDDX=3.3V, VREG5VEN = 1'b0, ZVL(A)128/96/64 only						
6a	Output Voltage V_{DDX}, with external PNP Full Performance Mode V_{SUP} >5.5V[1] Full Performance Mode V_{SUP} >5.5V[4] Full Performance Mode 3.5V <= V_{SUP} <=5.5V Reduced Performance Mode (stopmode) V_{SUP} > =3.5V	V_{DDX}	 3.2 3.23 3.13 2.2	 3.3 3.3 - 3.3	 3.39 3.36 3.39 3.6	V
6b	Output Voltage V_{DDX}, without PNP Full Performance Mode V_{SUP} >5.5V[1] Full Performance Mode V_{SUP} >5.5V[4] Full Performance Mode 3.5V <= V_{SUP} <=5.5V Reduced Performance Mode (stopmode) V_{SUP} > =3.5V	V_{DDX}	 3.18 3.21 3.13 2.2	 3.28 3.28 - 3.3	 3.37 3.35 3.37 3.6	V
7	Load Current V_{DDX}[2,3] without external PNP Full Performance Mode V_{SUP} > 5.5V Full Performance Mode 3.5V <= V_{SUP} <=5.5V Reduced Performance Mode (stopmode)	I_{DDX}	 0 0 0	 - - -	 70 25 5	mA
8	Short Circuit V_{DDX} fall back current V_{DDX} <= 0.5V	I_{DDX}	—	100	—	mA
9	Low Voltage Interrupt Assert Level[5] Low Voltage Interrupt Deassert Level	V_{LVIA} V_{LVID}	4.04 4.19	4.23 4.38	4.40 4.49	V
10a	V_{DDX} Low Voltage Reset deassert[6]	V_{LVRXD}	—	—	3.13	V
10b	V_{DDX} Low Voltage Reset assert	V_{LVRXA}	2.95	3.02	—	V
11	Trimmed ACLK output frequency[7]	f_{ACLK}	—	20	—	KHz
12	Trimmed ACLK internal clock Δf / $f_{nominal}$ [8]	df_{ACLK}	- 6%	—	+ 6%	—
13	The first period after enabling the counter by APIFE might be reduced by API start up delay	t_{sdel}	—	—	100	µs
14	Temperature Sensor Slope	dV_{HT}	5.05	5.25	5.45	mV/°C
15	Temperature Sensor Output Voltage (T_j=150°C)	V_{HT}	—	2.4	—	V
16	High Temperature Interrupt Assert[9] High Temperature Interrupt Deassert	T_{HTIA} T_{HTID}	120 110	132 122	144 134	°C °C
17	Bandgap output voltage	V_{BG}	1.14	1.20	1.28	V
18	V_{BG} voltage variation over input voltage V_{SUP} 3.5V ≤ V_{SUP} ≤ 18V, T_J = 125°C	Δ_{VBGV}	-5		5	mV

NOTE

On timers and serial modules a prescaler will eliminate the effect of the jitter to a large extent.

Table B-5. ipll_1vdd_ll18 Characteristics

Conditions are: MC9S12ZVL(S)32\16\8: 3.13V ≤ V_{DDX} ≤ 5.5V, MC9S12ZVL(A)128\96\64: 3.2V ≤ V_{DDX} ≤ 5.15V, junction temperature from –40°C to +175°C, unless otherwise noted						
Num	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	VCO frequency during system reset	f_{VCORST}	8	—	32	MHz
2	VCO locking range	f_{VCO}	32	—	64	MHz
3	Reference Clock	f_{REF}	1	—	—	MHz
4	Lock Detection	$\|\Delta_{Lock}\|$	0	—	1.5	%[1]
5	Un-Lock Detection	$\|\Delta_{unl}\|$	0.5	—	2.5	%[1]
7	Time to lock	t_{lock}	—	—	150 + 256/f_{REF}	µs
8	Jitter fit parameter 1[2]	j_1	—	—	2	%
9	PLL Clock Monitor Failure assert frequency	f_{PMFA}	0.45	0.8	1.6	MHz

1 % deviation from target frequency

2 f_{REF} = 1MHz, f_{BUS} = 32MHz

Appendix I
ACMP Electrical Specifications

This section describe the electrical characteristics of the analog comparator module.

I.1 Maximum Ratings

Table I-1. Maximum Ratings of the analog comparator - ACMP

Characteristics noted under conditions 3.20V ≤ V_{DDA} ≤ 5.15V, -40°C ≤ T_J ≤ 175°C[1] unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C[2] under nominal conditions unless otherwise noted.						
Num	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	Max Rating (relative to supply)	V_{ACMP_MAX}	-0.3	–	VDDA +0.3	V
	Max Rating (absolute) V_{ACMP_0} V_{ACMP_1} V_{acmpi_0} V_{acmpi_1}	V_{ACMP_MAXA}	-0.3	–	6	V

1 T_J: Junction Temperature

2 T_A: Ambient Temperature

I.2 Static Electrical Characteristics

Table I-2. Static Electrical Characteristics of the analog comparator - ACMP

Characteristics noted under conditions 3.20V ≤ V_{DDA} ≤ 5.15V, -40°C ≤ T_J ≤ 175°C[1] unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C[2] under nominal conditions unless otherwise noted.						
Num	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
2	Supply Current of ACMP T_J ≤ 150°C • Module disabled • Module enabled ΔV_{in} > 5*V_{hyst}	 I_{ACMP_off} I_{ACMP_run}	 - 80	 - -	 3 180	 µA µA
3	Supply Current of ACMP 150°C <T_J ≤ 175°C • Module disabled • Module enabled ΔV_{in} > 5*V_{hyst}	 I_{ACMP_off} I_{ACMP_run}	 - 80	 - -	 5 180	 µA µA
4	Pad Input Current in V_{ACMP_in} range • -40°C ≤ T_J ≤ 80°C • -40°C ≤ T_J ≤ 150°C • -40°C ≤ T_J ≤ 175°C For 0V < V_{pad_in} < V_{DDA}	$I_{ACMP\_pad\_in}$	 -1 -2 -3	 - - -	 1 2 3	 µA µA µA
5	Input Offset • -40°C ≤ T_J ≤ 175°C	V_{ACMP_offset}	-25	0	25	mV

O.11 0x05C0-0x05FF TIM0 (continued)

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x05C5	TIM0TCNTL	R W	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0
0x05C6	TIM0TSCR1	R W	TEN	TSWAI	TSFRZ	TFFCA	PRNT	0	0	0
0x05C7	TIM0TTOV	R W	RESERVED	RESERVED	TOV5	TOV4	TOV3	TOV2	TOV1	TOV0
0x05C8	TIM0TCTL1	R W	RESERVED	RESERVED	RESERVED	RESERVED	OM5	OL5	OM4	OL4
0x05C9	TIM0TCTL2	R W	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
0x05CA	TIM0TCTL3	R W	RESERVED	RESERVED	RESERVED	RESERVED	EDG5B	EDG5A	EDG4B	EDG4A
0x05CB	TIM0TCTL4	R W	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
0x05CC	TIM0TIE	R W	RESERVED	RESERVED	C5I	C4I	C3I	C2I	C1I	C0I
0x05CD	TIM0TSCR2	R W	TOI	0	0	0	RESERVED	PR2	PR1	PR0
0x05CE	TIM0TFLG1	R W	RESERVED	RESERVED	C5F	C4F	C3F	C2F	C1F	C0F
0x05CF	TIM0TFLG2	R W	TOF	0	0	0	0	0	0	0
0x05D0	TIM0TC0H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x05D1	TIM0TC0L	R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05D2	TIM0TC1H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x05D3	TIM0TC1L	R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05D4	TIM0TC2H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x05D5	TIM0TC2L	R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05D6	TIM0TC3H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8