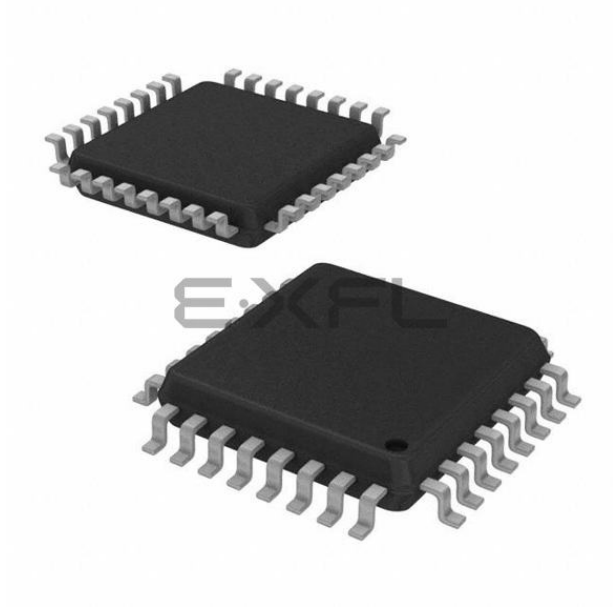

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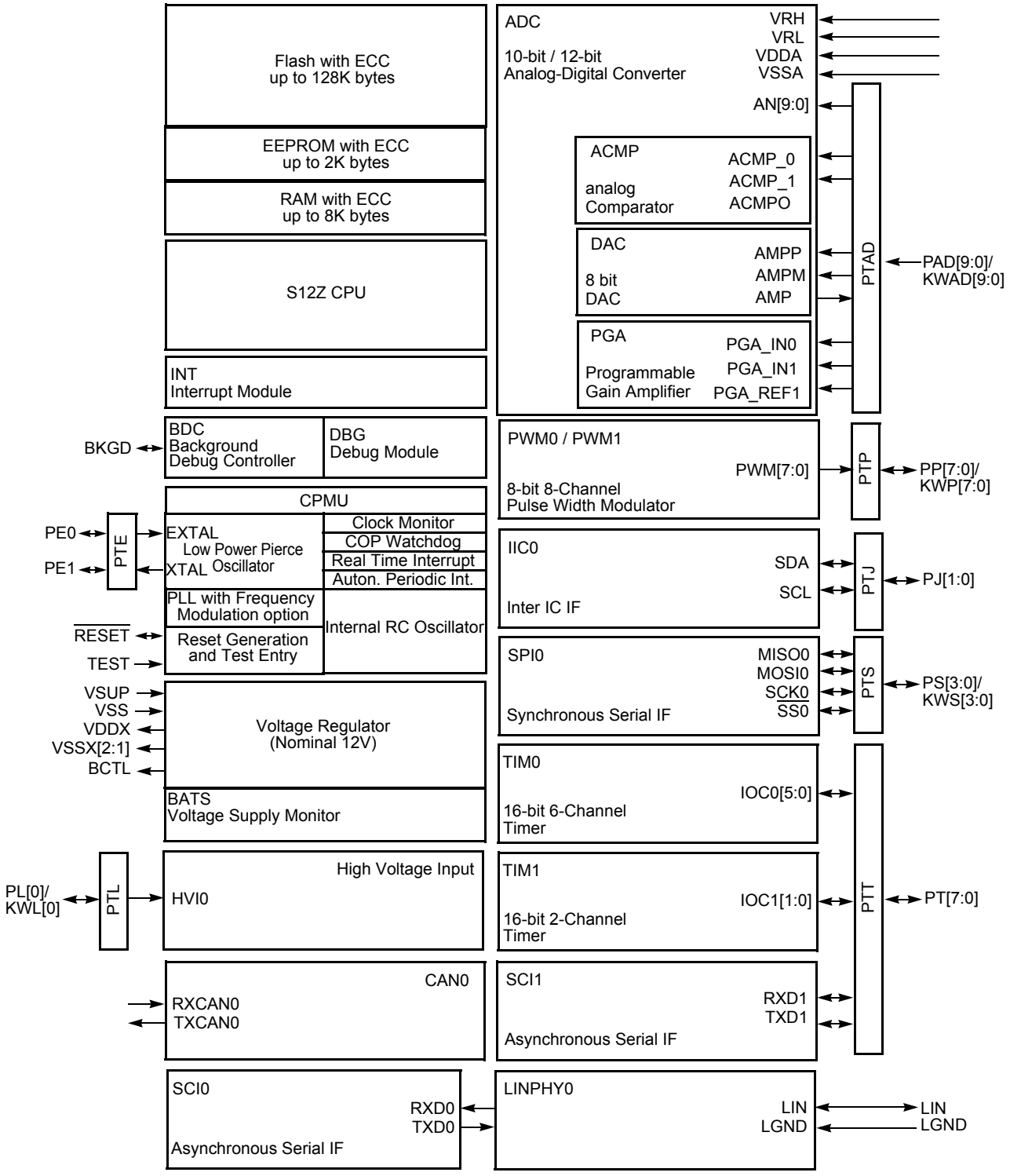
Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SCI, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	19
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	5.5V ~ 18V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvl64f0vlc

Revision History

Date	Revision Level	Description
13 May 2015	2.00 Draft E	• Added new version of Chapter 12, “Programmable Gain Amplifier (PGAV1) • Added new version of Chapter 11, “Digital Analog Converter (DAC_8B5V_V2) • added missing modules DAC, PGA, ACMP, PWM1 to Appendix O, “Detailed Register Address Map • update voltage range inside Appendix I, “ACMP Electrical Specifications and Appendix G, “DAC_8B5V Electrical Specifications
05 June 2015	2.00 Draft F	• Added new version of Chapter 1, “Device Overview MC9S12ZVL-Family” • Added new version of Appendix A, “MCU Electrical Specifications
27 October 2015	2.00 Draft G	• Added new version v0.4 of Appendix A, “MCU Electrical Specifications” • correct Order Information
25 February 2016	2.00Draft I	• change to NXP style • Added new version of Appendix A, “MCU Electrical Specifications
10 May 2016	2.00	• Added version 0.80 of Appendix A, “MCU Electrical Specifications • changed to Chapter 10, “Analog-to-Digital Converter (ADC12B_LBA) version V3
08 August 2017	2.10	• Added version 0.90 of Appendix A, “MCU Electrical Specifications • Added version 2.00 of Chapter 1, “Device Overview MC9S12ZVL-Family
12 September 2017	2.20	• Added version 1.0 of Appendix A, “MCU Electrical Specifications
10 October 2017	2.30	• Added version 1.1 of Appendix A, “MCU Electrical Specifications
19 October 2017	2.40	• Added version 1.2 of Appendix A, “MCU Electrical Specifications
24 October 2017	2.41	• Added version 1.21 of Appendix A, “MCU Electrical Specifications

1.5 Block Diagram



Block Diagram shows the maximum configuration
Not all pins or all peripherals are available on all devices and packages.
Rerouting options are not shown.

Figure 1-1. MC9S12ZVL-Family Block Diagram

COP is stopped during Full Stop Mode and COP continues to operate after exit from Full Stop Mode. For this COP configuration (ACLK clock source, CSAD set) a latency time (please refer to CSAD bit description for details) occurs when entering or exiting (Full, Pseudo) Stop Mode. When bit CSAD is clear the ACLK clock source is on for the COP during Full Stop Mode and COP is operating.
During Full Stop Mode the RTI counter halts.
After wake-up from Full Stop Mode the Core Clock and Bus Clock are running on PLLCLK (PLLSEL=1). The COP runs on ACLK and RTI is running on IRCCLK (COPOSCSEL0=0, RTIOSCSEL=0).

- **Pseudo Stop Mode (PSTP = 1 and OSCE=1)**
  External oscillator (XOSCLCP) continues to run.
  - If COPOSCSEL1=0:
    If the respective enable bits are set (PCE=1 and PRE=1) the COP and RTI will continue to run with a clock derived from the oscillator clock.
    The clock configuration bits PLLSEL, COPOSCSEL0, RTIOSCSEL are unchanged.
  - If COPOSCSEL1=1:
    If the respective enable bit for the RTI is set (PRE=1) the RTI will continue to run with a clock derived from the oscillator clock.
    The clock for the COP is derived from ACLK (trimmable internal RC-Oscillator clock). During Pseudo Stop Mode the ACLK for the COP can be stopped (COP static) or running (COP active) depending on the setting of bit CSAD. When bit CSAD is set the ACLK for the COP is stopped during Pseudo Stop Mode and COP continues to operate after exit from Pseudo Stop Mode. For this COP configuration (ACLK clock source, CSAD set) a latency time (please refer to CSAD bit description for details) occurs when entering or exiting (Pseudo, Full) Stop Mode. When bit CSAD is clear the ACLK clock source is on for the COP during Pseudo Stop Mode and COP is operating.
    The clock configuration bits PLLSEL, COPOSCSEL0, RTIOSCSEL are unchanged.

NOTE

When starting up the external oscillator (either by programming OSCE bit to 1 or on exit from Full Stop Mode with OSCE bit already 1) the software must wait for a minimum time equivalent to the startup-time of the external oscillator t_{UPOSC} before entering Pseudo Stop Mode.

9.1.2.4 Freeze Mode (BDM active)

For S12CPMU_UHV Freeze Mode is the same as Run Mode except for RTI and COP which can be frozen in Active BDM Mode with the RSBCK bit in the CPMUCOP register. After exiting BDM Mode RTI and COP will resume its operations starting from this frozen status.

Additionally the COP can be forced to the maximum time-out period in Active BDM Mode. For details please see also the RSBCK and CR[2:0] bit description field of Table 9-14 in Section 9.3.2.12, “S12CPMU_UHV COP Control Register (CPMUCOP)

This supply domain is monitored by the Low Voltage Reset circuit.

VDDX has to be connected externally to VDDA.

9.2.6 BCTL — Base Control Pin for external PNP

BCTL is the ballast connection for the on chip voltage regulator. It provides the base current of an external

BJT (PNP) of the VDDX and VDDA supplies. An additional 1KΩ resistor between emitter and base of the BJT is required. See the device specification if this pin is available on this device.

9.2.7 VSS — Core Logic Ground Pin

VSS is the core logic supply return pin. It must be grounded.

9.2.8 VDD — Internal Regulator Output Supply (Core Logic)

Node VDD is a device internal supply output of the voltage regulator that provides the power supply for the internal core logic.

This supply domain is monitored by the Low Voltage Reset circuit and The Power On Reset circuit.

9.2.9 VDDF — Internal Regulator Output Supply (NVM Logic)

Node VDDF is a device internal supply output of the voltage regulator that provides the power supply for the NVM logic.

This supply domain is monitored by the Low Voltage Reset circuit.

9.2.10 API_EXTCLK — API external clock output pin

This pin provides the signal selected via APIES and is enabled with APIEA bit. See the device specification if this clock output is available on this device and to which pin it might be connected.

9.2.11 TEMPSENSE — Internal Temperature Sensor Output Voltage

Depending on the VSEL setting either the voltage level generated by the temperature sensor or the VREG bandgap voltage is driven to a special channel input of the ADC Converter. See device level specification for connectivity of ADC special channels.

9.3.2 Register Descriptions

This section describes all the S12CPMU_UHV registers and their individual bits.

Address order is as listed in Figure 9-3

9.3.2.1 Reserved Register CPMUVREGTRIM0

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in Special Mode can alter the S12CPMU_UHV's functionality.

.

Module Base + 0x0001

	7	6	5	4	3	2	1	0
R	0	0	0	0	U			
W								
Reset	0	0	0	0	F	F	F	F
Power on Reset	0	0	0	0	0	0	0	0

Note: After de-assert of System Reset a value is automatically loaded from the Flash memory.

Figure 9-4. Reserved Register (CPMUVREGTRIM0)

Read: Anytime

Write: Only in Special Mode

9.3.2.2 Reserved Register CPMUVREGTRIM1

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in Special Mode can alter the S12CPMU_UHV's functionality.

.

9.3.2.25 S12CPMU_UHV Protection Register (CPMUPROT)

This register protects the following important configuration registers from accidental overwrite:

CPMUSYNR, CPMUREFDIV, CPMUCLKS, CPMUPLL, CPMUIRCTRIMH/L, CPMUOSC and CPMUOSC2

Module Base + 0x001B

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	PROT
W								
Reset	0	0	0	0	0	0	0	0

Figure 9-34. S12CPMU_UHV Protection Register (CPMUPROT)

Read: Anytime

Write: Anytime

Field	Description
PROT	**Clock Configuration Registers Protection Bit** — This bit protects the clock and voltage regulator configuration registers from accidental overwrite (see list of protected registers above): Writing 0x26 to the CPMUPROT register clears the PROT bit, other write accesses set the PROT bit. 0 Protection of clock and voltage regulator configuration registers is disabled. 1 Protection of clock and voltage regulator configuration registers is enabled. (see list of protected registers above).

10.5.2.2 ADC Control Register 1 (ADCCTL_1)

Module Base + 0x0001

	7	6	5	4	3	2	1	0
R	CSL_BMOD	RVL_BMOD	SMOD_ACC	AUT_RSTA	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 10-5. ADC Control Register 1 (ADCCTL_1)

Read: Anytime

Write:

- Bit CSL_BMOD and RVL_BMOD writable if bit ADC_EN clear or bit SMOD_ACC set
- Bit SMOD_ACC only writable in MCU Special Mode
- Bit AUT_RSTA writable anytime

Table 10-5. ADCCTL_1 Field Descriptions

Field	Description
7 CSL_BMOD	**CSL Buffer Mode Select Bit** — This bit defines the CSL buffer mode. This bit is only writable if ADC_EN is clear. 0 CSL single buffer mode. 1 CSL double buffer mode.
6 RVL_BMOD	**RVL Buffer Mode Select Bit** — This bit defines the RVL buffer mode. 0 RVL single buffer mode 1 RVL double buffer mode
5 SMOD_ACC	**Special Mode Access Control Bit** — This bit controls register access rights in MCU Special Mode. This bit is automatically cleared when leaving MCU Special Mode. Note: When this bit is set also the ADCCMD register is writeable via the data bus to allow modification of the current command for debugging purpose. But this is only possible if the current command is not already processed (conversion not started). Please see access details given for each register. Care must be taken when modifying ADC registers while bit SMOD_ACC is set to not corrupt a possible ongoing conversion. 0 Normal user access - Register write restrictions exist as specified for each bit. 1 Special access - Register write restrictions are lifted.
4 AUT_RSTA	**Automatic Restart Event after exit from MCU Stop and Wait Mode (SWAI set)** — This bit controls if a Restart Event is automatically generated after exit from MCU Stop Mode or Wait Mode with bit SWAI set. It can be configured for ADC conversion flow control mode “Trigger Mode” and “Restart Mode” (anytime during application runtime). 0 No automatic Restart Event after exit from MCU Stop Mode. 1 Automatic Restart Event occurs after exit from MCU Stop Mode.

10.5.2.6 ADC Conversion Flow Control Register (ADCFLWCTL)

Bit set and bit clear instructions should not be used to access this register.

When the ADC is enabled the bits of ADCFLWCTL register can be modified after a latency time of three Bus Clock cycles.
All bits are cleared if bit ADC_EN is clear or via ADC soft-reset.

Module Base + 0x0005

	7	6	5	4	3	2	1	0
R	SEQA	TRIG	RSTA	LDOK	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 10-9. ADC Conversion Flow Control Register (ADCFLWCTL)

Read: Anytime

Write:

- Bits SEQA, TRIG, RSTA, LDOK can only be set if bit ADC_EN is set.
- Writing 1’b0 to any of these bits does not have an effect

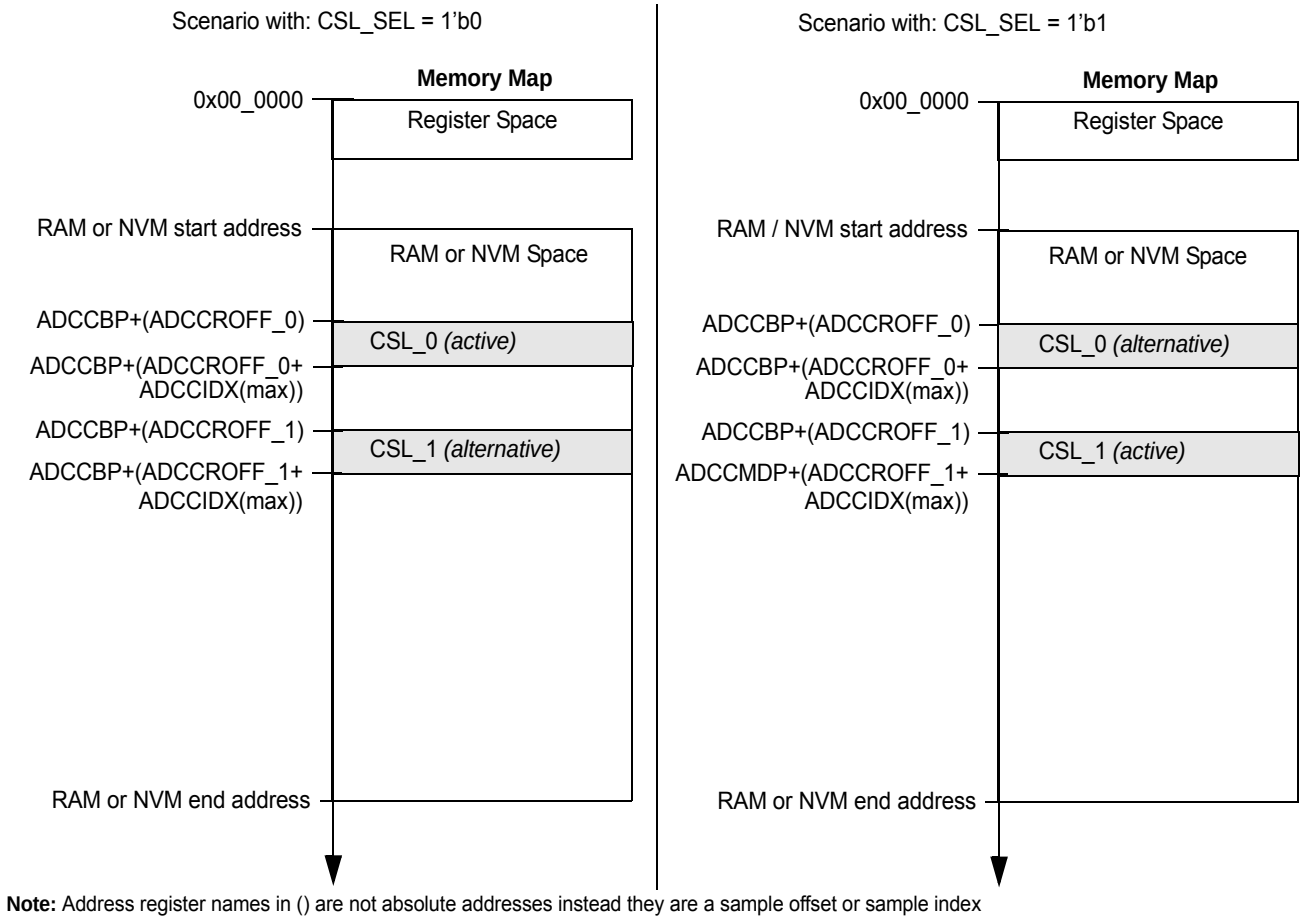
Timing considerations (Trigger Event - channel sample start) depending on ADC mode configuration:

- Restart Mode
  When the Restart Event has been processed (initial command of current CSL is loaded) it takes two Bus Clock cycles plus two ADC conversion clock cycles (pump phase) from the Trigger Event (bit TRIG set) until the select channel starts to sample.
  During a conversion sequence (back to back conversions) it takes five Bus Clock cycles plus two ADC conversion clock cycles (pump phase) from current conversion period end until the newly selected channel is sampled in the following conversion period.
- Trigger Mode
  When a Restart Event occurs a Trigger Event is issued simultaneously. The time required to process the Restart Event is mainly defined by the internal read data bus availability and therefore can vary. In this mode the Trigger Event is processed immediately after the Restart Event is finished and both conversion flow control bits are cleared simultaneously. From de-assert of bit TRIG until sampling begins five Bus Clock cycles are required. Hence from occurrence of a Restart Event until channel sampling it takes five Bus Clock cycles plus an uncertainty of a few Bus Clock cycles.

For more details regarding the sample phase please refer to Section 10.6.2.2, “Sample and Hold Machine with Sample Buffer Amplifier.

10.6.3.2.2 Introduction of the two Command Sequence Lists (CSLs)

The two Command Sequence Lists (CSLs) can be referred to via the Command Base Pointer Register plus the Command and Result Offset Registers plus the Command Index Register (ADCCBP, ADCCROFF_0/1, ADCCIDX).
The final address for conversion command loading is calculated by the sum of these registers (e.g.: ADCCBP+ADCCROFF_0+ADCCIDX or ADCCBP+ADCCROFF_1+ADCCIDX).
Bit CSL_BMOD selects if the CSL is used in double buffer or single buffer mode. In double buffer mode, the CSL can be swapped by flow control bits LDOK and RSTA. For detailed information about when and how the CSL is swapped, please refer to Section 10.6.3.2.5, “The four ADC conversion flow control bits - description of Restart Event + CSL Swap, Section 10.9.7.1, “Initial Start of a Command Sequence List and Section 10.9.7.3, “Restart CSL execution with new/other CSL (alternative CSL becomes active CSL) — CSL swapping
Which list is actively used for ADC command loading is indicated by bit CSL_SEL. The register to define the CSL start addresses (ADCCBP) can be set to any even location of the system RAM or NVM area. It is the user’s responsibility to make sure that the different ADC lists do not overlap or exceed the system RAM or the NVM area, respectively. The error flag IA_EIF will be set for accesses to ranges outside system RAM area and cause an error interrupt if enabled.



Note: Address register names in () are not absolute addresses instead they are a sample offset or sample index

Figure 10-31. Command Sequence List Schema in Double Buffer Mode

13.3.2.15 MSCAN Transmit Error Counter (CANTXERR)

This register reflects the status of the MSCAN transmit error counter.

Module Base + 0x000F — Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 13-18. MSCAN Transmit Error Counter (CANTXERR)

1 Read: Only when in sleep mode (SLPRQ = 1 and SLPAK = 1) or initialization mode (INITRQ = 1 and INITAK = 1)
Write: Unimplemented

NOTE

Reading this register when in any other mode other than sleep or initialization mode, may return an incorrect value. For MCUs with dual CPUs, this may result in a CPU fault condition.

13.3.2.16 MSCAN Identifier Acceptance Registers (CANIDAR0-7)

On reception, each message is written into the background receive buffer. The CPU is only signalled to read the message if it passes the criteria in the identifier acceptance and identifier mask registers (accepted); otherwise, the message is overwritten by the next message (dropped).

The acceptance registers of the MSCAN are applied on the IDR0–IDR3 registers (see Section 13.3.3.1, “Identifier Registers (IDR0–IDR3)”) of incoming messages in a bit by bit manner (see Section 13.4.3, “Identifier Acceptance Filter”).

For extended identifiers, all four acceptance and mask registers are applied. For standard identifiers, only the first two (CANIDAR0/1, CANIDMR0/1) are applied.

Module Base + 0x0010 to Module Base + 0x0013 — Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
Reset	0	0	0	0	0	0	0	0

Figure 13-19. MSCAN Identifier Acceptance Registers (First Bank) — CANIDAR0–CANIDAR3

1 Read: Anytime
Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

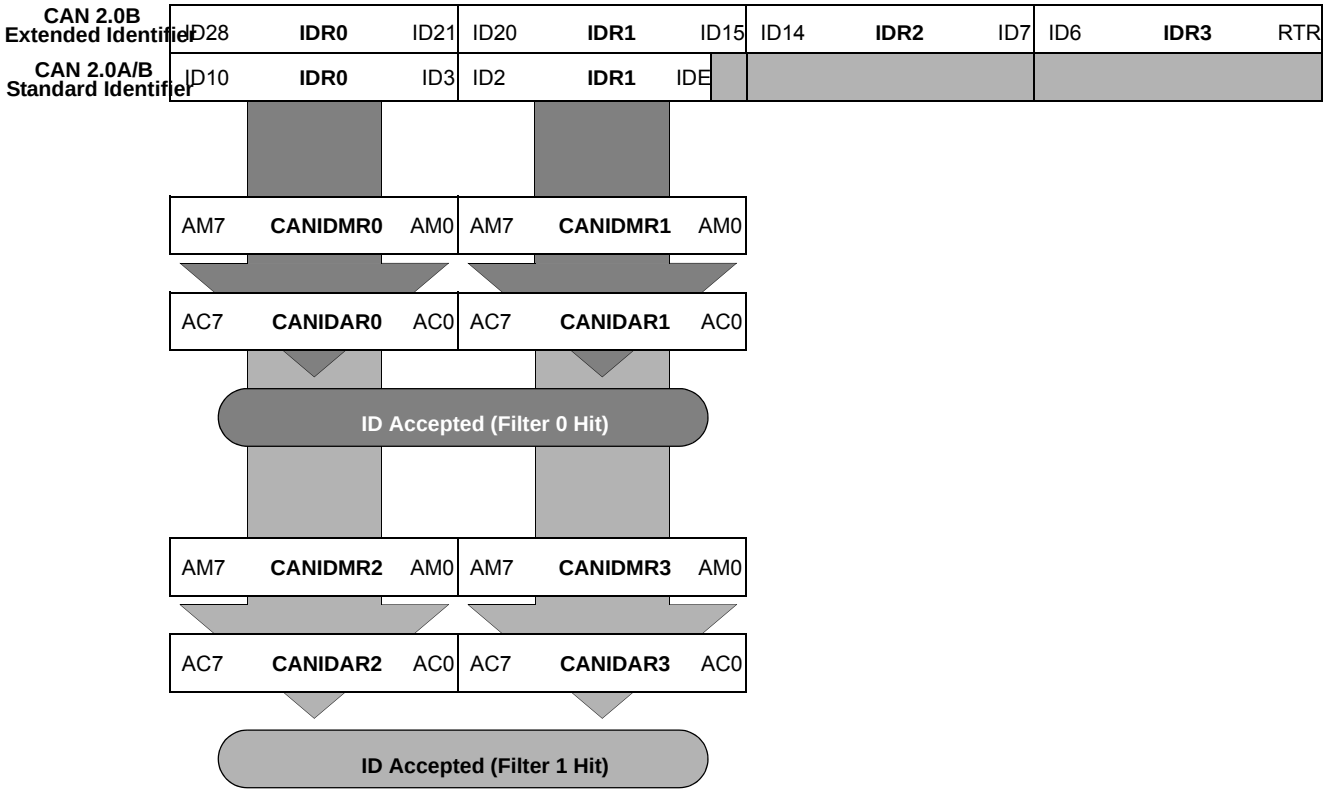


Figure 13-40. 16-bit Maskable Identifier Acceptance Filters

The comparator outputs BVLC and BVHC are forced to zero if the comparator is disabled (configuration bit BSUSE is cleared). If the software disables the comparator during a high or low Voltage condition (BVHC or BVLC active), then an additional interrupt is generated. To avoid this behavior the software must disable the interrupt generation before disabling the comparator.

The BATS interrupt vector is named in Table 14-6. Vector addresses and interrupt priorities are defined at MCU level.

The module internal interrupt sources are combined into one module interrupt signal.

Table 14-6. BATSV3 Interrupt Sources

Module Interrupt Source	Module Internal Interrupt Source	Local Enable
BATSV3 Interrupt (BATI)	BATS Voltage Low Condition Interrupt (BVLI)	BVLIE = 1
	BATS Voltage High Condition Interrupt (BVHI)	BVHIE = 1

14.4.2.1 BATS Voltage Low Condition Interrupt (BVLI)

To use the Voltage Low Interrupt the Level Sensing must be enabled (BSUSE =1).

If measured when

a) V_{LBI1} selected with BVLS[1:0] = 0x0
$V_{measure} < V_{LBI1\_A}$ (falling edge) or $V_{measure} < V_{LBI1\_D}$ (rising edge)

or when

b) V_{LBI2} selected with BVLS[1:0] = 0x1 at pin VSUP
$V_{measure} < V_{LBI2\_A}$ (falling edge) or $V_{measure} < V_{LBI2\_D}$ (rising edge)

or when

c) V_{LBI3} selected with BVLS[1:0] = 0x2
$V_{measure} < V_{LBI3\_A}$ (falling edge) or $V_{measure} < V_{LBI3\_D}$ (rising edge)

or when

d) V_{LBI4} selected with BVLS[1:0] = 0x3
$V_{measure} < V_{LBI4\_A}$ (falling edge) or $V_{measure} < V_{LBI4\_D}$ (rising edge)

then BVLC is set. BVLC status bit indicates that a low voltage at pin VSUP is present. The Low Voltage Interrupt flag (BVLIF) is set to 1 when the Voltage Low Condition (BVLC) changes state . The Interrupt flag BVLIF can only be cleared by writing a 1. If the interrupt is enabled by bit BVLIE the module requests an interrupt to MCU (BATI).

14.4.2.2 BATS Voltage High Condition Interrupt (BVHI)

To use the Voltage High Interrupt the Level Sensing must be enabled (BSUSE=1).

Clock A and B can be software selected to be 1, 1/2, 1/4, 1/8,..., 1/64, 1/128 times the bus clock. Clock SA uses clock A as an input and divides it further with a reloadable counter. Similarly, clock SB uses clock B as an input and divides it further with a reloadable counter. The rates available for clock SA are software selectable to be clock A divided by 2, 4, 6, 8,..., or 512 in increments of divide by 2. Similar rates are available for clock SB. Each PWM channel has the capability of selecting one of four clocks, clock A, Clock B, clock SA or clock SB.

The block diagram in Figure 17-15 shows the four different clocks and how the scaled clocks are created.

17.4.1.1 Prescale

The input clock to the PWM prescaler is the bus clock. It can be disabled whenever the part is in freeze mode by setting the PFRZ bit in the PWMCTL register. If this bit is set, whenever the MCU is in freeze mode (freeze mode signal active) the input clock to the prescaler is disabled. This is useful for emulation in order to freeze the PWM. The input clock can also be disabled when all available PWM channels are disabled (PWMEx-0 = 0). This is useful for reducing power by disabling the prescale counter.

Clock A and clock B are scaled values of the input clock. The value is software selectable for both clock A and clock B and has options of 1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, or 1/128 times the bus clock. The value selected for clock A is determined by the PCKA2, PCKA1, PCKA0 bits in the PWMPRCLK register. The value selected for clock B is determined by the PCKB2, PCKB1, PCKB0 bits also in the PWMPRCLK register.

17.4.1.2 Clock Scale

The scaled A clock uses clock A as an input and divides it further with a user programmable value and then divides this by 2. The scaled B clock uses clock B as an input and divides it further with a user programmable value and then divides this by 2. The rates available for clock SA are software selectable to be clock A divided by 2, 4, 6, 8,..., or 512 in increments of divide by 2. Similar rates are available for clock SB.

Table 18-8. IRSCI Transmit Pulse Width

TNP[1:0]	Narrow Pulse Width
00	3/16

Table 18-9. Bit Error Mode Coding

BERRM1	BERRM0	Function
0	0	Bit error detect circuit is disabled
0	1	Receive input sampling occurs during the 9th time tick of a transmitted bit (refer to Figure 18-19)
1	0	Receive input sampling occurs during the 13th time tick of a transmitted bit (refer to Figure 18-19)
1	1	Reserved

18.3.2.6 SCI Control Register 2 (SCICR2)

Module Base + 0x0003

	7	6	5	4	3	2	1	0
R W	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
Reset	0	0	0	0	0	0	0	0

Figure 18-9. SCI Control Register 2 (SCICR2)

Read: Anytime

Write: Anytime

Table 18-10. SCICR2 Field Descriptions

Field	Description
7 TIE	**Transmitter Interrupt Enable Bit** — TIE enables the transmit data register empty flag, TDRE, to generate interrupt requests. 0 TDRE interrupt requests disabled 1 TDRE interrupt requests enabled
6 TCIE	**Transmission Complete Interrupt Enable Bit** — TCIE enables the transmission complete flag, TC, to generate interrupt requests. 0 TC interrupt requests disabled 1 TC interrupt requests enabled
5 RIE	**Receiver Full Interrupt Enable Bit** — RIE enables the receive data register full flag, RDRF, or the overrun flag, OR, to generate interrupt requests. 0 RDRF and OR interrupt requests disabled 1 RDRF and OR interrupt requests enabled
4 ILIE	**Idle Line Interrupt Enable Bit** — ILIE enables the idle line flag, IDLE, to generate interrupt requests. 0 IDLE interrupt requests disabled 1 IDLE interrupt requests enabled

Appendix F
BATS Electrical Specifications

This section describe the electrical characteristics of the Supply Voltage Sense module.Static Electrical Characteristics.

Table F-1. Static Electrical Characteristics - Supply Voltage Sense - (BATS)

Characteristics noted under conditions 5.5V ≤ V_{SUP} ≤ 18V, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C[1] under nominal conditions unless otherwise noted.						
Num	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	Low Voltage Warning (LBI 1)					
	Ratio = 9					
	Assert (Measured on selected pin, falling edge)	$V_{LBI1\_A\_9}$	4.75	5.5	6	V
	Deassert (Measured on selected pin, rising edge)	$V_{LBI1\_D\_9}$	–	–	6.5	V
	Hysteresis (measured on selected pin)	$V_{LBI1\_H\_9}$	–	0.4	–	V
	Ratio = 17[2]					
	Assert (Measured on selected pin, falling edge)	$V_{LBI1\_A\_17}$	5.0	5.5	6.5	V
	Deassert (Measured on selected pin, rising edge)	$V_{LBI1\_D\_17}$	–	–	7.5	V
	Hysteresis (measured on selected pin)	$V_{LBI1\_H\_17}$	–	1.0	–	V
2	Low Voltage Warning (LBI 2)					
	Ratio = 9					
	Assert (Measured on selected pin, falling edge) on S12ZVL(S)32/16/8	$V_{LBI2\_A\_9}$	5.75	6.75	7.25	V
	Assert (Measured on selected pin, falling edge) on S12ZVL(A)128/96/64	$V_{LBI2\_A\_9}$	5.5	6.75	7.25	V
	Deassert (Measured on selected pin, rising edge)	$V_{LBI2\_D\_9}$	–	–	7.75	
	Hysteresis (measured on selected pin)	$V_{LBI2\_H\_9}$	–	0.4	–	V
	Ratio = 17[2]					V
	Assert (Measured on selected pin, falling edge)	$V_{LBI2\_A\_17}$	6.5	7.5	9.0	
	Deassert (Measured on selected pin, rising edge)	$V_{LBI2\_D\_17}$	–	–	10.0	
	Hysteresis (measured on selected pin)	$V_{LBI2\_H\_17}$	–	1.0	–	
3	Low Voltage Warning (LBI 3)					
	Ratio = 9					
	Assert (Measured on selected pin, falling edge)	$V_{LBI3\_A\_9}$	7	7.75	8.5	V
	Deassert (Measured on selected pin, rising edge)	$V_{LBI3\_D\_9}$	–	–	9	V
	Hysteresis (measured on selected pin)	$V_{LBI3\_H\_9}$	–	0.4	–	V
	Ratio = 17[2]					
	Assert (Measured on selected pin, falling edge)	$V_{LBI3\_A\_17}$	6.5	7.5	8.5	V
	Deassert (Measured on selected pin, rising edge)	$V_{LBI3\_D\_17}$	–	–	9.5	V
	Hysteresis (measured on selected pin)	$V_{LBI3\_H\_17}$	–	1.0	–	V

O.8 0x0400-0x042F TIM1

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0400	TIM1TIOS	R W	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	IOS1	IOS0
0x0401	TIM1CFORC	R W	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	FOC1	FOC0
0x0402- 0x0403	Reserved	R W								
0x0404	TIM1TCNTH	R W	TCNT15	TCNT14	TCNT13	TCNT12	TCNT11	TCNT10	TCNT9	TCNT8
0x0405	TIM1TCNTL	R W	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0
0x0406	TIM1TSCR1	R W	TEN	TSWAI	TSFRZ	TFFCA	PRNT	0	0	0
0x0047	TIM1TTOV	R W	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	TOV1	TOV0
0x0408	TIM1TCTL1	R W	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
0x0409	TIM1TCTL2	R W	RESERVED	RESERVED	OM2	OL2	OM1	OL1	OM0	OL0
0x040A	TIM1TCTL3	R W	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
0x040B	TIM1TCTL4	R W	RESERVED	RESERVED	RESERVED	RESERVED	EDG1B	EDG1A	EDG0B	EDG0A
0x040C	TIM1TIE	R W	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	C1I	C0I
0x040D	TIM1TSCR2	R W	TOI	0	0	0	RESERVED	PR2	PR1	PR0
0x040E	TIM1TFLG1	R W	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	C1F	C0F
0x040F	TIM1TFLG2	R W	TOF	0	0	0	0	0	0	0
0x0400	TIM1TC0H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x0411	TIM1TC0L	R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0412	TIM1TC1H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

O.9 0x0480-x04AF PWM0 (continued)

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x048A - 0x048B	RESERVED	R	0	0	0	0	0	0	0	0
		W								
0x048C	PWMCNT0	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x048D	PWMCNT1	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x048E	PWMCNT2	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x048F	PWMCNT3	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x0490	PWMCNT4	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x0491	PWMCNT5	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x0492	PWMCNT6	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x0493	PWMCNT7	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x0494	PWMPER0	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0495	PWMPER1	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0496	PWMPER2	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0497	PWMPER3	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0498	PWMPER4	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0499	PWMPER5	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x049A	PWMPER6	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x049B	PWMPER7	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								

O.15 0x06C0-0x06DF CPMU (continued)

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x06CC	CPMUCOP	R	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
		W			WRTMASK					
0x06CD	RESERVED CPMUTEST0	R	0	0	0	0	0	0	0	0
		W								
0x06CE	RESERVED CPMUTEST1	R	0	0	0	0	0	0	0	0
		W								
0x06CF	CPMU ARMCOP	R	0	0	0	0	0	0	0	0
		W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x06D0	CPMU HTCTL	R	0	0	VSEL	0	HTE	HTDS	HTIE	HTIF
		W								
0x06D1	CPMU LVCTL	R	0	0	0	0	0	LVDS	LVIE	LVIF
		W								
0x06D2	CPMU APICTL	R	APICLK	0	0	APIES	APIEA	APIFE	APIE	APIF
		W								
0x06D3	CPMUACLKTR	R	ACLKTR5	ACLKTR4	ACLKTR3	ACLKTR2	ACLKTR1	ACLKTR0	0	0
		W								
0x06D4	CPMUAPIRH	R	APIR15	APIR14	APIR13	APIR12	APIR11	APIR10	APIR9	APIR8
		W								
0x06D5	CPMUAPIRL	R	APIR7	APIR6	APIR5	APIR4	APIR3	APIR2	APIR1	APIR0
		W								
0x06D6	RESERVED CPMUTEST3	R	0	0	0	0	0	0	0	0
		W								
0x06D7	CPMUHTTR	R	HTOE	0	0	0	HTTR3	HTTR2	HTTR1	HTTR0
		W								
0x06D8	CPMU IRCTRIMH	R	TCTRIM[4:0]					0	IRCTRIM[9:8]	
		W								
0x06D9	CPMU IRCTRIML	R	IRCTRIM[7:0]							
		W								
0x06DA	CPMUOSC	R	OSCE	Reserved	Reserved	Reserved				
		W								
0x06DB	CPMUPROT	R	0	0	0	0	0	0	0	PROT
		W								
0x06DC	RESERVED CPMUTEST2	R	0	0	0	0	0	0	0	0
		W								

O.17 0x0700-0x0707 SCI0 (continued)

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0706	SCI0DRH	R	R8	T8	0	0	0	0	0	0
		W								
0x0707	SCI0DRL	R	R7	R6	R5	R4	R3	R2	R1	R0
		W	T7	T6	T5	T4	T3	T2	T1	T0

1 These registers are accessible if the AMAP bit in the SCISR2 register is set to zero.

2 These registers are accessible if the AMAP bit in the SCISR2 register is set to one.

O.18 0x0710-0x0717 SCI1

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0710	SCI1BDH[1]	R	SBR15	SBR14	SBR13	SBR12	SBR11	SBR10	SBR9	SBR8
		W								
0x0711	SCI1BDL[1]	R	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
		W								
0x0712	SCI1CR1[1]	R	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
		W								
0x0710	SCI1ASR1[2]	R	RXEDGIF	0	0	0	0	BERRV	BERRIF	BKDIF
		W								
0x0711	SCI1ACR1[2]	R	RXEDGIE	0	0	0	0	0	BERRIE	BKDIE
		W								
0x0712	SCI1ACR2[2]	R	IREN	TNP1	TNP0	0	0	BERRM1	BERRM0	BKDFE
		W								
0x0713	SCI1CR2	R	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		W								
0x0714	SCI1SR1	R	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		W								
0x0715	SCI1SR2	R	AMAP	0	0	TXPOL	RXPOL	BRK13	TXDIR	RAF
		W								
0x0716	SCI1DRH	R	R8	T8	0	0	0	0	0	0
		W								
0x0717	SCI1DRL	R	R7	R6	R5	R4	R3	R2	R1	R0
		W	T7	T6	T5	T4	T3	T2	T1	T0

1 These registers are accessible if the AMAP bit in the SCISR2 register is set to zero.

2 These registers are accessible if the AMAP bit in the SCISR2 register is set to one.