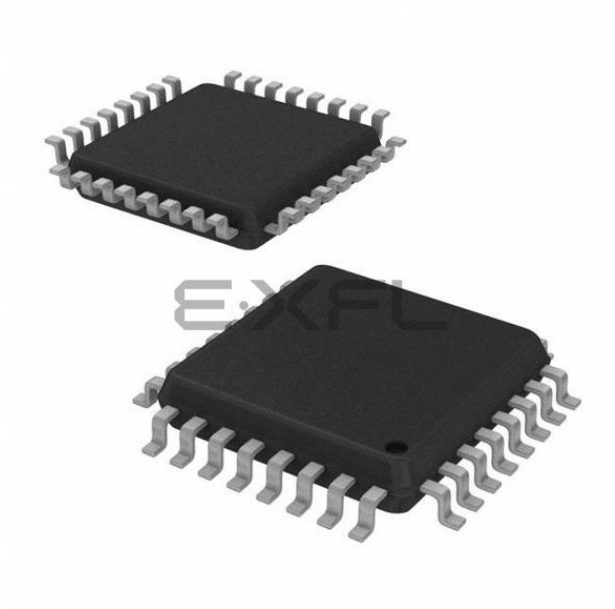


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SCI, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	19
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	5.5V ~ 18V
Data Converters	A/D 6x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s912zvla12f0clcr

1.13 Module device level dependencies

1.13.1 COP Configuration

The COP time-out rate bits CR[2:0] and the WCOP bit in the CPMUCOP register are loaded from the Flash configuration field byte at global address 0xFF_FE0E during the reset sequence. See Table 1-13 and Table 1-14 for coding.

Table 1-13. Initial COP Rate Configuration

NV[2:0] in FOPT Register	CR[2:0] in COPCTL Register
000	111
001	110
010	101
011	100
100	011
101	010
110	001
111	000

Table 1-14. Initial WCOP Configuration

NV[3] in FOPT Register	WCOP in COPCTL Register
1	0
0	1

1.13.2 BDC Command Restriction

The BDC command READ_DBGTB returns 0x00 on this device because the DBG module does not feature a trace buffer.

4.1.4.2 Power modes

The S12ZDBG module is only active in run and wait mode.There is no bus activity in stop mode.

4.1.5 Block Diagram

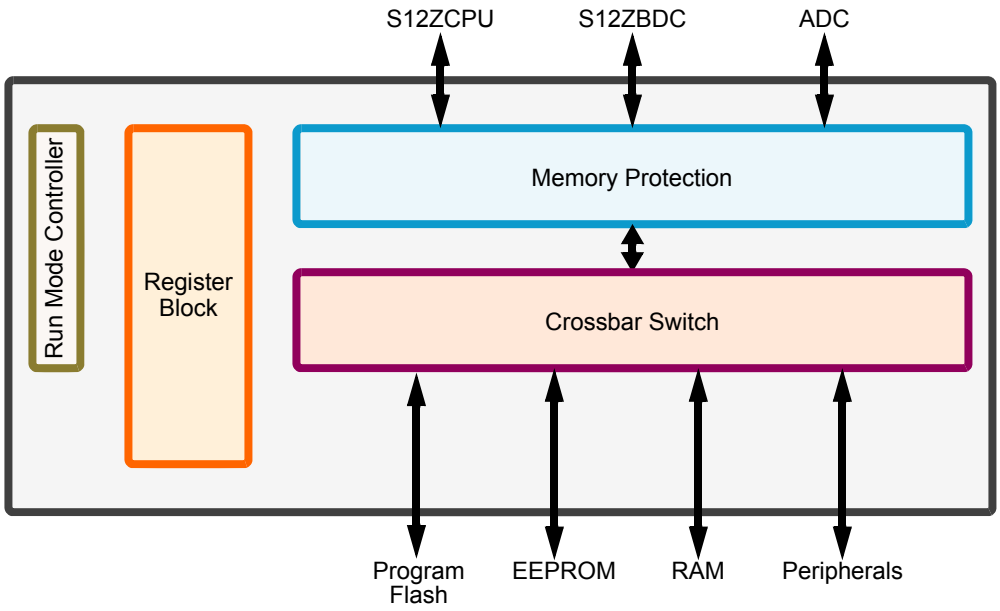


Figure 4-1. S12ZDBG Block Diagram

4.2 External Signal Description

The S12ZDBG uses two external pins to determine the devices operating mode: RESET and MODC (Table 4-3)
See device overview for the mapping of these signals to device pins.

Table 4-3. External System Pins Associated With S12ZDBG

Pin Name	Description
$\overline{\text{RESET}}$	External reset signal. The $\overline{\text{RESET}}$ signal is active low.
MODC	This input is captured in bit MODC of the MODE register when the external $\overline{\text{RESET}}$ pin deasserts.

4.3 Memory Map and Register Definition

4.3.1 Memory Map

A summary of the registers associated with the MMC block is shown in Figure 4-2. Detailed descriptions of the registers and bits are given in the subsections that follow.

Table 4-6. MMCCCRH and MMCCCRL Field Descriptions

Field	Description
7 (MMCCCRH) CPUU	**S12ZCPU User State Flag** — This bit shows the state of the user/supervisor mode bit in the S12ZCPU's CCR at the time the access violation has occurred. The S12ZCPU user state flag is read-only; it will be automatically updated when the next error condition is flagged through the MMCEC register. This bit is undefined if the error code registers (MMCECn) are cleared.
6 (MMCCCRL) CPUX	**S12ZCPU X-Interrupt Mask**— This bit shows the state of the X-interrupt mask in the S12ZCPU's CCR at the time the access violation has occurred. The S12ZCPU X-interrupt mask is read-only; it will be automatically updated when the next error condition is flagged through the MMCEC register. This bit is undefined if the error code registers (MMCECn) are cleared.
4 (MMCCCRL) CPUI	**S12ZCPU I-Interrupt Mask**— This bit shows the state of the I-interrupt mask in the CPU's CCR at the time the access violation has occurred. The S12ZCPU I-interrupt mask is read-only; it will be automatically updated when the next error condition is flagged through the MMCEC register. This bit is undefined if the error code registers (MMCECn) are cleared.

4.3.2.4 Captured S12ZCPU Program Counter (MMCPCH, MMCPCM, MMCPCL)

Address: 0x0085 (MMCPCH)

	7	6	5	4	3	2	1	0
R	CPUPC[23:16]							
W								
Reset	0	0	0	0	0	0	0	0

Address: 0x0086 (MMCPCM)

	7	6	5	4	3	2	1	0
R	CPUPC[15:8]							
W								
Reset	0	0	0	0	0	0	0	0

Address: 0x0087 (MMCPCL)

	7	6	5	4	3	2	1	0
R	CPUPC[7:0]							
W								
Reset	0	0	0	0	0	0	0	0

Figure 4-7. Captured S12ZCPU Program Counter (MMCPCH, MMCPCM, MMCPCL)

Read: Anytime

Write: Never

The ACK handshake protocol does not support nested ACK pulses. If a BDC command is not acknowledged by an ACK pulse, the host needs to abort the pending command first in order to be able to issue a new BDC command. The host can decide to abort any possible pending ACK pulse in order to be sure a new command can be issued. Therefore, the protocol provides a mechanism in which a command, and its corresponding ACK, can be aborted.

Commands With-Status do not generate an ACK, thus if ACK is enabled and a With-Status command is issued, the host must use the 512 cycle timeout to calculate when the data is ready for retrieval.

5.4.7.1 Long-ACK Hardware Handshake Protocol

If a command results in an error condition, whereby a BDCCSRL flag is set, then the target generates a “Long-ACK” low pulse of 64 BDCSI clock cycles, followed by a brief speed pulse. This indicates to the host that an error has occurred. The host can subsequently read BDCCSR to determine the type of error. Whether normal ACK or Long-ACK, the ACK pulse is not issued earlier than 32 BDCSI clock cycles after the BDC command was issued. The end of the BDC command is assumed to be the 16th BDCSI clock cycle of the last bit. The 32 cycle minimum delay differs from the 16 cycle delay time with ACK disabled.

If a BDC access request does not gain access within 512 core clock cycles, the request is aborted, the NORESP flag is set and a Long-ACK pulse is transmitted to indicate an error case.

Following a STOP or WAI instruction, if the BDC is enabled, the first ACK, following stop or wait mode entry is a long ACK to indicate an exception.

5.4.8 Hardware Handshake Abort Procedure

The abort procedure is based on the SYNC command. To abort a command that has not responded with an ACK pulse, the host controller generates a sync request (by driving BKGD low for at least 128 BDCSI clock cycles and then driving it high for one BDCSI clock cycle as a speedup pulse). By detecting this long low pulse in the BKGD pin, the target executes the SYNC protocol, see Section 5.4.4.1, “SYNC”, and assumes that the pending command and therefore the related ACK pulse are being aborted. After the SYNC protocol has been completed the host is free to issue new BDC commands.

The host can issue a SYNC close to the 128 clock cycles length, providing a small overhead on the pulse length to assure the sync pulse is not misinterpreted by the target. See Section 5.4.4.1, “SYNC”.

Figure 5-11 shows a SYNC command being issued after a READ_MEM, which aborts the READ_MEM command. Note that, after the command is aborted a new command is issued by the host.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0140	DBGDCTL	R	0	0	INST	0	RW	RWE	reserved	COMPE
		W								
0x0141-0x0144	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0145	DBGDAH	R	DBGDA[23:16]							
		W								
0x0146	DBGDAM	R	DBGDA[15:8]							
		W								
0x0147	DBGDAL	R	DBGDA[7:0]							
		W								
0x0148-0x017F	Reserved	R	0	0	0	0	0	0	0	0
		W								

Figure 7-2. Quick Reference to DBG Registers

7.3.2 Register Descriptions

This section consists of the DBG register descriptions in address order. When ARM is set in DBGC1, the only bits in the DBG module registers that can be written are ARM, and TRIG

7.3.2.1 Debug Control Register 1 (DBGC1)

Address: 0x0100

	7	6	5	4	3	2	1	0
0x0100	ARM	0 TRIG	reserved	BDMBP	BRKCPU	reserved	EEVE1	0
Reset	0	0	0	0	0	0	0	0

Figure 7-3. Debug Control Register (DBGC1)

Read: Anytime

Write: Bit 7 Anytime . An ongoing profiling session must be finished before DBG can be armed again. Bit 6 can be written anytime but always reads back as 0.
Bits 5:0 anytime DBG is not armed.

NOTE

On a write access to DBGC1 and simultaneous hardware disarm from an internal event, the hardware disarm has highest priority, clearing the ARM bit and generating a breakpoint, if enabled.

Address column refers to the address bits[1:0] of the lowest accessed address (most significant data byte).

Table 7-29. Data Register Use Dependency On CPU Access Type

			Memory Address[2:0]						
Case	Access Address	Access Size	000	001	010	011	100	101	110
1	00	32-bit	DBGxD0	DBGxD1	DBGxD2	DBGxD3			
2	01	32-bit		DBGxD1	DBGxD2	DBGxD3	DBGxD0		
3	10	32-bit			DBGxD2	DBGxD3	DBGxD0	DBGxD1	
4	11	32-bit				DBGxD3	DBGxD0	DBGxD1	DBGxD2
5	00	16-bit	DBGxD0	DBGxD1					
6	01	16-bit		DBGxD1	DBGxD2				
7	10	16-bit			DBGxD2	DBGxD3			
8	11	16-bit				DBGxD3	DBGxD0		
9	00	8-bit	DBGxD0						
10	01	8-bit		DBGxD1					
11	10	8-bit			DBGxD2				
12	11	8-bit				DBGxD3			
13	00	8-bit					DBGxD0		
				Denotes byte that is not accessed.					

For a match of a 32-bit access with data compare, the address comparator must be loaded with the address of the lowest accessed byte. For Case1 Table 7-29 this corresponds to 000, for Case2 it corresponds to 001. To compare all 32-bits, it is required that no bits are masked.

7.4.2.3 Data Bus Comparison NDB Dependency

The NDB control bit allows data bus comparators to be configured to either match on equivalence or on difference. This allows monitoring of a difference in the contents of an address location from an expected value.

When matching on an equivalence (NDB=0), each individual data bus bit position can be masked out by clearing the corresponding mask bit, so that it is ignored in the comparison. A match occurs when all data bus bits with corresponding mask bits set are equivalent. If all mask register bits are clear, then a match is based on the address bus only, the data bus is ignored.

When matching on a difference, mask bits can be cleared to ignore bit positions. A match occurs when any data bus bit with corresponding mask bit set is different. Clearing all mask bits, causes all bits to be ignored and prevents a match because no difference can be detected. In this case address bus equivalence does not cause a match. Bytes that are not accessed are ignored. Thus when monitoring a multi byte field for a difference, partial accesses of the field only return a match if a difference is detected in the accessed bytes.

9.3.2.10 S12CPMU_UHV PLL Control Register (CPMUPLL)

This register controls the PLL functionality.

Module Base + 0x000A

	7	6	5	4	3	2	1	0
R	0	0	FM1	FM0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 9-13. S12CPMU_UHV PLL Control Register (CPMUPLL)

Read: Anytime

Write: Anytime if PROT=0 (CPMUPROT register) and PLLSEL=1 (CPMUCLKS register). Else write has no effect.

NOTE

Write to this register clears the LOCK and UPOSC status bits.

NOTE

Care should be taken to ensure that the bus frequency does not exceed the specified maximum when frequency modulation is enabled.

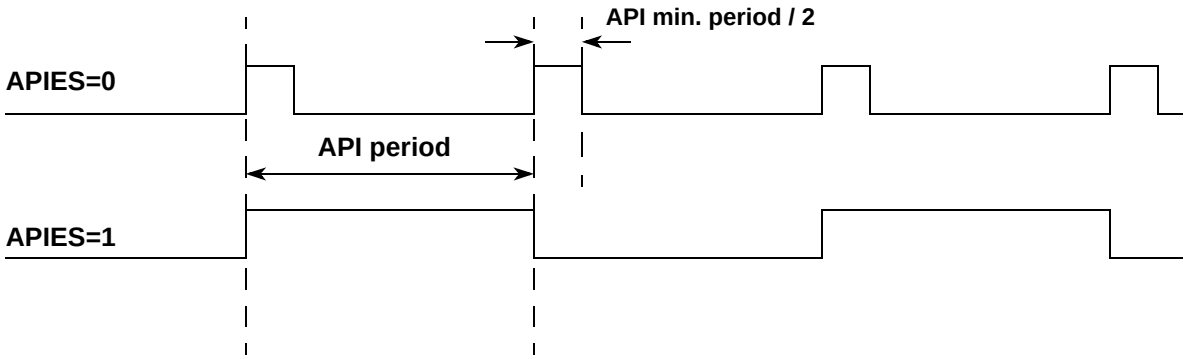
Table 9-9. CPMUPLL Field Descriptions

Field	Description
5, 4 FM1, FM0	PLL **Frequency Modulation Enable Bits** — FM1 and FM0 enable frequency modulation on the VCOCLK. This is to reduce noise emission. The modulation frequency is f_{ref} divided by 16. See Table 9-10 for coding.

Table 9-10. FM Amplitude selection

FM1	FM0	FM Amplitude / f_{VCO} Variation
0	0	FM off
0	1	±1%
1	0	±2%
1	1	±4%

Figure 9-23. Waveform selected on API_EXTCLK pin (APIEA=1, APIFE=1)

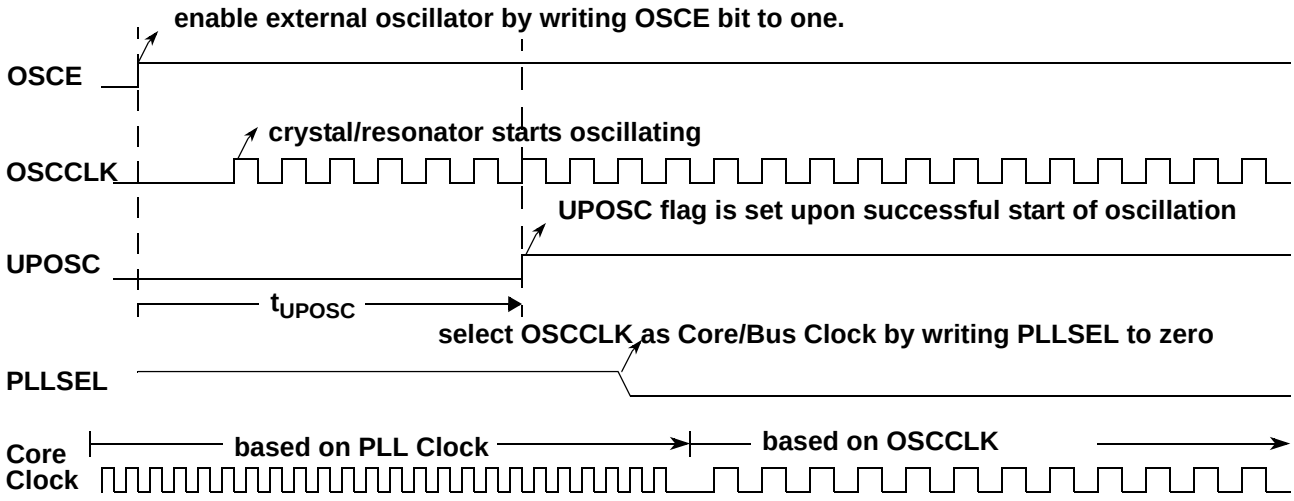


9.4.5 External Oscillator

9.4.5.1 Enabling the External Oscillator

An example of how to use the oscillator as source of the Bus Clock is shown in Figure 9-41.

Figure 9-41. Enabling the external oscillator



Chapter 11
Digital Analog Converter (DAC_8B5V_V2)

11.1 Revision History

Table 11-1. Revision History Table

1.4	17-Nov.-10	11.2.2	Update the behavior of the DACU pin during stop mode
1.5	29-Aug.-13	11.2.2, 11.3	added note about settling time added link to DACM register inside section 11.3
2.0	30-Jan.-14	11.2.3, 11.4.2.1, 11.5.4	added mode “Internal DAC only“
2.1	13-May.-15	Figure 11-5	correct read value of reserved register, Figure 11-5

Glossary

Table 11-2. Terminology

Term	Meaning
DAC	Digital to Analog Converter
VRL	Low Reference Voltage
VRH	High Reference Voltage
FVR	Full Voltage Range
SSC	Special Single Chip

11.2 Introduction

The DAC_8B5V module is a digital to analog converter. The converter works with a resolution of 8 bit and generates an output voltage between VRL and VRH.

The module consists of configuration registers and two analog functional units, a DAC resistor network and an operational amplifier.

The configuration registers provide all required control bits for the DAC resistor network and for the operational amplifier.

The DAC resistor network generates the desired analog output voltage. The unbuffered voltage from the DAC resistor network output can be routed to the external DACU pin. When enabled, the buffered voltage from the operational amplifier output is available on the external AMP pin.

The operational amplifier is also stand alone usable.

Figure 11-1 shows the block diagram of the DAC_8B5V module.

12.3.2.2 PGA Control Register (PGACNTL)

Module Base + 0x0001 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	PGAREFSEL[1:0]		0	0	PGAINSEL[1:0]	
W								
Reset	0	0	0	0	0	0	0	0

Figure 12-4. PGA Control Register (PGACNTL)

1 Read: Anytime
Write: Anytime

Table 12-4. PGACNTL Field Description

Field	Description
5:4 PGAREFSEL[1:0]	**PGA reference voltage selection** — If PGAEN=1 these register bits select the source for the reference voltage (PGAREF, minus input of both amplifier stages). 00 Internally generated V_{DDA} / 2 is selected as reference voltage (PGAREF) 01 Reserved 10 External PGA_REF0 input is selected as reference voltage (PGAREF). 11 External PGA_REF1 input is selected as reference voltage (PGAREF).
1:0 PGAINSEL[1:0]	**PGA input voltages selection** — This register bit defines the source for the plus input voltage of the amplifier. 00 no input voltage selected (PGAIN). 01 input voltage selection controlled by external modules, please see SoC level connection for more details. If the external control signals enables both inputs, then PGA_IN0 is selected. 10 PGA_IN0 is selected as input voltage (PGAIN). 11 PGA_IN1 is selected as input voltage (PGAIN).

12.3.2.3 PGA Gain Register (PGAGAIN)

Module Base + 0x0002 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0				PGAGAIN[3:0]			
W								
Reset	0	0	0	0	0	0	0	0

Figure 12-5. PGA Gain Register (PGAGAIN)

1 Read: Anytime
Write: Anytime

Table 12-5. PGAGAIN Field Description

Field	Description
3:0 PGAGAIN[3:0]	**PGA1 gain**— These register bits select the gain A_{PGA} (amplification factor) for the PGA stage, see Table 12-6., “Amplifier Gain

Table 13-11. CANRFLG Register Field Descriptions (continued)

Field	Description
1 OVRIF	**Overrun Interrupt Flag** — This flag is set when a data overrun condition occurs. If not masked, an error interrupt is pending while this flag is set. 0 No data overrun condition 1 A data overrun detected
0 RXF[2]	**Receive Buffer Full Flag** — RXF is set by the MSCAN when a new message is shifted in the receiver FIFO. This flag indicates whether the shifted buffer is loaded with a correctly received message (matching identifier, matching cyclic redundancy code (CRC) and no other errors detected). After the CPU has read that message from the RxFG buffer in the receiver FIFO, the RXF flag must be cleared to release the buffer. A set RXF flag prohibits the shifting of the next FIFO entry into the foreground buffer (RxFG). If not masked, a receive interrupt is pending while this flag is set. 0 No new message available within the RxFG 1 The receiver FIFO is not empty. A new message is available in the RxFG

1 Redundant Information for the most critical CAN bus status which is “bus-off”. This only occurs if the Tx error counter exceeds a number of 255 errors. Bus-off affects the receiver state. As soon as the transmitter leaves its bus-off state the receiver state skips to RxOK too. Refer also to TSTAT[1:0] coding in this register.

2 To ensure data integrity, do not read the receive buffer registers while the RXF flag is cleared. For MCUs with dual CPUs, reading the receive buffer registers while the RXF flag is cleared may result in a CPU fault condition.

13.3.2.6 MSCAN Receiver Interrupt Enable Register (CANRIER)

This register contains the interrupt enable bits for the interrupt flags described in the CANRFLG register.

Module Base + 0x0005 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
Reset:	0	0	0	0	0	0	0	0

Figure 13-9. MSCAN Receiver Interrupt Enable Register (CANRIER)

1 Read: Anytime
Write: Anytime when not in initialization mode

NOTE

The CANRIER register is held in the reset state when the initialization mode is active (INITRQ=1 and INITAK=1). This register is writable when not in initialization mode (INITRQ=0 and INITAK=0).

The RSTATE[1:0], TSTATE[1:0] bits are not affected by initialization mode.

15.3.2.8 Timer Interrupt Enable Register (TIE)

Module Base + 0x000C

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	C5I	C4I	C3I	C2I	C1I	C0I
Reset	0	0	0	0	0	0	0	0

Figure 15-14. Timer Interrupt Enable Register (TIE)

Read: Anytime

Write: Anytime.

Table 15-10. TIE Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero

Field	Description
5:0 C5I:C0I	**Input Capture/Output Compare "x" Interrupt Enable —** The bits in TIE correspond bit-for-bit with the bits in the TFLG1 status register. If cleared, the corresponding flag is disabled from causing a hardware interrupt. If set, the corresponding flag is enabled to cause a interrupt.

15.3.2.9 Timer System Control Register 2 (TSCR2)

Module Base + 0x000D

	7	6	5	4	3	2	1	0
R	TOI	0	0	0	RESERVED	PR2	PR1	PR0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 15-15. Timer System Control Register 2 (TSCR2)

Read: Anytime

Write: Anytime.

Table 15-11. TSCR2 Field Descriptions

Field	Description
7 TOI	Timer Overflow Interrupt Enable 0 Interrupt inhibited. 1 Hardware interrupt requested when TOF flag set.
2:0 PR[2:0]	**Timer Prescaler Select** — These three bits select the frequency of the timer prescaler clock derived from the Bus Clock as shown in Table 15-12.

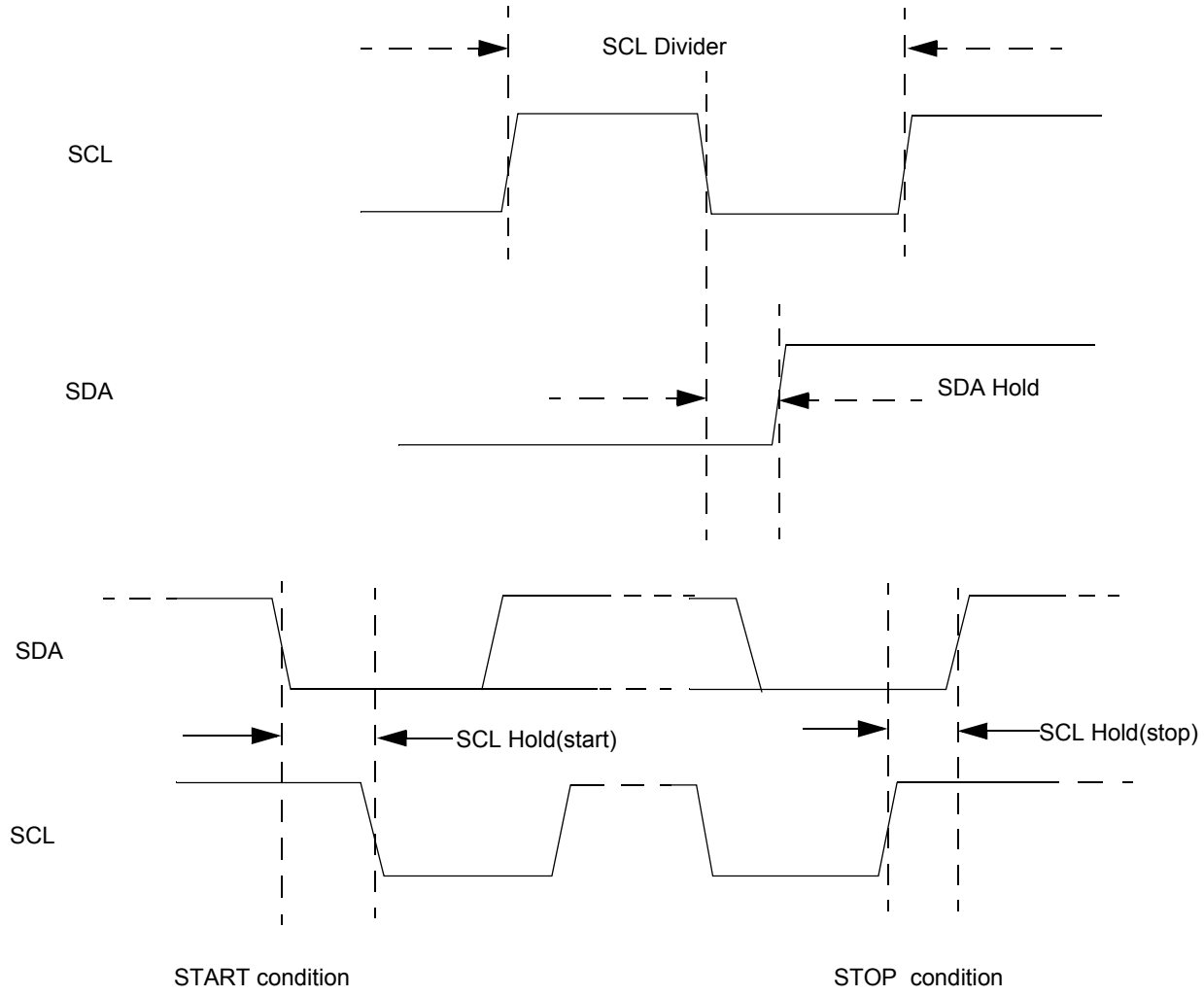


Figure 20-5. SCL Divider and SDA Hold

The equation used to generate the divider values from the IBFD bits is:

SCL Divider = MUL x {2 x (scl2tap + [(SCL_Tap -1) x tap2tap] + 2)}

The SDA hold delay is equal to the CPU clock period multiplied by the SDA Hold value shown in Table 20-7. The equation used to generate the SDA Hold value from the IBFD bits is:

SDA Hold = MUL x {scl2tap + [(SDA_Tap - 1) x tap2tap] + 3}

The equation for SCL Hold values to generate the start and stop conditions from the IBFD bits is:

SCL Hold(start) = MUL x [scl2start + (SCL_Tap - 1) x tap2tap]

SCL Hold(stop) = MUL x [scl2stop + (SCL_Tap - 1) x tap2tap]

Table 20-7. IIC Divider and Hold Values (Sheet 1 of 6)

IBC[7:0] (hex)	SCL Divider (clocks)	SDA Hold (clocks)	SCL Hold (start)	SCL Hold (stop)
MUL=1				

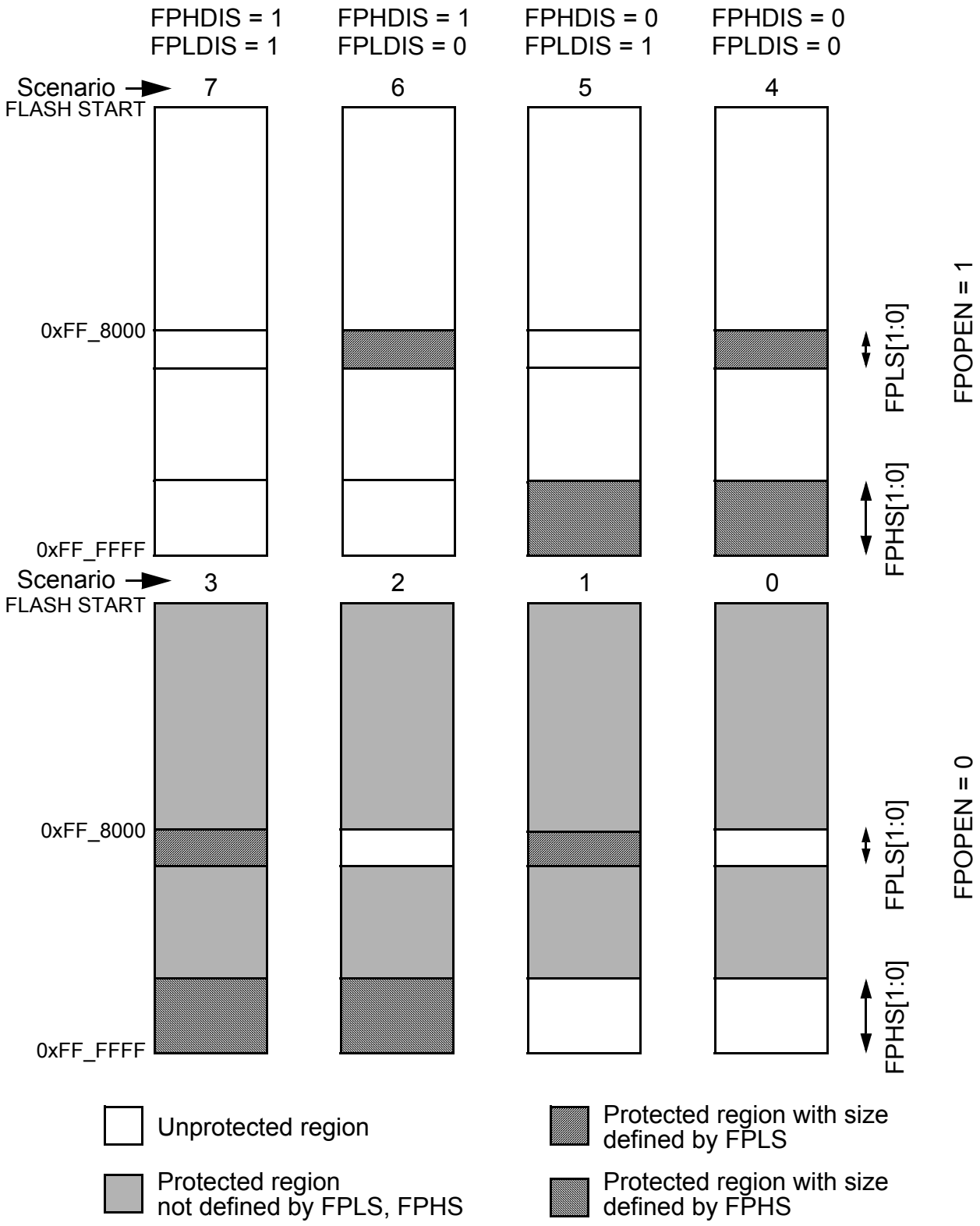


Figure 22-14. P-Flash Protection Scenarios

Table C-3. ADC Conversion Performance 5V range

Supply voltage:
MC9S12ZVL(S)32\16\8: 4.5V ≤ V_{DDX} ≤ 5.5V, 4.5V ≤ V_{REF} ≤ 5.5V,
MC9S12ZVL(A)128\96\64: 4.85V ≤ V_{DDX} ≤ 5.15V, 4.85V ≤ V_{REF} ≤ 5.15V,
-40°C < T_J < 175°C, V_{REF} = V_{RH} - V_{RL}, f_{ADCCLK} = 8.0MHz
The values are tested to be valid with no port AD output drivers switching simultaneous with conversions.

Num	Rating[1]		Symbol	Min	Typ	Max	Unit
1	Resolution	12-Bit	LSB		1.25		mV
2	Differential Nonlinearity	12-Bit	DNL	-4	±2	4	counts
3	Integral Nonlinearity	12-Bit	INL	-5	±2.5	5	counts
4	Absolute Error[2]	12-Bit	AE	-7	±4	7	counts
5	Resolution	10-Bit	LSB		5		mV
6	Differential Nonlinearity	10-Bit	DNL	-1	±0.5	1	counts
7	Integral Nonlinearity	10-Bit	INL	-2	±1	2	counts
8	Absolute Error[2]	10-Bit	AE	-3	±2	3	counts
9	Resolution	8-Bit	LSB		20		mV
10	Differential Nonlinearity	8-Bit	DNL	-0.5	±0.3	0.5	counts
11	Integral Nonlinearity	8-Bit	INL	-1	±0.5	1	counts
12	Absolute Error[2]	8-Bit	AE	-1.5	±1	1.5	counts

1 The 8-bit and 10-bit mode operation is structurally tested in production test. Absolute values are tested in 12-bit mode.

2 These values include the quantization error which is inherently 1/2 count for any A/D converter.

Table C-4. DC Conversion Performance 3.3V range

Supply voltage MC9S12ZVL(A)128\96\64: 3.20V ≤ V_{DDA} ≤ 3.39V, -40°C < T_J < 175°C. 3.20V ≤ V_{REF} ≤ 3.39V = V_{RH} - V_{RL}.
f_{ADCCLK} = 8.0MHz
The values are tested to be valid with no port AD output drivers switching simultaneous with conversions.

Num	Rating[1]		Symbol	Min	Typ	Max	Unit
1	Resolution	12-Bit	LSB		0.80		mV
2	Differential Nonlinearity	12-Bit	DNL	-6	±3	6	counts
3	Integral Nonlinearity	12-Bit	INL	-7	±3	7	counts
4	Absolute Error[2]	12-Bit	AE	-8	±4	8	counts
5	Resolution	10-Bit	LSB		3.22		mV
6	Differential Nonlinearity	10-Bit	DNL	-1.5	±1	1.5	counts
7	Integral Nonlinearity	10-Bit	INL	-2	±1	2	counts
8	Absolute Error[2]	10-Bit	AE	-3	±2	3	counts
9	Resolution	8-Bit	LSB		12.89		mV
10	Differential Nonlinearity	8-Bit	DNL	-0.5	±0.3	0.5	counts
11	Integral Nonlinearity	8-Bit	INL	-1	±0.5	1	counts
12	Absolute Error[2]	8-Bit	AE	-1.5	±1	1.5	counts

Appendix D
LINPHY Electrical Specifications

D.1 Maximum Ratings

Table D-1. Maximum ratings of the LINPHY

Num	Ratings	Symbol	Value	Unit
1	DC voltage on LIN	V_{LIN}	-32 to +42	V
2	Continuous current on LIN	I_{LIN}	± 200 [1]	mA

[1]The current on the LIN pin is internally limited. Therefore, it should not be possible to reach the 200mA anyway.

D.2 Static Electrical Characteristics

Table D-2. Static electrical characteristics of the LINPHY

Characteristics noted under conditions 5.5V ≤ V_{LINSUP} ≤ 18V unless otherwise noted[1 2 3]. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.						
Num	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	V_{LINSUP} operating range	V_{LINSUP_LIN}	5.5[1 2]	12	18	V
2	Current limitation into the LIN pin in dominant state[4] V_{LIN} = $V_{LINSUP\_LIN\_MAX}$	I_{LIN_LIM}	40		200	mA
3	Input leakage current in dominant state, driver off, internal pull-up on V_{LIN} = 0V, V_{LINSUP} = 12V	$I_{LIN\_PAS\_dom}$	-1			mA
4	Input leakage current in recessive state, driver off 5.5V<V_{LINSUP}<18V, 5.5V<V_{LIN}<18V, V_{LIN} > V_{LINSUP}	$I_{LIN\_PAS\_rec}$			20	µA
5	Input leakage current when ground disconnected -40°C < TJ < 175°C GND_{Device} = V_{LINSUP}, 0V<V_{LIN}<18V, V_{LINSUP} = 12V	$I_{LIN\_NO\_GND}$	-1		1	mA
6	Input leakage current when battery disconnected -40°C < TJ < 175°C V_{LINSUP} = GND_{Device}, 0<V_{LIN}<18V	$I_{LIN\_NO\_BAT}$			30	µA
7	Receiver dominant state	V_{LINdom}			0.4	V_{LINSUP}
8	Receiver recessive state	V_{LINrec}	0.6			V_{LINSUP}
9	V_{LIN_CNT} =(V_{th_dom}+ V_{th_rec})/2	V_{LIN_CNT}	0.475	0.5	0.525	V_{LINSUP}
10	V_{HYS} = V_{th_rec} -V_{th_dom}	V_{HYS}			0.175	V_{LINSUP}
11	Maximum capacitance allowed on slave node including external components	C_{slave}		220	250	pF
12a	Capacitance of the LIN pin, Recessive state	C_{LIN}		20		pF

Table E-2. NVM Timing Characteristics ZVL(A)128/96/64

Num	Command	f_{NVMOP} cycle	f_{NVMBUS} cycle	Symbol	Min[1]	Typ[2]	Max[3]	Lfmax[4]	Unit
1	Bus frequency	1	—	f_{NVMBUS}	1	32	32		MHz
2	NVM Operating frequency	—	1	f_{NVMOP}	0.8	1	1.05		MHz
3	Erase Verify All Blocks[5,6]	0	34528	t_{RD1ALL}	1.08	1.08	2.16	69.06	ms
4	Erase Verify Block (Pflash)[5]	0	33323	t_{RD1BLK_P}	1.04	1.04	2.08	66.65	ms
5	Erase Verify Block (EEPROM)[6]	0	1591	t_{RD1BLK_D}	0.05	0.05	0.10	3.18	ms
6	Erase Verify P-Flash Section	0	508	t_{RD1SEC}	0.02	0.02	0.03	1.02	ms
7	Read Once	0	481	t_{RDONCE}	15.03	15.03	15.03	481.00	us
8	Program P-Flash (4 Word)	164	3133	t_{PGM_4}	0.25	0.26	0.56	12.74	ms
9	Program Once	164	3107	$t_{PGMONCE}$	0.25	0.26	0.26	3.31	ms
10	Erase All Blocks[5,6]	100066	34991	t_{ERSALL}	96.39	101.16	102.25	195.06	ms
11	Erase Flash Block (Pflash)[5]	100060	33692	t_{ERSBLK_P}	96.35	101.11	102.17	192.46	ms
12	Erase Flash Block (EEPROM)[6]	100060	1930	t_{ERSBLK_D}	95.36	100.12	100.18	128.94	ms
13	Erase P-Flash Sector	20015	924	t_{ERSPG}	19.09	20.04	20.07	26.87	ms
14	Unsecure Flash	100066	35069	t_{UNSECU}	96.40	101.16	102.26	195.22	ms
15	Verify Backdoor Access Key	0	493	t_{VFYKEY}	15.41	15.41	15.41	493.00	us
16	Set User Margin Level	0	436	t_{MLOADU}	13.63	13.63	13.63	436.00	us
17	Set Factory Margin Level	0	445	t_{MLOADF}	13.91	13.91	13.91	445.00	us
18	Erase Verify EEPROM Section	0	583	$t_{DRD1SEC}$	0.02	0.02	0.04	1.17	ms
19	Program EEPROM (1 Word)	68	1678	t_{DPGM_1}	0.12	0.12	0.28	6.80	ms
20	Program EEPROM (2 Word)	136	2702	t_{DPGM_2}	0.21	0.22	0.47	10.98	ms
21	Program EEPROM (3 Word)	204	3726	t_{DPGM_3}	0.31	0.32	0.67	15.16	ms
22	Program EEPROM (4 Word)	272	4750	t_{DPGM_4}	0.41	0.42	0.87	19.34	ms
23	Erase EEPROM Sector	5015	817	t_{DERSPG}	4.80	5.04	20.49	38.96	ms
24	Protection Override	0	475	$t_{PRTOVRD}$	14.84	14.84	14.84	475.00	us

1 Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}

2 Typical times are based on typical f_{NVMOP} and typical f_{NVMBUS}

3 Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging

4 Lowest-frequency max times are based on minimum f_{NVMOP} and minimum f_{NVMBUS} plus aging

5 Affected by Pflash size

6 Affected by EEPROM size

E.2 NVM Reliability Parameters

The reliability of the NVM blocks is guaranteed by stress test during qualification, constant process monitors and burn-in to screen early life failures.

[4] The structure of the HVI pins does not include diode structures shown in Figure A-1 that inject current when the input voltage goes outside the supply-ground range. Thus the HVI pin current injection is limited to below 200uA within the absolute maximum pin voltage range. However if the HVI impedance converter bypass is enabled, then even currents in this range can corrupt ADC results from simultaneous conversions on other channels. This can be prevented by disabling the bypass, either by clearing the PTAENLx or PTABYPLx bit. Similarly when the ADC is converting a HVI pin voltage then the impedance converter bypass must be disabled to ensure that current injection on PADx pins does not impact the HVI ADC conversion result.

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0830-0x083F	CANTXFG	R W	See Section 13.3.3, “Programmer’s Model of Message Storage”							

O.22 0x0980-0x0987 LINPHY0

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0980	LP0DR	R	0	0	0	0	0	0	LPDR1	LPDR0
		W								
0x0981	LP0CR	R	0	0	0	0	LPE	RXONLY	LPWUE	LPPUE
		W								
0x0982	Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		W								
0x0983	LPSLRM	R	LPDTDIS	0	0	0	0	0	LPSLR1	LPSLR0
		W								
0x0984	Reserved	R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		W								
0x0985	LP0SR	R	LPDT	0	0	0	0	0	0	0
		W								
0x0986	LP0IE	R	LPDTIE	LPOCIE	0	0	0	0	0	0
		W								
0x0987	LP0IF	R	LPDTIF	LPOCIF	0	0	0	0	0	0
		W								

O.23 0x0B40-0x0B47 PGA

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0B40	PGAEN	R	0	0	0	0	0		PGAOFFSCEN	PGAEN
		W								
0x0B41	PGACNTL	R	0	0	PGAREFSEL[1:0]		0	0	PGAINSEL[1:0]	
		W								
0x0B42	PGAGAIN	R	0	0	0	0	PGAGAIN[3:0]			
		W								
0x0B43	PGAOFFSET	R	0		PGAOFFSET[5:0]					
		W								
0x0B44-0xB46	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0B47	Reserved	R	0	0	0	0	0	Reserved	Reserved	Reserved
		W								