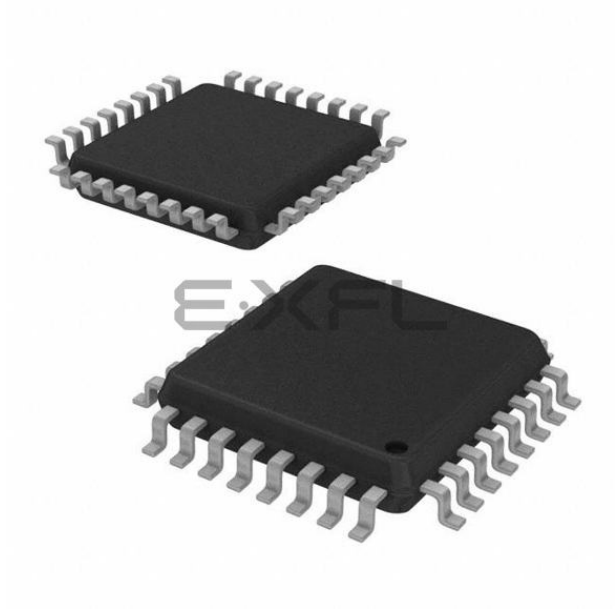

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SCI, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	19
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	5.5V ~ 18V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12zvl16f0mlcr

1.7.2.17.2 TXD[1:0] Signals

These signals are associated with the transmit functionality of the serial communication interfaces (SCI[1:0]).

1.7.2.18 IIC0 Signals

1.7.2.18.1 SCL0

This signal is associated with the SCL functionality of the IIC0 module.

1.7.2.18.2 SDA0

This signal is associated with the SDA functionality of the IIC0 module.

1.7.2.19 Timer0 IOC0[5:0] Signals

The signals IOC0[5:0] are associated with the input capture or output compare functionality of the timer (TIM0) module.

1.7.2.20 Timer1 IOC1[1:0] Signals

The signals IOC1[1:0] are associated with the input capture or output compare functionality of the timer (TIM1) module.

1.7.2.21 PWM[7:0] Signals

The signals PWM[7:0] are associated with the PWM module digital channel outputs.

1.7.2.22 Interrupt Signals — $\overline{\text{IRQ}}$ and $\overline{\text{XIRQ}}$

$\overline{\text{IRQ}}$ is a maskable level or falling edge sensitive input. $\overline{\text{XIRQ}}$ is a non-maskable level-sensitive interrupt.

1.7.2.23 Oscillator and Clock Signals

1.7.2.23.1 Oscillator Signals — EXTAL and XTAL

EXTAL and XTAL are the crystal driver and external clock pins. On reset all the device clocks are derived from the internal PLLCLK, independent of EXTAL and XTAL. XTAL is the oscillator output. The EXTAL and XTAL signals are associated with PE[1:0].

1.7.2.23.2 ECLK

This signal is associated with the output of the bus clock (ECLK).

NOTE

This feature is only intended for debug purposes at room temperature.
It must not be used for clocking external devices in an application.

Chapter 5
Background Debug Controller (S12ZBDCV2)

Table 5-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V2.04	03.Dec.2012	Section 5.1.3.3, “Low-Power Modes	Included BACKGROUND/ Stop mode dependency
V2.05	22.Jan.2013	Section 5.3.2.2, “BDC Control Status Register Low (BDCCSRL)	Improved NORESP description and added STEP1/ Wait mode dependency
V2.06	22.Mar.2013	Section 5.3.2.2, “BDC Control Status Register Low (BDCCSRL)	Improved NORESP description of STEP1/ Wait mode dependency
V2.07	11.Apr.2013	Section 5.1.3.3.1, “Stop Mode	Improved STOP and BACKGROUND interdepency description
V2.08	31.May.2013	Section 5.4.4.4, “BACKGROUND Section 5.4.7.1, “Long-ACK Hardware Handshake Protocol	Removed misleading WAIT and BACKGROUND interdepency description Added subsection dedicated to Long-ACK
V2.09	29.Aug.2013	Section 5.4.4.12, “READ_DBGTB	Noted that READ_DBGTB is only available for devices featuring a trace buffer.
V2.10	21.Oct.2013	Section 5.1.3.3.2, “Wait Mode	Improved description of NORESP dependence on WAIT and BACKROUND
V2.11	02.Feb.2015	Section 5.1.3.3.1, “Stop Mode Section 5.3.2, “Register Descriptions	Corrected name of clock that can stay active in Stop mode

5.1 Introduction

The background debug controller (BDC) is a single-wire, background debug system implemented in on-chip hardware for minimal CPU intervention. The device BKGD pin interfaces directly to the BDC.

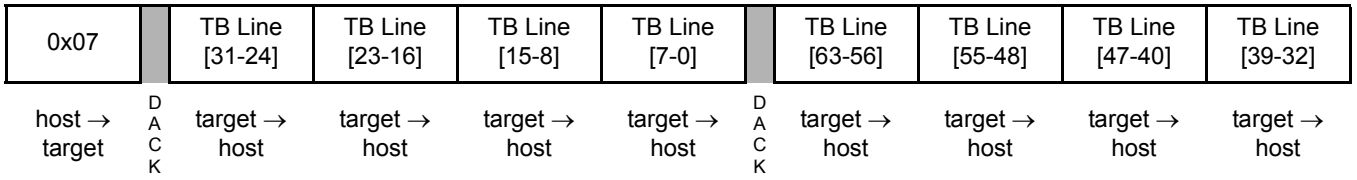
The S12ZBDC maintains the standard S12 serial interface protocol but introduces an enhanced handshake protocol and enhanced BDC command set to support the linear instruction set family of S12Z devices and offer easier, more flexible internal resource access over the BDC serial interface.

returned before the read data. This status byte reflects the state after the memory read was performed. If enabled, an ACK pulse is driven before the data bytes are transmitted.

The examples show the READ_MEM.B{_WS}, READ_MEM.W{_WS} and READ_MEM.L{_WS} commands.

5.4.4.12 READ_DBGTB

Read DBG trace buffer **Non-intrusive**



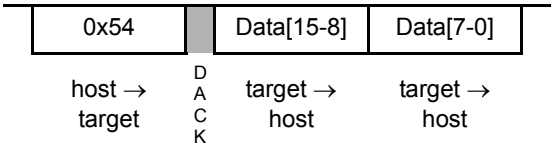
This command is only available on devices, where the DBG module includes a trace buffer. Attempted use of this command on devices without a traace buffer return 0x00.

Read 64 bits from the DBG trace buffer. Refer to the DBG module description for more detailed information. If enabled an ACK pulse is generated before each 32-bit longword is ready to be read by the host. After issuing the first ACK a timeout is still possible whilst accessing the second 32-bit longword, since this requires separate internal accesses. The first 32-bit longword corresponds to trace buffer line bits[31:0]; the second to trace buffer line bits[63:32]. If ACK handshaking is disabled, the host must wait 16 clock cycles (DLY) after completing the first 32-bit read before starting the second 32-bit read.

5.4.4.13 READ_SAME.sz, READ_SAME.sz_WS

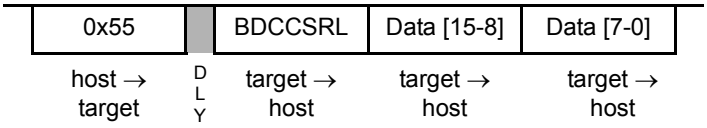
READ_SAME

Read same location specified by previous READ_MEM{_WS} **Non-intrusive**



READ_SAME_WS

Read same location specified by previous READ_MEM{_WS} **Non-intrusive**



9.3.2.22 High Temperature Trimming Register (CPMUHTTR)

The CPMUHTTR register configures the trimming of the S12CPMU_UHV temperature sense.

Module Base + 0x0017

	7	6	5	4	3	2	1	0
R	HTOE	0	0	0	HTTR3	HTTR2	HTTR1	HTTR0
W								
Reset	0	0	0	0	F	F	F	F

After de-assert of System Reset a trim value is automatically loaded from the Flash memory. See Device specification for details.

= Unimplemented or Reserved

Figure 9-28. High Temperature Trimming Register (CPMUHTTR)

Read: Anytime

Write: Anytime

Table 9-25. CPMUHTTR Field Descriptions

Field	Description
7 HTOE	**High Temperature Offset Enable Bit** — If set the temperature sense offset is enabled. 0 The temperature sense offset is disabled. HTTR[3:0] bits don't care. 1 The temperature sense offset is enabled. HTTR[3:0] select the temperature offset.
3–0 HTTR[3:0]	**High Temperature Trimming Bits** — See Table 9-26 for trimming effects.

Table 9-26. Trimming Effect of HTTR

HTTR[3:0]	Temperature sensor voltage V_{HT}	Interrupt threshold temperatures T_{HTIA} and T_{HTID}
0000	lowest	highest
0001	increasing	decreasing
....		
1110		
1111	highest	lowest

Several examples of PLL divider settings are shown in Table 9-33. The following rules help to achieve optimum stability and shortest lock time:

- Use lowest possible f_{VCO} / f_{REF} ratio (SYNDIV value).
- Use highest possible REFCLK frequency f_{REF}.

Table 9-33. Examples of PLL Divider Settings

f_{osc}	REFDIV[3:0]	f_{REF}	REFFRQ[1:0]	SYNDIV[5:0]	f_{VCO}	VCOFRQ[1:0]	POSTDIV[4:0]	f_{PLL}	f_{bus}
off	$00	1MHz	00	$18	50MHz	01	$03	12.5MHz	6.25MHz
off	$00	1MHz	00	$18	50MHz	01	$00	50MHz	25MHz
4MHz	$00	4MHz	01	$05	48MHz	00	$00	48MHz	24MHz

The phase detector inside the PLL compares the feedback clock (FBCLK = VCOCLK/(SYNDIV+1)) with the reference clock (REFCLK = (IRC1M or OSCCLK)/(REFDIV+1)). Correction pulses are generated based on the phase difference between the two signals. The loop filter alters the DC voltage on the internal filter capacitor, based on the width and direction of the correction pulse which leads to a higher or lower VCO frequency.

The user must select the range of the REFCLK frequency (REFFRQ[1:0] bits) and the range of the VCOCLK frequency (VCOFRQ[1:0] bits) to ensure that the correct PLL loop bandwidth is set.

The lock detector compares the frequencies of the FBCLK and the REFCLK. Therefore the speed of the lock detector is directly proportional to the reference clock frequency. The circuit determines the lock condition based on this comparison. So e.g. a failure in the reference clock will cause the PLL not to lock.

If PLL LOCK interrupt requests are enabled, the software can wait for an interrupt request and for instance check the LOCK bit. If interrupt requests are disabled, software can poll the LOCK bit continuously (during PLL start-up) or at periodic intervals. In either case, only when the LOCK bit is set, the VCOCLK will have stabilized to the programmed frequency.

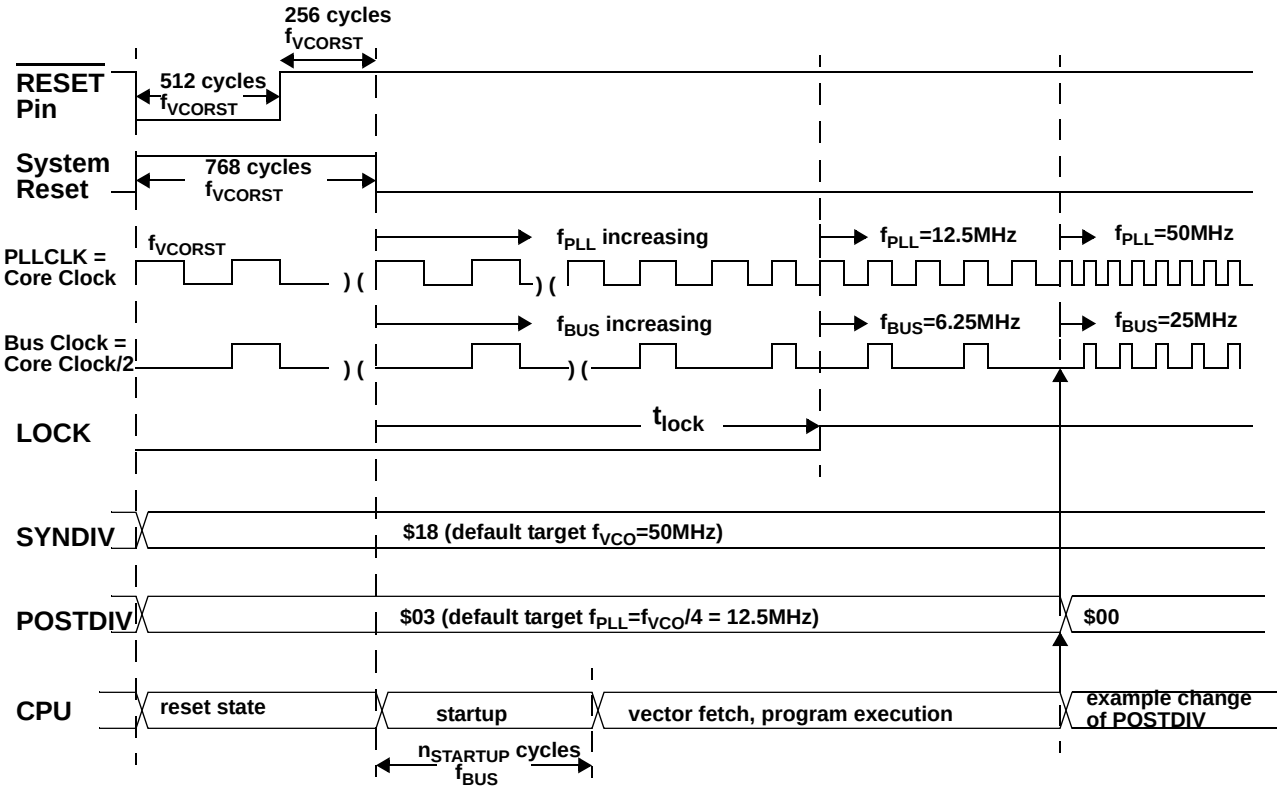
- The LOCK bit is a read-only indicator of the locked state of the PLL.
- The LOCK bit is set when the VCO frequency is within the tolerance, Δ_{Lock}, and is cleared when the VCO frequency is out of the tolerance, Δ_{unl}.
- Interrupt requests can occur if enabled (LOCKIE = 1) when the lock condition changes, toggling the LOCK bit.

In case of loss of reference clock (e.g. IRCCLK) the PLL will not lock or if already locked, then it will unlock. The frequency of the VCOCLK will be very low and will depend on the value of the VCOFRQ[1:0] bits.

9.4.2 Startup from Reset

An example for startup of the clock system from Reset is given in Figure 9-38.

Figure 9-38. Startup of clock system after Reset



10.5.2.15 ADC Command Register 0 (ADCCMD_0)

Module Base + 0x0014

	31	30	29	28	27	26	25	24
R	CMD_SEL		0	0	INTFLG_SEL[3:0]			
W								
R	CMD_SEL		OPT[1:0][1]		INTFLG_SEL[3:0]			
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 10-18. ADC Command Register 0 (ADCCMD_0)

[1] Only available on ADC12B_LBA V2 and V3 (see Table 10-2 for details)

Read: Anytime

Write: Only writable if bit SMOD_ACC is set
(see also Section 10.5.2.2, “ADC Control Register 1 (ADCCTL_1) bit SMOD_ACC description for more details)

Table 10-20. ADCCMD_0 Field Descriptions

Field	Description
31-30 CMD_SEL[1:0]	**Conversion Command Select Bits** — These bits define the type of current conversion described in Table 10-21.
	ADC12B_LBA V2 and V3 (includes OPT[1:0])
29-28 OPT[1:0]	**Option Bits** — These two option bits can be used to control a SoC level feature/function. These bits are used together with Option bits OPT[2:3]. Please refer to the device reference manual for details of the feature/functionality controlled by these bits
27-24 INTFLG_SEL[3:0]	**Conversion Interrupt Flag Select Bits** — These bits define which interrupt flag is set in the ADCIFH/L register at the end of current conversion.The interrupt flags ADCIF[15:1] are selected via binary coded bits INTFLG_SEL[3:0]. See also Table 10-22

NOTE

If bit SMOD_ACC is set modifying this register must be done carefully - only when no conversion and conversion sequence is ongoing.

Table 10-21. Conversion Command Type Select

CMD_SEL[1]	CMD_SEL[0]	Conversion Command Type Description
0	0	Normal Conversion
0	1	End Of Sequence (Wait for Trigger to execute next sequence or for a Restart)

10.5.2.19 ADC Command Index Register (ADCCIDX)

It is important to note that these bits do not represent absolute addresses instead it is a sample index (object size 32bit).

Module Base + 0x001C

	7	6	5	4	3	2	1	0
R	0	0	CMD_IDX[5:0]					
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 10-22. ADC Command Index Register (ADCCIDX)

Read: Anytime

Write: NA

Table 10-27. ADCCIDX Field Descriptions

Field	Description
5-0 CMD_IDX [5:0]	**ADC Command Index Bits** — These bits represent the command index value for the conversion commands relative to the two CSL start addresses in the memory map. These bits do not represent absolute addresses instead it is a sample index (object size 32bit). See also Section 10.6.3.2.2, “Introduction of the two Command Sequence Lists (CSLs) for more details.

Address Offset / Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0002 PGAGAIN	R	0	0	0	0	PGAGAIN[3:0]			
	W								
0x0003 PGAOFFSET	R	0		PGAOFFSET[5:0]					
	W								
0x0004-0x0006 Reserved	R	0	0	0	0	0	0	0	0
	W								
0x0007 Reserved	R	0	0	0	0	0	Reserved	Reserved	Reserved
	W								

= Unimplemented

Figure 12-2. PGA Register Summary

12.3.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

12.3.2.1 PGA Enable Register (PGAEN)

Module Base + 0x0000 — Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0		PGAOFFSCEN	PGAEN
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented

Figure 12-3. PGA Enable Register (PGAEN)

[1] Read: Anytime
Write: Anytime

Table 13-12. CANRIER Register Field Descriptions

Field	Description
7 WUPIE[1]	**Wake-Up Interrupt Enable** 0 No interrupt request is generated from this event. 1 A wake-up event causes a Wake-Up interrupt request.
6 CSCIE	**CAN Status Change Interrupt Enable** 0 No interrupt request is generated from this event. 1 A CAN Status Change event causes an error interrupt request.
5-4 RSTATE[1:0]	**Receiver Status Change Enable** — These RSTAT enable bits control the sensitivity level in which receiver state changes are causing CSCIF interrupts. Independent of the chosen sensitivity level the RSTAT flags continue to indicate the actual receiver state and are only updated if no CSCIF interrupt is pending. 00 Do not generate any CSCIF interrupt caused by receiver state changes. 01 Generate CSCIF interrupt only if the receiver enters or leaves “bus-off” state. Discard other receiver state changes for generating CSCIF interrupt. 10 Generate CSCIF interrupt only if the receiver enters or leaves “RxErr” or “bus-off”[2] state. Discard other receiver state changes for generating CSCIF interrupt. 11 Generate CSCIF interrupt on all state changes.
3-2 TSTATE[1:0]	**Transmitter Status Change Enable** — These TSTAT enable bits control the sensitivity level in which transmitter state changes are causing CSCIF interrupts. Independent of the chosen sensitivity level, the TSTAT flags continue to indicate the actual transmitter state and are only updated if no CSCIF interrupt is pending. 00 Do not generate any CSCIF interrupt caused by transmitter state changes. 01 Generate CSCIF interrupt only if the transmitter enters or leaves “bus-off” state. Discard other transmitter state changes for generating CSCIF interrupt. 10 Generate CSCIF interrupt only if the transmitter enters or leaves “TxErr” or “bus-off” state. Discard other transmitter state changes for generating CSCIF interrupt. 11 Generate CSCIF interrupt on all state changes.
1 OVRIE	**Overrun Interrupt Enable** 0 No interrupt request is generated from this event. 1 An overrun event causes an error interrupt request.
0 RXFIE	**Receiver Full Interrupt Enable** 0 No interrupt request is generated from this event. 1 A receive buffer full (successful message reception) event causes a receiver interrupt request.

1 WUPIE and WUPE (see Section 13.3.2.1, “MSCAN Control Register 0 (CANCTL0)”) must both be enabled if the recovery mechanism from stop or wait is required.

2 Bus-off state is only defined for transmitters by the CAN standard (see Bosch CAN 2.0A/B protocol specification). Because the only possible state change for the transmitter from bus-off to TxOK also forces the receiver to skip its current state to RxOK, the coding of the RXSTAT[1:0] flags define an additional bus-off state for the receiver (see Section 13.3.2.5, “MSCAN Receiver Flag Register (CANRFLG)”).

13.3.2.7 MSCAN Transmitter Flag Register (CANTFLG)

The transmit buffer empty flags each have an associated interrupt enable bit in the CANTIER register.

Table 13-25. Message Buffer Organization

Offset Address	Register	Access
0x00X0	IDR0 — Identifier Register 0	R/W
0x00X1	IDR1 — Identifier Register 1	R/W
0x00X2	IDR2 — Identifier Register 2	R/W
0x00X3	IDR3 — Identifier Register 3	R/W
0x00X4	DSR0 — Data Segment Register 0	R/W
0x00X5	DSR1 — Data Segment Register 1	R/W
0x00X6	DSR2 — Data Segment Register 2	R/W
0x00X7	DSR3 — Data Segment Register 3	R/W
0x00X8	DSR4 — Data Segment Register 4	R/W
0x00X9	DSR5 — Data Segment Register 5	R/W
0x00XA	DSR6 — Data Segment Register 6	R/W
0x00XB	DSR7 — Data Segment Register 7	R/W
0x00XC	DLR — Data Length Register	R/W
0x00XD	TBPR — Transmit Buffer Priority Register[1]	R/W
0x00XE	TSRH — Time Stamp Register (High Byte)	R
0x00XF	TSRL — Time Stamp Register (Low Byte)	R

[1] Not applicable for receive buffers

Figure 13-23 shows the common 13-byte data structure of receive and transmit buffers for extended identifiers. The mapping of standard identifiers into the IDR registers is shown in Figure 13-24.

All bits of the receive and transmit buffers are ‘x’ out of reset because of RAM-based implementation[1]. All reserved or unused bits of the receive and transmit buffers always read ‘x’.

1. Exception: The transmit buffer priority registers are 0 out of reset.

Table 14-5. BATIF Register Field Descriptions

Field	Description
1 BVHIF	**BATSV3 Interrupt Flag High Detect** — The flag is set to 1 when BVHC status bit changes. 0 No change of the BVHC status bit since the last clearing of the flag. 1 BVHC status bit has changed since the last clearing of the flag.
0 BVLIF	**BATSV3 Interrupt Flag Low Detect** — The flag is set to 1 when BVLC status bit changes. 0 No change of the BVLC status bit since the last clearing of the flag. 1 BVLC status bit has changed since the last clearing of the flag.

14.3.2.5 Reserved Register

Module Base + 0x0006
Module Base + 0x0007

Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset	x	x	x	x	x	x	x	x

Figure 14-8. Reserved Register

[1] Read: Anytime
Write: Only in special mode

NOTE

These reserved registers are designed for factory test purposes only and are not intended for general user access. Writing to these registers when in special mode can alter the module's functionality.

14.4 Functional Description

14.4.1 General

The BATS module allows measuring the voltage on the VSUP pin. The voltage at the VSUP pin can be routed via an internal voltage divider to an internal Analog to Digital Converter Channel. Also the BATS module can be configured to generate a low and high voltage interrupt based on VSUP. The trigger level of the high and low interrupt are selectable.

14.4.2 Interrupts

This section describes the interrupt generated by the BATS module. The interrupt is only available in CPU run mode. Entering and exiting CPU stop mode has no effect on the interrupt flags.

To make sure the interrupt generation works properly the bus clock frequency must be higher than the Voltage Warning Low Pass Filter frequency (f_{VWLP_filter}).

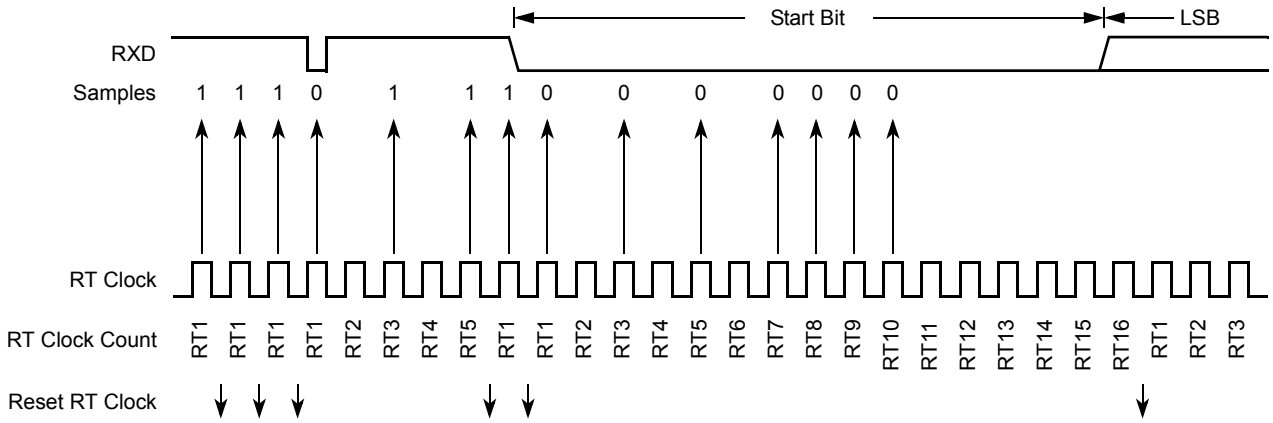


Figure 18-22. Start Bit Search Example 1

In Figure 18-23, verification sample at RT3 is high. The RT3 sample sets the noise flag. Although the perceived bit time is misaligned, the data samples RT8, RT9, and RT10 are within the bit time and data recovery is successful.

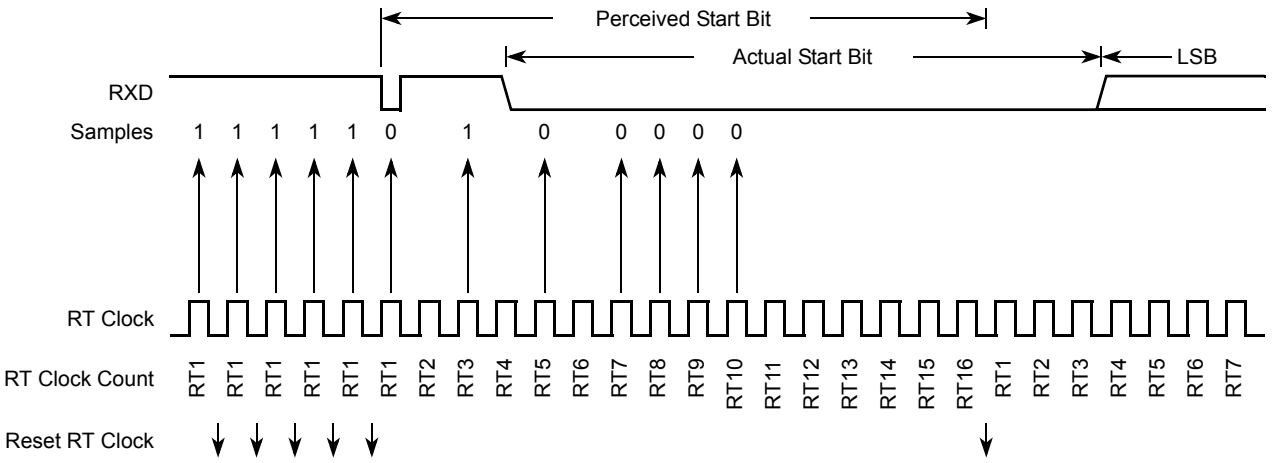


Figure 18-23. Start Bit Search Example 2

In Figure 18-24, a large burst of noise is perceived as the beginning of a start bit, although the test sample at RT5 is high. The RT5 sample sets the noise flag. Although this is a worst-case misalignment of perceived bit time, the data samples RT8, RT9, and RT10 are within the bit time and data recovery is successful.

19.3.2.5 SPI Data Register (SPIDR = SPIDRH:SPIDRL)

Module Base +0x0004

	7	6	5	4	3	2	1	0
R	R15	R14	R13	R12	R11	R10	R9	R8
W	T15	T14	T13	T12	T11	T10	T9	T8
Reset	0	0	0	0	0	0	0	0

Figure 19-7. SPI Data Register High (SPIDRH)

Module Base +0x0005

	7	6	5	4	3	2	1	0
R	R7	R6	R5	R4	R3	R2	R1	R0
W	T7	T6	T5	T4	T3	T2	T1	T0
Reset	0	0	0	0	0	0	0	0

Figure 19-8. SPI Data Register Low (SPIDRL)

Read: Anytime; read data only valid when SPIF is set

Write: Anytime

The SPI data register is both the input and output register for SPI data. A write to this register allows data to be queued and transmitted. For an SPI configured as a master, queued data is transmitted immediately after the previous transmission has completed. The SPI transmitter empty flag SPTEF in the SPISR register indicates when the SPI data register is ready to accept new data.

Received data in the SPIDR is valid when SPIF is set.

If SPIF is cleared and data has been received, the received data is transferred from the receive shift register to the SPIDR and SPIF is set.

If SPIF is set and not serviced, and a second data value has been received, the second received data is kept as valid data in the receive shift register until the start of another transmission. The data in the SPIDR does not change.

If SPIF is set and valid data is in the receive shift register, and SPIF is serviced before the start of a third transmission, the data in the receive shift register is transferred into the SPIDR and SPIF remains set (see Figure 19-9).

If SPIF is set and valid data is in the receive shift register, and SPIF is serviced after the start of a third transmission, the data in the receive shift register has become invalid and is not transferred into the SPIDR (see Figure 19-10).

22.4.7.3 Erase Verify P-Flash Section Command

The Erase Verify P-Flash Section command will verify that a section of code in the P-Flash memory is erased. The Erase Verify P-Flash Section command defines the starting point of the code to be verified and the number of phrases.

Table 22-36. Erase Verify P-Flash Section Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x03	Global address [23:16] of a P-Flash block
FCCOB1	Global address [15:0] of the first phrase to be verified	
FCCOB2	Number of phrases to be verified	

Upon clearing CCIF to launch the Erase Verify P-Flash Section command, the Memory Controller will verify the selected section of Flash memory is erased. The CCIF flag will set after the Erase Verify P-Flash Section operation has completed. If the section is not erased, it means blank check failed, both MGSTAT bits will be set.

Table 22-37. Erase Verify P-Flash Section Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command not available in current mode (see Table 22-28)
		Set if an invalid global address [23:0] is supplied see Table 22-2)
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
		Set if the requested section crosses a the P-Flash address boundary
	FPVIOL	None
	MGSTAT1	Set if any errors have been encountered during the read or if blank check failed.
	MGSTAT0	Set if any non-correctable errors have been encountered during the read or if blank check failed.

22.4.7.4 Read Once Command

The Read Once command provides read access to a reserved 64 byte field (8 phrases) located in the nonvolatile information register of P-Flash. The Read Once field is programmed using the Program Once command described in Section 22.4.7.6. The Read Once command must not be executed from the Flash block containing the Program Once reserved field to avoid code runaway.

Table 22-38. Read Once Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x04	Not Required
FCCOB1	Read Once phrase index (0x0000 - 0x0007)	
FCCOB2	Read Once word 0 value	

The erase-all function requires the clock divider register FCLKDIV (see Section 22.3.2.1) to be loaded before invoking this function using *soc_erase_all_req* input pin. The FCLKDIV configuration for this feature is described at device level. If FCLKDIV is not properly set the erase-all operation will not execute and the ACCERR flag in FSTAT register will set. After the execution of the erase-all function the FCLKDIV register will be reset and the value of register FCLKDIV must be loaded before launching any other command afterwards.

Before invoking the erase-all function using the *soc_erase_all_req* pin, the ACCERR and FPVIOL flags in the FSTAT register must be clear. When invoked from *soc_erase_all_req* the erase-all function will erase all P-Flash memory and EEPROM memory space regardless of the protection settings. If the post-erase verify passes, the routine will then release security by setting the SEC field of the FSEC register to the unsecure state (see Section 22.3.2.2). The security byte in the Flash Configuration Field will be programmed to the unsecure state (see Table 22-8). The status of the erase-all request is reflected in the ERSAREQ bit in the FCNFG register (see Section 22.3.2.5). The ERSAREQ bit in FCNFG will be cleared once the operation has completed and the normal FSTAT error reporting will be available as described inTable 22-46.

At the end of the erase-all sequence Protection will remain configured as it was before executing the erase-all function. If the application requires programming P-Flash and/or EEPROM after the erase-all function completes, the existing protection limits must be taken into account. If protection needs to be disabled the user may need to reset the system right after completing the erase-all function.

Table 22-46. Erase All Pin Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if command not available in current mode (see Table 22-28)
	MGSTAT1	Set if any errors have been encountered during the erase verify operation, or during the program verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the erase verify operation, or during the program verify operation

22.4.7.8 Erase Flash Block Command

The Erase Flash Block operation will erase all addresses in a P-Flash or EEPROM block.

Table 22-47. Erase Flash Block Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x09	Global address [23:16] to identify Flash block
FCCOB1	Global address [15:0] in Flash block to be erased	

Upon clearing CCIF to launch the Erase Flash Block command, the Memory Controller will erase the selected Flash block and verify that it is erased. The CCIF flag will set after the Erase Flash Block operation has completed.

Table 22-56. Valid Set User Margin Level Settings

FCCOB2	Level Description
0x0000	Return to Normal Level
0x0001	User Margin-1 Level[1]
0x0002	User Margin-0 Level[2]

1 Read margin to the erased state

2 Read margin to the programmed state

Table 22-57. Set User Margin Level Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 010 at command launch
		Set if command not available in current mode (see Table 22-28)
		Set if an invalid global address [23:0] is supplied see Table 22-2)
		Set if an invalid margin level setting is supplied
	FPVIOL	None
	MGSTAT1	None
	MGSTAT0	None

NOTE

User margin levels can be used to check that Flash memory contents have adequate margin for normal level read operations. If unexpected results are encountered when checking Flash memory contents at user margin levels, a potential loss of information has been detected.

22.4.7.13 Set Field Margin Level Command

The Set Field Margin Level command, valid in special modes only, causes the Memory Controller to set the margin level specified for future read operations of the P-Flash or EEPROM block.

Table 22-58. Set Field Margin Level Command FCCOB Requirements

Register	FCCOB Parameters	
FCCOB0	0x0E	Global address [23:16] to identify Flash block
FCCOB1	Global address [15:0] to identify Flash block	
FCCOB2	Margin level setting.	

Upon clearing CCIF to launch the Set Field Margin Level command, the Memory Controller will set the field margin level for the targeted block and then set the CCIF flag.

Appendix H
PGA Electrical Specifications

This section describe the electrical characteristics of the PGA module.

H.1 Static Electrical Characteristics

Table H-1. Static Electrical Characteristics - PGA

Supply voltage 4.85V ≤ V_{DDA} ≤ 5.15 V, -40^{o}C < T_J < 150^{o}C						
Num	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	Settling time	$t_{PGA\_settling}$		5	10	us
2	Common mode voltage input range	V_{CM}	1.5		V_{DDA} - 1.5	V
3	DC Gain Error for gain A_{PGA}	E_A	-2.5		1.0	%
4	Initial input offset	$V_{initial\_offset}$	-10.0		10.0	mV
5	Input offset difference to offset at room temperature	V_{var_offset}	-2	-	2	mV
6	Current consumption	I_{PGA}		1		mA
7	Supply voltage	V_{DDA}	4.5	5.0	5.5	V
8	output voltage range	V_{OUT}	0.5		V_{DDA}-0.5	V

O.11 0x05C0-0x05FF TIM0 (continued)

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x05D7	TIM0TC3L	R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05D8	TIM0TC4H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x05D9	TIM0TC4L	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x05DA	TIM0TC5H	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x05DB	TIM0TC5L	R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0x05DC– 0x05EB	Reserved	R W								
0x05EC	TIM0OCPD	R W	RESERVED	RESERVED	OCPD5	OCPD4	OCPD3	OCPD2	OCPD1	OCPD0
0x05ED	Reserved	R W								
0x05EE	TIM0PTPSR	R W	PTPS7	PTPS6	PTPS5	PTPS4	PTPS3	PTPS2	PTPS1	PTPS0
0x05EF	Reserved	R W								

O.12 0x0600-0x063F ADC0

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0600	ADC0CTL_0	R W	ADC_EN	ADC_SR	FRZ_MOD	SWAI	ACC_CFG[1:0]		STR_SEQA	MOD_CFG
0x0601	ADC0CTL_1	R W	CSL_BMOD	RVL_BMOD	SMOD_ACC	AUT_RSTA	0	0	0	0
0x0602	ADC0STS	R W	CSL_SEL	RVL_SEL	DBECC_ERR	Reserved	READY	0	0	0
0x0603	ADC0TIM	R W	0	PRS[6:0]						
0x0604	ADC0FMT	R W	DJM	0	0	0	0	SRES[2:0]		
0x0605	ADC0FLWCTL	R W	SEQA	TRIG	RSTA	LDOK	0	0	0	0
0x0606	ADC0EIE	R W	IA_EIE	CMD_EIE	EOL_EIE	Reserved	TRIG_EIE	RSTAR_EIE	LDOK_EIE	0
0x0607	ADC0IE	R W	SEQAD_IE	CONIF_OIE	Reserved	0	0	0	0	0