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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SCI, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	19
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	5.5V ~ 18V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=s9s12zvl16f0vlc

Chapter 14
Supply Voltage Sensor (BATSV3)

Chapter 15
Timer Module (TIM16B6CV3)

Chapter 16
Timer Module (TIM16B2CV3)

The MC9S12ZVL-Family is a general-purpose family of devices suitable for a wide range of applications. The MC9S12ZVL-Family is targeted at generic automotive applications requiring LIN connectivity. Typical examples of these applications include switch panels and body endpoints for sensors.

1.2 Features

This section describes the key features of the MC9S12ZVL-Family.

1.2.1 MC9S12ZVL-Family Member Comparison

Table 1-2 provides a summary of main features within the MC9S12ZVL-Family.

Table 1-2. MC9S12ZVL-Family Comparison

Feature	MC9S12ZVL128 MC9S12ZVLA128	MC9S12ZVL96 MC9S12ZVLA96	MC9S12ZVL64 MC9S12ZVLA64	MC9S12ZVL32	MC9S12ZVL16	MC9S12ZVL8	MC9S12ZVLS32	MC9S12ZVLS16
Flash memory (ECC) [KB]	128	96	64	32	16	8	32	16
EEPROM (ECC) [Byte]	2048		1024	128			128	
RAM (ECC) [Byte]	8192		4096	1024	1024	512	1024	
max bus clock	32 MHz			32 MHz			32 MHz	
HVI	1			1			1	
LIN Physical layer	1			1			1	
Vreg current capability[1] - 70 mA (VDDX) - 170 mA ballast option (BCTL) - tolerance - 3.3V VDDX support, see also: 9.3.2.27, “Voltage Regulator Control Register (CPMUVREGCTL)	yes yes 3% / 2%[2] yes			yes yes 3% no			yes yes 3% no	
ASIL SEooC target	A			A			A	
Package	48-pin / 32-pin LQFP / 32-pin QFN-EP			48-pin / 32-pin LQFP			32-pin QFN-EP	
ADC channels -10-bit -12-bit	10[3] / 6 10[3][2] / 6[2]			10[3] / 6 -			6 -	
PWM	8 16 bit Channels			8 Channel (up to 4 16 bit)			8 Channel (up to 4 16 bit)	
DAC	1[4][2]			-			-	
PGA[5]	1[2]			-			-	
ACMP	1[2]			-			-	
Timer	6 + 2 channel			6 + 2 channel			6 + 2 channel	

Port	Pin	Pin Function & Priority	I/O	Description	Routing Register Bit	Pin Function after Reset
AD	PAD7	AMPP (DAC)	I	DAC AMP non-inverting input (+)	—	GPIO
		AN7	I	ADC0 analog input	—	
		PTADL[7]/ KWADL[7]	I/O	General-purpose; with interrupt and key-wakeup	—	
	PAD6	AMP (DAC)	O	DAC AMP output	—	
		AN6	I	ADC0 analog input	—	
		PTADL[6]/ KWADL[6]	I/O	General-purpose; with interrupt and key-wakeup	—	
	PAD5	AN5	I	ADC0 analog input	—	
		(ETRIG0)	I	ADC0 external trigger	TRIG0RR2-0	
		PTADL[5]/ KWADL[5]	I/O	General-purpose; with interrupt and key-wakeup	—	
	PAD4	ACMP_1	I	ACMP input 1 (to mux)	—	
		AN4	I	ADC0 analog input	—	
		PTADL[4]/ KWADL[4]	I/O	General-purpose; with interrupt and key-wakeup	—	
	PAD3	PGA_IN1	I	PGA input option 1	—	
		AN3	I	ADC0 analog input	—	
		PTADL[3]/ KWADL[3]	I/O	General-purpose; with interrupt and key-wakeup	—	
	PAD2	PGA_IN0	I	PGA input option 0	—	
		AN2	I	ADC0 analog input	—	
		PTADL[2]/ KWADL[2]	I/O	General-purpose; with interrupt and key-wakeup	—	
	PAD1	PGA_REF	I	PGA reference input	—	
		VRL	I	ADC0 voltage reference low	—	
		AN1	I	ADC0 analog input	—	
		PTADL[1]/ KWADL[1]	I/O	General-purpose; with interrupt and key-wakeup	—	
	PAD0	ACMP_0	I	ACMP input 0	—	
		VRH	I	ADC0 voltage reference high	—	
		AN0	I	ADC0 analog input	—	
		PTADL[0]/ KWADL[0]	I/O	General-purpose; with interrupt and key-wakeup	—	

3.6.2 Register Descriptions

3.6.2.1 ACMP Control Register 0 (ACMPC0)

Module Base + 0x0000 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	ACE	ACOPE	ACOPS	ACDLY	ACHYS1-0		ACMOD1-0	
Reset	0	0	0	0	0	0	0	0

Figure 3-2. ACMP Control Register (ACMPC0)

[1] Read: Anytime
Write: Anytime

Table 3-2. ACMPC0 Register Field Descriptions

Field	Description
7 ACE	**ACMP Enable —** This bit enables the ACMP module. When set the related input pins are connected with the low pass input filters. **Note:** After setting ACE to 1 an initialization delay of 127 bus clock cycles must be accounted for. During this time the comparator output path to all subsequent logic (ACO, ACIF, timer link) is held at its current state. When setting ACE to 0 the current state of the comparator will be maintained.For ACMPO a delay of $t_{ACMP\_delay\_en}$ must be accounted for. 0 ACMP disabled 1 ACMP enabled
6 ACOPE	**ACMP Output Pin Enable —** This bit enables the ACMP output on external ACMPO pin. 0 ACMP output pin disabled 1 ACMP output is driven out to ACMPO
5 ACOPS	**ACMP Output Polarity Select** — This bit selects the output polarity on ACMPO. 0 ACMPO is ACMP output 1 ACMPO is ACMP output inverted
4 ACDLY	**ACMP Input Filter Select for Inputs ACMP_0 and ACMP_1** — This bit selects the analog input filter characteristics resulting in a signal propagation delay of t_{ACMP_delay}. 0 Select input filter with low speed characteristics 1 Select input filter with high speed characteristics

Table 5-10. Field Location to Byte Access Mapping

Address[1:0]	Access Size	00	01	10	11	Note
00	32-bit	Data[31:24]	Data[23:16]	Data [15:8]	Data [7:0]	
01	32-bit	Data[31:24]	Data[23:16]	Data [15:8]	Data [7:0]	Realigned
10	32-bit	Data[31:24]	Data[23:16]	Data [15:8]	Data [7:0]	Realigned
11	32-bit	Data[31:24]	Data[23:16]	Data [15:8]	Data [7:0]	Realigned
00	16-bit	Data [15:8]	Data [7:0]			
01	16-bit		Data [15:8]	Data [7:0]		
10	16-bit			Data [15:8]	Data [7:0]	
11	16-bit			Data [15:8]	Data [7:0]	Realigned
00	8-bit	Data [7:0]				
01	8-bit		Data [7:0]			
10	8-bit			Data [7:0]		
11	8-bit				Data [7:0]	
			Denotes byte that is not transmitted			

5.4.5.2.1 FILL_MEM and DUMP_MEM Increments and Alignment

FILL_MEM and DUMP_MEM increment the previously accessed address by the previous access size to calculate the address of the current access. On misaligned longword accesses, the address bits [1:0] are forced to zero, therefore the following FILL_MEM or DUMP_MEM increment to the first address in the next 4-byte field. This is shown in Table 5-11, the address of the first DUMP_MEM.32 following READ_MEM.32 being calculated from 0x004000+4.

When misaligned word accesses are realigned, then the original address (not the realigned address) is incremented for the following FILL_MEM, DUMP_MEM command.

Misaligned word accesses can cause the same locations to be read twice as shown in rows 6 and 7. The hardware ensures alignment at an attempted misaligned word access across a 4-byte boundary, as shown in row 7. The following word access in row 8 continues from the realigned address of row 7.

Table 5-11. Consecutive Accesses With Variable Size

Row	Command	Address	Address[1:0]	00	01	10	11
1	READ_MEM.32	0x004003	11	Accessed	Accessed	Accessed	Accessed
2	DUMP_MEM.32	0x004004	00	Accessed	Accessed	Accessed	Accessed
3	DUMP_MEM.16	0x004008	00	Accessed	Accessed		
4	DUMP_MEM.16	0x00400A	10			Accessed	Accessed
5	DUMP_MEM.08	0x00400C	00	Accessed			
6	DUMP_MEM.16	0x00400D	01		Accessed	Accessed	
7	DUMP_MEM.16	0x00400E	10			Accessed	Accessed
8	DUMP_MEM.16	0x004010	01	Accessed	Accessed		

7.3.2.14 Debug Comparator D Control Register (DBGDCTL)

Address: 0x0140

	7	6	5	4	3	2	1	0
R	0	0	INST	0	RW	RWE	reserved	COMPE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 7-17. Debug Comparator D Control Register

Read: Anytime.

Write: If DBG not armed.

Table 7-24. DBGDCTL Field Descriptions

Field[1]	Description
5 INST	**Instruction Select** — This bit configures the comparator to compare PC or data access addresses. 0 Comparator compares addresses of data accesses 1 Comparator compares PC address
3 RW	**Read/Write Comparator Value Bit** — The RW bit controls whether read or write is used in compare for the associated comparator. The RW bit is ignored if RWE is clear or INST is set. 0 Write cycle is matched 1 Read cycle is matched
2 RWE	**Read/Write Enable Bit** — The RWE bit controls whether read or write comparison is enabled for the associated comparator. This bit is ignored if INST is set. 0 Read/Write is not used in comparison 1 Read/Write is used in comparison
0 COMPE	**Enable Bit** — Determines if comparator is enabled 0 The comparator is not enabled 1 The comparator is enabled

1 If the CDCM field selects range mode comparisons, then DBGCCTL bits configure the comparison, DBGDCTL is ignored.

Table 7-25 shows the effect for RWE and RW on the comparison conditions. These bits are ignored if INST is set, because matches based on opcodes reaching the execution stage are data independent.

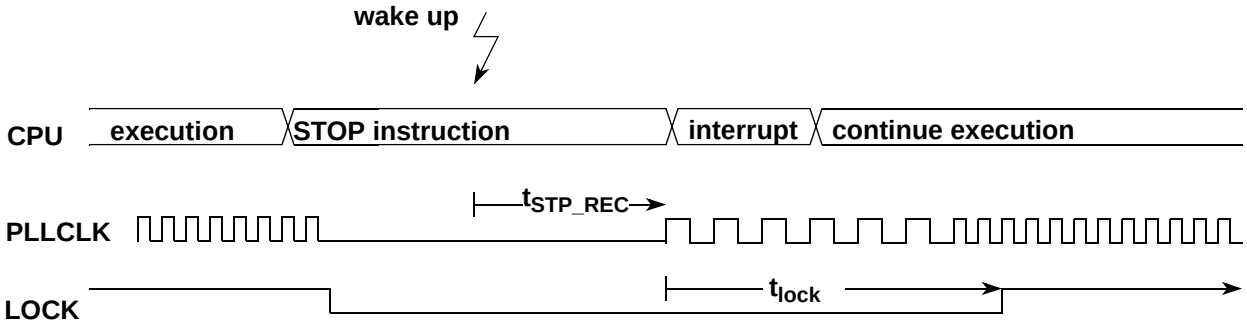
Table 7-25. Read or Write Comparison Logic Table

RWE Bit	RW Bit	RW Signal	Comment
0	x	0	RW not used in comparison
0	x	1	RW not used in comparison
1	0	0	Write match
1	0	1	No match
1	1	0	No match
1	1	1	Read match

9.4.3 Stop Mode using PLLCLK as source of the Bus Clock

An example of what happens going into Stop Mode and exiting Stop Mode after an interrupt is shown in Figure 9-39. Disable PLL Lock interrupt (LOCKIE=0) before going into Stop Mode.

Figure 9-39. Stop Mode using PLLCLK as source of the Bus Clock



Depending on the COP configuration there might be an additional significant latency time until COP is active again after exit from Stop Mode due to clock domain crossing synchronization. This latency time occurs if COP clock source is ACLK and the CSAD bit is set (please refer to CSAD bit description for details).

9.4.4 Full Stop Mode using Oscillator Clock as source of the Bus Clock

An example of what happens going into Full Stop Mode and exiting Full Stop Mode after an interrupt is shown in Figure 9-40.

Disable PLL Lock interrupt (LOCKIE=0) and oscillator status change interrupt (OSCIE=0) before going into Full Stop Mode.

[1] Read: Anytime
Write: Anytime when not in initialization mode

NOTE

The CANTIER register is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK = 1). This register is writable when not in initialization mode (INITRQ = 0 and INITAK = 0).

Table 13-14. CANTIER Register Field Descriptions

Field	Description
2-0 TXEIE[2:0]	**Transmitter Empty Interrupt Enable** 0 No interrupt request is generated from this event. 1 A transmitter empty (transmit buffer available for transmission) event causes a transmitter empty interrupt request.

13.3.2.9 MSCAN Transmitter Message Abort Request Register (CANTARQ)

The CANTARQ register allows abort request of queued messages as described below.

Module Base + 0x0008 Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 13-12. MSCAN Transmitter Message Abort Request Register (CANTARQ)

[1] Read: Anytime
Write: Anytime when not in initialization mode

NOTE

The CANTARQ register is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK = 1). This register is writable when not in initialization mode (INITRQ = 0 and INITAK = 0).

Table 13-15. CANTARQ Register Field Descriptions

Field	Description
2-0 ABTRQ[2:0]	**Abort Request** — The CPU sets the ABTRQx bit to request that a scheduled message buffer (TXEx = 0) be aborted. The MSCAN grants the request if the message has not already started transmission, or if the transmission is not successful (lost arbitration or error). When a message is aborted, the associated TXE (see Section 13.3.2.7, “MSCAN Transmitter Flag Register (CANTFLG)”) and abort acknowledge flags (ABTAK, see Section 13.3.2.10, “MSCAN Transmitter Message Abort Acknowledge Register (CANTAAK)”) are set and a transmit interrupt occurs if enabled. The CPU cannot reset ABTRQx. ABTRQx is reset whenever the associated TXE flag is set. 0 No abort request 1 Abort request pending

Table 20-9. IBSR Field Descriptions (continued)

Field	Description
3 RESERVED	**Reserved** — Bit 3 of IBSR is reserved for future use. A read operation on this bit will return 0.
2 SRW	**Slave Read/Write** — When IAAS is set this bit indicates the value of the R/W command bit of the calling address sent from the master This bit is only valid when the I-bus is in slave mode, a complete address transfer has occurred with an address match and no other transfers have been initiated. Checking this bit, the CPU can select slave transmit/receive mode according to the command of the master. 0 Slave receive, master writing to slave 1 Slave transmit, master reading from slave
1 IBIF	**I-Bus Interrupt** — The IBIF bit is set when one of the following conditions occurs: — Arbitration lost (IBAL bit set) — Data transfer complete (TCF bit set) — Addressed as slave (IAAS bit set) It will cause a processor interrupt request if the IBIE bit is set. This bit must be cleared by software, writing a one to it. A write of 0 has no effect on this bit.
0 RXAK	**Received Acknowledge** — The value of SDA during the acknowledge bit of a bus cycle. If the received acknowledge bit (RXAK) is low, it indicates an acknowledge signal has been received after the completion of 8 bits data transmission on the bus. If RXAK is high, it means no acknowledge signal is detected at the 9th clock. 0 Acknowledge received 1 No acknowledge received

20.3.1.5 IIC Data I/O Register (IBDR)

Module Base + 0x0004

	7	6	5	4	3	2	1	0
R W	D7	D6	D5	D4	D3	D2	D1	D0
Reset	0	0	0	0	0	0	0	0

Figure 20-8. IIC Bus Data I/O Register (IBDR)

In master transmit mode, when data is written to the IBDR a data transfer is initiated. The most significant bit is sent first. In master receive mode, reading this register initiates next byte data receiving. In slave mode, the same functions are available after an address match has occurred.Note that the Tx/Rx bit in the IBCR must correctly reflect the desired direction of transfer in master and slave modes for the transmission to begin. For instance, if the IIC is configured for master transmit but a master receive is desired, then reading the IBDR will not initiate the receive.

Reading the IBDR will return the last byte received while the IIC is configured in either master receive or slave receive modes. The IBDR does not reflect every byte that is transmitted on the IIC bus, nor can software verify that a byte has been written to the IBDR correctly by reading it back.

In master transmit mode, the first byte of data written to IBDR following assertion of MS/$\overline{SL}$ is used for the address transfer and should com.prise of the calling address (in position D7:D1) concatenated with the required R/$\overline{W}$ bit (in position D0).

20.4.1.2 Slave Address Transmission

The first byte of data transfer immediately after the START signal is the slave address transmitted by the master. This is a seven-bit calling address followed by a R/W bit. The R/W bit tells the slave the desired direction of data transfer.

1 = Read transfer, the slave transmits data to the master.
0 = Write transfer, the master transmits data to the slave.

If the calling address is 10-bit, another byte is followed by the first byte.Only the slave with a calling address that matches the one transmitted by the master will respond by sending back an acknowledge bit. This is done by pulling the SDA low at the 9th clock (see Figure 20-10).

No two slaves in the system may have the same address. If the IIC bus is master, it must not transmit an address that is equal to its own slave address. The IIC bus cannot be master and slave at the same time.However, if arbitration is lost during an address cycle the IIC bus will revert to slave mode and operate correctly even if it is being addressed by another master.

20.4.1.3 Data Transfer

As soon as successful slave addressing is achieved, the data transfer can proceed byte-by-byte in a direction specified by the R/W bit sent by the calling master

All transfers that come after an address cycle are referred to as data transfers, even if they carry sub-address information for the slave device.

Each data byte is 8 bits long. Data may be changed only while SCL is low and must be held stable while SCL is high as shown in Figure 20-10. There is one clock pulse on SCL for each data bit, the MSB being transferred first. Each data byte has to be followed by an acknowledge bit, which is signalled from the receiving device by pulling the SDA low at the ninth clock. So one complete data byte transfer needs nine clock pulses.

If the slave receiver does not acknowledge the master, the SDA line must be left high by the slave. The master can then generate a stop signal to abort the data transfer or a start signal (repeated start) to commence a new calling.

If the master receiver does not acknowledge the slave transmitter after a byte transmission, it means 'end of data' to the slave, so the slave releases the SDA line for the master to generate STOP or START signal.Note in order to release the bus correctly,after no-acknowledge to the master,the slave must be immediately switched to receiver and a following dummy reading of the IBDR is necessary.

20.4.1.4 STOP Signal

The master can terminate the communication by generating a STOP signal to free the bus. However, the master may generate a START signal followed by a calling command without generating a STOP signal first. This is called repeated START. A STOP signal is defined as a low-to-high transition of SDA while SCL at logical 1 (see Figure 20-10).

The master can generate a STOP even if the slave has generated an acknowledge at which point the slave must release the bus.

Chapter 22
Flash Module (S12ZFTMRZ)

Table 22-1. Revision History

Revision Number	Revision Date	Sections Affected	Description of Changes
V02.03	12 Apr 2012	22.3/22-618	Corrected many typo. Changed caution note
V02.04	17 May 2012	22.3.2.6/22-631	- Removed flag DFDIE
V02.05	11 Jul 2012		- Added explanation about when MGSTAT[1:0] bits are cleared, Section 22.3.2.7 - Added note about possibility of reading P-Flash and EEPROM simultaneously, Section 22.4.6
V02.06	18 Mar 2013		- Standardized nomenclature in references to memory sizes
V02.07	24 May 2013		- Revised references to NVM Resource Area to improve readability
V02.8	12 Jun 2013		- Changed MLOADU Section 22.4.7.12 and MLOADF Section 22.4.7.13 **FCCOB1 to FCCOB2**
V02.9	15 Oct 2014		Created memory-size independent version of this module description

22.1 Introduction

The P-Flash (Program Flash) and EEPROM memory sizes are specified at device level (Reference Manual device overview chapter). The description in the following sections is valid for all P-Flash and EEPROM memory sizes.

The Flash memory is ideal for single-supply applications allowing for field reprogramming without requiring external high voltage sources for program or erase operations. The Flash module includes a memory controller that executes commands to modify Flash memory contents. The user interface to the memory controller consists of the indexed Flash Common Command Object (FCCOB) register which is written to with the command, global address, data, and any required command parameters. The memory controller must complete the execution of a command before the FCCOB register can be written to with a new command.

CAUTION

A Flash word or phrase must be in the erased state before being programmed. Cumulative programming of bits within a Flash word or phrase is not allowed.

The Flash memory may be read as bytes and aligned words. Read access time is one bus cycle for bytes and aligned words. For misaligned words access, the CPU has to perform twice the byte read access command. For Flash memory, an erased bit reads 1 and a programmed bit reads 0.

Upon clearing CCIF to launch the Program P-Flash command, the Memory Controller will program the data words to the supplied global address and will then proceed to verify the data words read back as expected. The CCIF flag will set after the Program P-Flash operation has completed.

Table 22-41. Program P-Flash Command Error Handling

Register	Error Bit	Error Condition
FSTAT	ACCERR	Set if CCOBIX[2:0] != 101 at command launch
		Set if command not available in current mode (see Table 22-28)
		Set if an invalid global address [23:0] is supplied see Table 22-2)
		Set if a misaligned phrase address is supplied (global address [2:0] != 000)
	FPVIOL	Set if the global address [17:0] points to a protected area
	MGSTAT1	Set if any errors have been encountered during the verify operation
	MGSTAT0	Set if any non-correctable errors have been encountered during the verify operation

22.4.7.6 Program Once Command

The Program Once command restricts programming to a reserved 64 byte field (8 phrases) in the nonvolatile information register located in P-Flash. The Program Once reserved field can be read using the Read Once command as described in Section 22.4.7.4. The Program Once command must only be issued once since the nonvolatile information register in P-Flash cannot be erased. The Program Once command must not be executed from the Flash block containing the Program Once reserved field to avoid code runaway.

Table 22-42. Program Once Command FCCOB Requirements

CCOBIX[2:0]	FCCOB Parameters	
FCCOB0	0x07	Not Required
FCCOB1	Program Once phrase index (0x0000 - 0x0007)	
FCCOB2	Program Once word 0 value	
FCCOB3	Program Once word 1 value	
FCCOB4	Program Once word 2 value	
FCCOB5	Program Once word 3 value	

Upon clearing CCIF to launch the Program Once command, the Memory Controller first verifies that the selected phrase is erased. If erased, then the selected phrase will be programmed and then verified with read back. The CCIF flag will remain clear, setting only after the Program Once operation has completed.

The reserved nonvolatile information register accessed by the Program Once command cannot be erased and any attempt to program one of these phrases a second time will not be allowed. Valid phrase index values for the Program Once command range from 0x0000 to 0x0007. During execution of the Program Once command, any attempt to read addresses within P-Flash will return invalid data.

Table B-1. Voltage Regulator Electrical Characteristics

-40°C ≤T_J ≤ 175°C unless noted otherwise, V_{DDA} and V_{DDX} must be shorted on the application board.						
Num	**Characteristic**	**Symbol**	**Min**	**Typical**	**Max**	**Unit**
VDDX=3.3V, VREG5VEN = 1'b0, ZVL(A)128/96/64 only						
6a	Output Voltage V_{DDX}, with external PNP Full Performance Mode V_{SUP} >5.5V[1] Full Performance Mode V_{SUP} >5.5V[4] Full Performance Mode 3.5V <= V_{SUP} <=5.5V Reduced Performance Mode (stopmode) V_{SUP} > =3.5V	V_{DDX}	 3.2 3.23 3.13 2.2	 3.3 3.3 - 3.3	 3.39 3.36 3.39 3.6	V
6b	Output Voltage V_{DDX}, without PNP Full Performance Mode V_{SUP} >5.5V[1] Full Performance Mode V_{SUP} >5.5V[4] Full Performance Mode 3.5V <= V_{SUP} <=5.5V Reduced Performance Mode (stopmode) V_{SUP} > =3.5V	V_{DDX}	 3.18 3.21 3.13 2.2	 3.28 3.28 - 3.3	 3.37 3.35 3.37 3.6	V
7	Load Current V_{DDX}[2,3] without external PNP Full Performance Mode V_{SUP} > 5.5V Full Performance Mode 3.5V <= V_{SUP} <=5.5V Reduced Performance Mode (stopmode)	I_{DDX}	 0 0 0	 - - -	 70 25 5	mA
8	Short Circuit V_{DDX} fall back current V_{DDX} <= 0.5V	I_{DDX}	—	100	—	mA
9	Low Voltage Interrupt Assert Level[5] Low Voltage Interrupt Deassert Level	V_{LVIA} V_{LVID}	4.04 4.19	4.23 4.38	4.40 4.49	V
10a	V_{DDX} Low Voltage Reset deassert[6]	V_{LVRXD}	—	—	3.13	V
10b	V_{DDX} Low Voltage Reset assert	V_{LVRXA}	2.95	3.02	—	V
11	Trimmed ACLK output frequency[7]	f_{ACLK}	—	20	—	KHz
12	Trimmed ACLK internal clock Δf / $f_{nominal}$ [8]	df_{ACLK}	- 6%	—	+ 6%	—
13	The first period after enabling the counter by APIFE might be reduced by API start up delay	t_{sdel}	—	—	100	µs
14	Temperature Sensor Slope	dV_{HT}	5.05	5.25	5.45	mV/°C
15	Temperature Sensor Output Voltage (T_j=150°C)	V_{HT}	—	2.4	—	V
16	High Temperature Interrupt Assert[9] High Temperature Interrupt Deassert	T_{HTIA} T_{HTID}	120 110	132 122	144 134	°C °C
17	Bandgap output voltage	V_{BG}	1.14	1.20	1.28	V
18	V_{BG} voltage variation over input voltage V_{SUP} 3.5V ≤ V_{SUP} ≤ 18V, T_J = 125°C	Δ_{VBGV}	-5		5	mV

Table C-2. ADC Electrical Characteristics

Supply voltage: MC9S12ZVL(S)32\16\8: 3.13V ≤ V_{DDX} ≤ 5.5V, MC9S12ZVL(A)128\96\64: 3.2V ≤ V_{DDX} ≤ 5.15V, -40°C < T_J < 175°C						
Num	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	Max input source resistance[1]	R_S	—	—	1	KΩ
2	Total input capacitance Non sampling Total input capacitance Sampling	C_{INN} C_{INS}	— —	— —	10 16	pF
3	Input internal Resistance	R_{INA}	-	5	15	kΩ
4	Disruptive analog input current	I_{NA}	-2.5	—	2.5	mA
5	Coupling ratio positive current injection	K_p	—	—	1E-4	A/A
6	Coupling ratio negative current injection	K_n	—	—	5E-3	A/A

1 1 Refer to C.1.1.2 for further information concerning source resistance

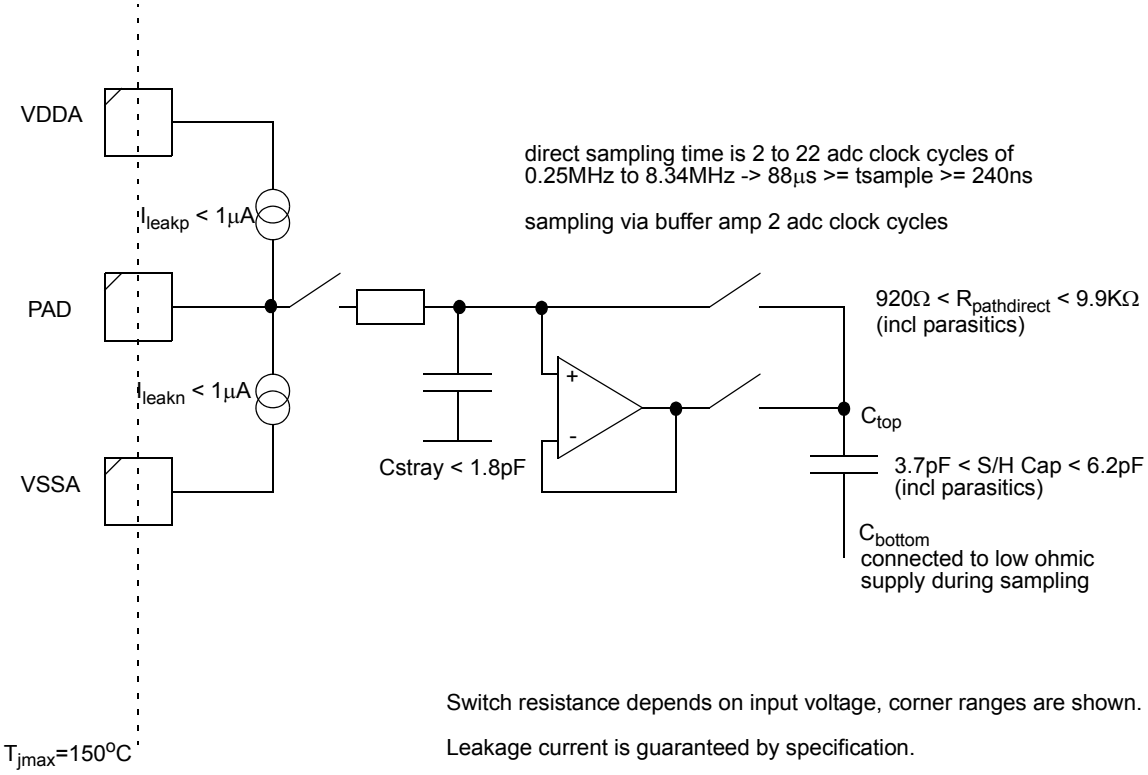


Figure C-1. ADC input logic

Table C-3. ADC Conversion Performance 5V range

Supply voltage:
MC9S12ZVL(S)32\16\8: 4.5V ≤ V_{DDX} ≤ 5.5V, 4.5V ≤ V_{REF} ≤ 5.5V,
MC9S12ZVL(A)128\96\64: 4.85V ≤ V_{DDX} ≤ 5.15V, 4.85V ≤ V_{REF} ≤ 5.15V,
-40°C < T_J < 175°C, V_{REF} = V_{RH} - V_{RL}, f_{ADCCLK} = 8.0MHz
The values are tested to be valid with no port AD output drivers switching simultaneous with conversions.

Num	Rating[1]		Symbol	Min	Typ	Max	Unit
1	Resolution	12-Bit	LSB		1.25		mV
2	Differential Nonlinearity	12-Bit	DNL	-4	±2	4	counts
3	Integral Nonlinearity	12-Bit	INL	-5	±2.5	5	counts
4	Absolute Error[2]	12-Bit	AE	-7	±4	7	counts
5	Resolution	10-Bit	LSB		5		mV
6	Differential Nonlinearity	10-Bit	DNL	-1	±0.5	1	counts
7	Integral Nonlinearity	10-Bit	INL	-2	±1	2	counts
8	Absolute Error[2]	10-Bit	AE	-3	±2	3	counts
9	Resolution	8-Bit	LSB		20		mV
10	Differential Nonlinearity	8-Bit	DNL	-0.5	±0.3	0.5	counts
11	Integral Nonlinearity	8-Bit	INL	-1	±0.5	1	counts
12	Absolute Error[2]	8-Bit	AE	-1.5	±1	1.5	counts

1 The 8-bit and 10-bit mode operation is structurally tested in production test. Absolute values are tested in 12-bit mode.

2 These values include the quantization error which is inherently 1/2 count for any A/D converter.

Table C-4. DC Conversion Performance 3.3V range

Supply voltage MC9S12ZVL(A)128\96\64: 3.20V ≤ V_{DDA} ≤ 3.39V, -40°C < T_J < 175°C. 3.20V ≤ V_{REF} ≤ 3.39V = V_{RH} - V_{RL}.
f_{ADCCLK} = 8.0MHz
The values are tested to be valid with no port AD output drivers switching simultaneous with conversions.

Num	Rating[1]		Symbol	Min	Typ	Max	Unit
1	Resolution	12-Bit	LSB		0.80		mV
2	Differential Nonlinearity	12-Bit	DNL	-6	±3	6	counts
3	Integral Nonlinearity	12-Bit	INL	-7	±3	7	counts
4	Absolute Error[2]	12-Bit	AE	-8	±4	8	counts
5	Resolution	10-Bit	LSB		3.22		mV
6	Differential Nonlinearity	10-Bit	DNL	-1.5	±1	1.5	counts
7	Integral Nonlinearity	10-Bit	INL	-2	±1	2	counts
8	Absolute Error[2]	10-Bit	AE	-3	±2	3	counts
9	Resolution	8-Bit	LSB		12.89		mV
10	Differential Nonlinearity	8-Bit	DNL	-0.5	±0.3	0.5	counts
11	Integral Nonlinearity	8-Bit	INL	-1	±0.5	1	counts
12	Absolute Error[2]	8-Bit	AE	-1.5	±1	1.5	counts

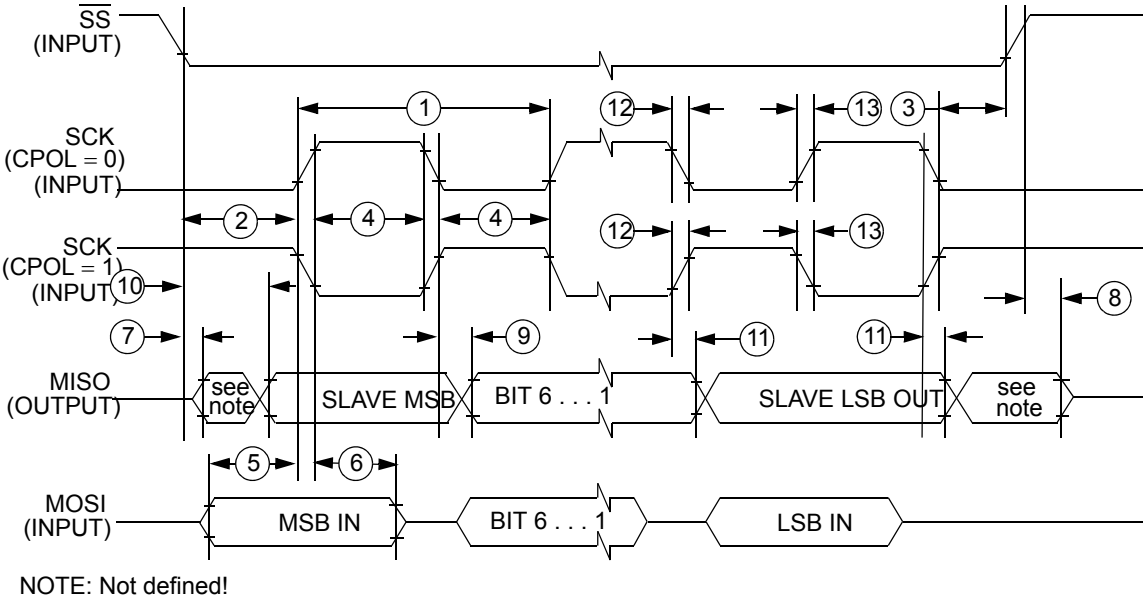


Figure K-3. SPI Slave Timing (CPHA=0)

In Figure K-4 the timing diagram for slave mode with transmission format CPHA=1 is depicted.

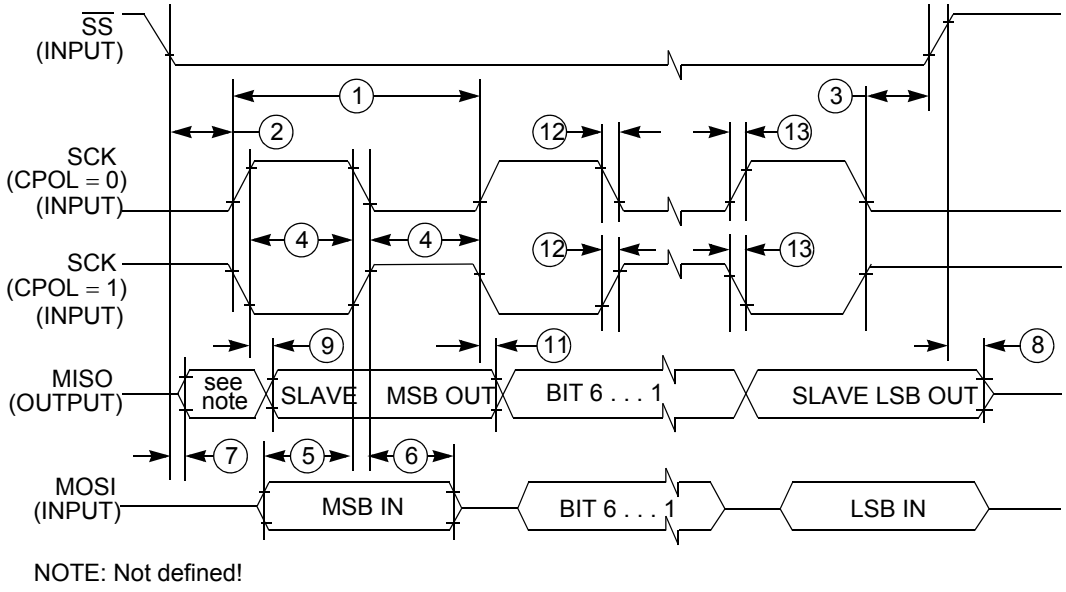


Figure K-4. SPI Slave Timing (CPHA=1)

Appendix L
MSCAN Electrical Specifications

L.1 MSCAN Wake-up Pulse Timing

Table L-1. MSCAN Wake-up Pulse Characteristics (Junction Temperature From –40°C To +175°C)

Conditions are 3.2 V < V_{DDX}< 5.15 V, unless otherwise noted.							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1		MSCAN wake-up dominant pulse filtered	t_{WUP}	—	—	1.5	µs
2		MSCAN wake-up dominant pulse pass	t_{WUP}	5	—	—	µs

O.3 0x0070-0x00FF S12ZMMC

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0070	MODE	R	MODC	0	0	0	0	0	0	0
		W								
0x0071-0x007F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0080	MMCECH	R	ITR[3:0]				TGT[3:0]			
		W								
0x0081	MMCECL	R	ACC[3:0]				ERR[3:0]			
		W								
0x0082	MMCCCRH	R	CPUU	0	0	0	0	0	0	0
		W								
0x0083	MMCCCRL	R	0	CPUX	0	CPUI	0	0	0	0
		W								
0x0084	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0085	MMCPCH	R	CPUPC[23:16]							
		W								
0x0086	MMCPCM	R	CPUPC[15:8]							
		W								
0x0087	MMCPCL	R	CPUPC[7:0]							
		W								
0x0088-0x00FF	Reserved	R	0	0	0	0	0	0	0	0
		W								

O.4 0x0100-0x017F S12ZDBG

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0100	DBGC1	R	ARM	0	reserved	BDMBP	BRKCPU	reserved	EEVE1	0
		W		TRIG						
0x0101	DBGC2	R	0	0	0	0	0	0	ABCM	
		W								
0x0102-0x0106	Reserved	R	0	0	0	0	0	0	0	0
		W								

O.10 0x0500-x052F PWM1 (continued)

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0507	RESERVED	R	0	0	0	0	0	0	0	0
		W								
0x0508	PWMSCLA	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0509	PWMSCLB	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x050A - 0x050B	RESERVED	R	0	0	0	0	0	0	0	0
		W								
0x050C	PWMCNT0	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x050D	PWMCNT1	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x050E	PWMCNT2	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x050F	PWMCNT3	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x0510	PWMCNT4	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x0511	PWMCNT5	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x0512	PWMCNT6	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x0513	PWMCNT7	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x0514	PWMPER0	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0515	PWMPER1	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0516	PWMPER2	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0517	PWMPER3	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0518	PWMPER4	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								

O.12 0x0600-0x063F ADC0 (continued)

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0620	ADC0RIDX	R	0	0	RES_IDX[5:0]					
		W								
0x0621	ADC0RBP_0	R	0	0	0	0	RES_PTR[19:16]			
		W								
0x0622	ADC0RBP_1	R	RES_PTR[15:8]							
		W								
0x0623	ADC0RBP_2	R	RES_PTR[7:2]						0	0
		W								
0x0624	ADC0CROFF0	R	0	CMDRES_OFF0[6:0]						
		W								
0x0625	ADC0CROFF1	R	0	CMDRES_OFF1[6:0]						
		W								
0x0626	Reserved	R	0	0	0	0	Reserved			
		W								
0x0627	Reserved	R	Reserved							
		W								
0x0628	Reserved	R	Reserved						0	0
		W								
0x0629	Reserved	R	Reserved	0	Reserved					
		W								
0x062A-0x063F	Reserved	R	0	0	0	0	0	0	0	0
		W								

O.13 0x0680-0x0687 DAC

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0680	DACCTL	R	FVR	DRIVE	0	0	0	DACM[2:0]		
		W								
0x0681	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0682	DACVOL	R	VOLTAGE[7:0]							
		W								
0x0683-0x0686	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0687	Reserved	R	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
		W								