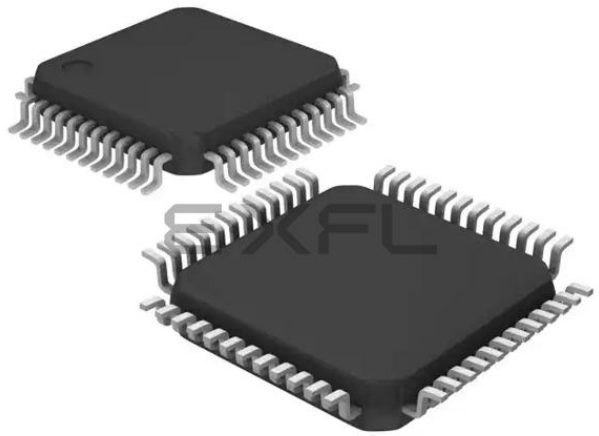

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S12Z
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SCI, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	5.5V ~ 18V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s12zvl32f0clf

Chapter 19
Serial Peripheral Interface (S12SPIV5)

Chapter 20
Inter-Integrated Circuit (IICV3)

Table 1-2. MC9S12ZVL-Family Comparison

Feature	MC9S12ZVL128 MC9S12ZVLA128	MC9S12ZVL96 MC9S12ZVLA96	MC9S12ZVL64 MC9S12ZVLA64	MC9S12ZVL32	MC9S12ZVL16	MC9S12ZVL8	MC9S12ZVLS32	MC9S12ZVLS16
SCI[6]	2			2			2	
SPI	1			1			1	
IIC	1			1			1	
MSCAN	1			-			-	
max SRAM_ECC access width	4 Byte			2 Byte			2 Byte	
Supported ADC option bits	yes			no			no	
General purpose I/O - pin to support 25 mA driver strength to VSSX - pin to support 20 mA driver strength from VDDX (EVDD)	34(3) / 19 3(3) / 1 1			34(3) / 19 3(3) / 1 1			18 3 1	
Interrupt capable pins[7] 5V / 12V	22(3) / 16 / 1			22(3) / 16 / 1			14 / 1	

1 total current capability for MCU and MCU - external loads (on same PCB - board)

2 MC9S12ZVLA device only

3 available in 48-pin packages only

4 to internally feed the ACMP or bonded out in 48-LQFP

5 only 5V operation mode supported

6 one SCI routed to the LINPHY

7 $\overline{\text{IRQ}}$ / $\overline{\text{XIRQ}}$ and KWx pins

NOTE

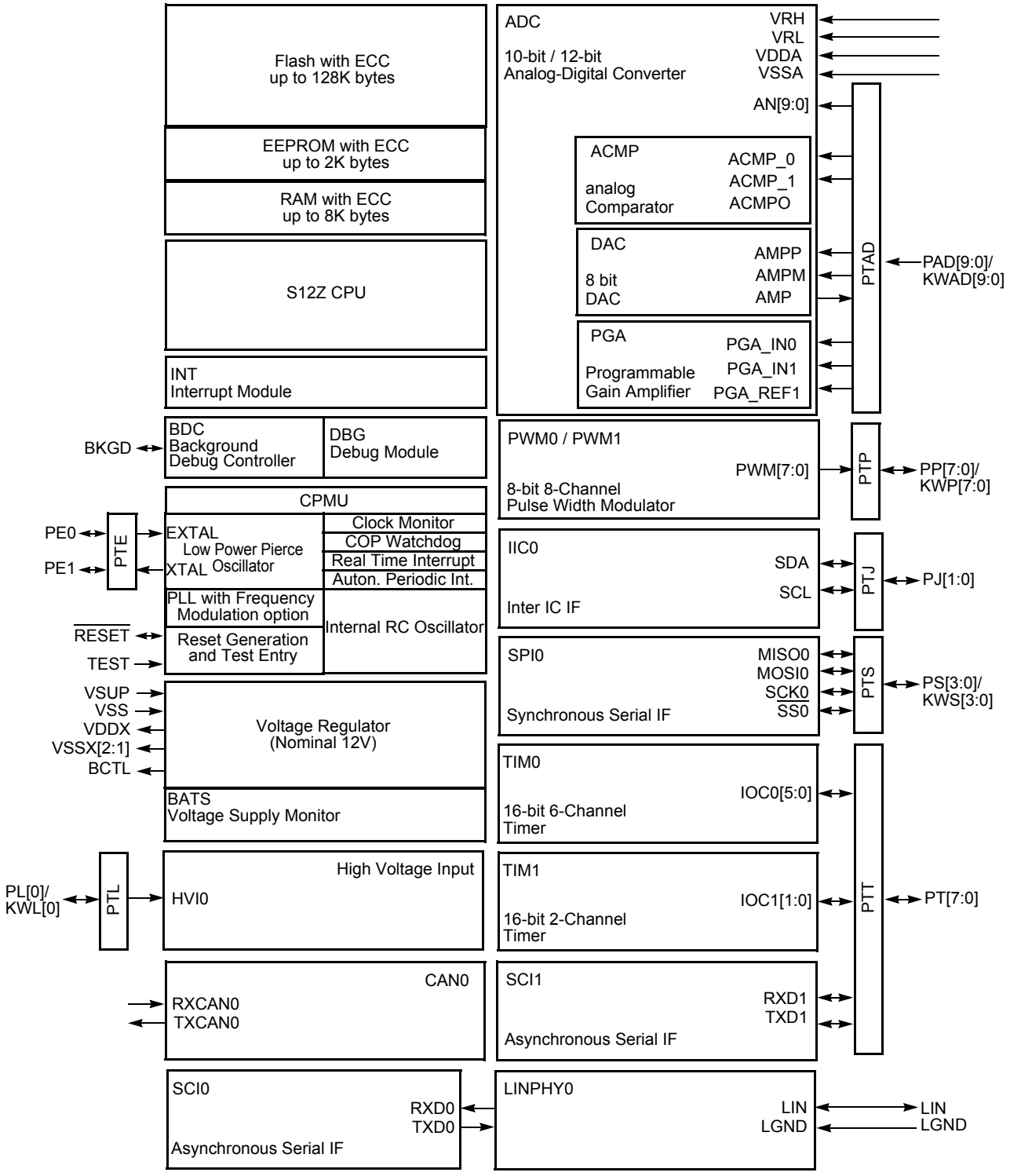
After power up, the MC9S12ZVL(A)128/96/64 devices starts in 3.3V VDDX mode. Then is possible to switch to the 5.0V VDDX behavior. For more details see the “Clock, Reset and Power Management Unit” section, 9.3.2.27, “Voltage Regulator Control Register (CPMUVREGCTL)

1.3 Chip-Level Features

On-chip modules available within the family include the following features:

- S12Z CPU core
- 128, 96, 64, 32, 16 or 8 KB on-chip flash with ECC
- 2048, 1024, 128 byte EEPROM with ECC
- 8192, 4096, 1024 or 512 byte on-chip SRAM with ECC
- Phase locked loop (IPLL) frequency multiplier with internal filter
- 1 MHz internal RC oscillator with +/-1.3% accuracy over rated temperature range
- 4-20 MHz amplitude controlled pierce oscillator

1.5 Block Diagram



Block Diagram shows the maximum configuration
Not all pins or all peripherals are available on all devices and packages.
Rerouting options are not shown.

Figure 1-1. MC9S12ZVL-Family Block Diagram

To avoid current drawn from floating inputs, all non-bonded pins should be configured as output or configured as input with a pull up or pull down device enabled

1.7.2 Detailed External Signal Descriptions

This section describes the properties of signals available at device pins. Signal names associated with modules that can be instantiated more than once on an S12 are indexed, even if the module is only instantiated once on the MC9S12ZVL-Family. If a signal already includes a channel number, then the index is inserted before the channel number. Thus ANx_y corresponds to AN instance x, channel number y.

1.7.2.1 $\overline{\text{RESET}}$ — External Reset Signal

The $\overline{\text{RESET}}$ signal is an active low bidirectional control signal. It acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset. The $\overline{\text{RESET}}$ pin has an internal pull-up device.

1.7.2.2 TEST — Test Pin

This input only pin is reserved for factory test. This pin has an internal pull-down device.

NOTE

The TEST pin must be tied to ground in all applications.

1.7.2.3 MODC — Mode C Signal

The MODC signal is used as a MCU operating mode select during reset. The state of this signal is latched to the MODC bit at the rising edge of $\overline{\text{RESET}}$. Out of reset the pull-up device is enabled.

1.7.2.4 PAD[9:0] / KWAD[9:0] — Port AD, Input Pins of ADC

PAD[9:0] are general-purpose input or output signals. The signals can be configured on per signal basis as interrupt inputs with wake-up capability (KWAD[9:0]). These signals can have a pull-up or pull-down device selected and enabled on per signal basis. During and out of reset the pull devices are disabled.

1.7.2.5 PE[1:0] — Port E I/O Signals

PE[1:0] are general-purpose input or output signals. The signals can have a pull-down device, enabled by on a per pin basis. Out of reset the pull-down devices are enabled.

1.7.2.6 PL0 — Port L Input Signal

PL0 is the high voltage input port. The signal can be configured as interrupt input with wake-up capability (KWL[0]).The pin voltage is divided and mapped to an ADC channel.

2.5 Initialization and Application Information

2.5.1 Port Data and Data Direction Register writes

It is not recommended to write PORTx/PTx and DDRx in a word access. When changing the register pins from inputs to outputs, the data may have extra transitions during the write access. Initialize the port data register before enabling the outputs.

2.5.2 SCI Baud Rate Detection

The baud rate for SCI0 and SCI1 can be determined by using a timer channel to measure the data rate on the related RXD signal.

1. Establish the link:
   - For SCI0: Set MODRR4[T0IC3RR1:T0IC3RR0]=0b01 to disconnect the pin from TIM0 input capture channel 3 and reroute the timer input to the internal RXD0 signal of SCI0.
   - For SCI1: Set MODRR4[T0IC3RR1:T0IC3RR0]=0b10 to disconnect the pin from TIM0 input capture channel 3 and reroute the timer input to the internal RXD1 signal of SCI1.
2. Determine pulse width of incoming data: Configure TIM0 input capture channel 3 to measure time between incoming signal edges.

2.5.3 Over-Current Protection on EVDD1

Pin PP7 can be used as general-purpose I/O or due to its increased current capability in output mode as a switchable external power supply pin (EVDD1) for external devices like Hall sensors.

EVDD1 connects the load to the digital supply VDDX.

An over-current monitor is implemented to protect the controller from short circuits or excess currents on the output which can only arise if the pin is configured for full drive. Although the full drive current is available on the high and low side, the protection is only available on the high side when sourcing current from EVDD1 to VSSX. There is also no protection to voltages higher than V_{DDX}.

To power up the over-current monitor set the related OCPEx bit.

In stop mode the over-current monitor is disabled for power saving. The increased current capability cannot be maintained to supply the external device. Therefore when using the pin as power supply the external load must be powered down prior to entering stop mode by driving the output low.

An over-current condition is detected if the output current level exceeds the threshold I_{OCD} in run mode. The output driver is immediately forced low and the over-current interrupt flag OCIFx asserts. Refer to Section 2.4.4.3, “Over-Current Interrupt”.

2.5.4 Over-Current Protection on PP[5,3,1]

Pins PP[5,3,1] can be used as general-purpose I/O or due to their increased current capability in output mode as a switchable external power ground pin for external devices like LEDs supplied by VDDX.

Field	Description
7-4 (MMCECL) ACC[3:0]	**Access Type Field** — The ACC[3:0] bits capture the type of memory access, which caused the access violation. The access type is captured in form of a 4 bit value which is assigned as follows: 0:none (no error condition detected) 1:opcode fetch 2:vector fetch 3:data load 4:data store 5-15: reserved
3-0 (MMCECL) ERR[3:0]	**Error Type Field** — The EC[3:0] bits capture the type of the access violation. The type is captured in form of a 4 bit value which is assigned as follows: 0:none (no error condition detected) 1:access to an illegal address 2:uncorrectable ECC error 3-15:reserved

The MMCEC register captures debug information about access violations. It is set to a non-zero value if a S12ZCPU access violation or an uncorrectable ECC error has occurred. At the same time this register is set to a non-zero value, access information is captured in the MMCPCn and MMCCCRn registers. The MMCECn, the MMCPCn and the MMCCCRn registers are not updated if the MMCECn registers contain a non-zero value. The MMCECn registers are cleared by writing the value 0xFFFF.

4.3.2.3 Captured S12ZCPU Condition Code Register (MMCCCRH, MMCCCRL)

Address: 0x0082 (MMCCCRH)

	7	6	5	4	3	2	1	0
R	CPUU	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Address: 0x0083 (MMCCCRL)

	7	6	5	4	3	2	1	0
R	0	CPUX	0	CPUI	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

Figure 4-6. Captured S12ZCPU Condition Code Register (MMCCCRH, MMCCCRL)

Read: Anytime

Write: Never

Table 9-13. RTI Frequency Divide Rates for RTDEC=1

RTR[3:0]	RTR[6:4] =							
	000 ($1x10^3$)	001 ($2x10^3$)	010 ($5x10^3$)	011 ($10x10^3$)	100 ($20x10^3$)	101 ($50x10^3$)	110 ($100x10^3$)	111 ($200x10^3$)
0000 (÷1)	$1x10^3$	$2x10^3$	$5x10^3$	$10x10^3$	$20x10^3$	$50x10^3$	$100x10^3$	$200x10^3$
0001 (÷2)	$2x10^3$	$4x10^3$	$10x10^3$	$20x10^3$	$40x10^3$	$100x10^3$	$200x10^3$	$400x10^3$
0010 (÷3)	$3x10^3$	$6x10^3$	$15x10^3$	$30x10^3$	$60x10^3$	$150x10^3$	$300x10^3$	$600x10^3$
0011 (÷4)	$4x10^3$	$8x10^3$	$20x10^3$	$40x10^3$	$80x10^3$	$200x10^3$	$400x10^3$	$800x10^3$
0100 (÷5)	$5x10^3$	$10x10^3$	$25x10^3$	$50x10^3$	$100x10^3$	$250x10^3$	$500x10^3$	$1x10^6$
0101 (÷6)	$6x10^3$	$12x10^3$	$30x10^3$	$60x10^3$	$120x10^3$	$300x10^3$	$600x10^3$	$1.2x10^6$
0110 (÷7)	$7x10^3$	$14x10^3$	$35x10^3$	$70x10^3$	$140x10^3$	$350x10^3$	$700x10^3$	$1.4x10^6$
0111 (÷8)	$8x10^3$	$16x10^3$	$40x10^3$	$80x10^3$	$160x10^3$	$400x10^3$	$800x10^3$	$1.6x10^6$
1000 (÷9)	$9x10^3$	$18x10^3$	$45x10^3$	$90x10^3$	$180x10^3$	$450x10^3$	$900x10^3$	$1.8x10^6$
1001 (÷10)	$10\ x10^3$	$20x10^3$	$50x10^3$	$100x10^3$	$200x10^3$	$500x10^3$	$1x10^6$	$2x10^6$
1010 (÷11)	$11\ x10^3$	$22x10^3$	$55x10^3$	$110x10^3$	$220x10^3$	$550x10^3$	$1.1x10^6$	$2.2x10^6$
1011 (÷12)	$12x10^3$	$24x10^3$	$60x10^3$	$120x10^3$	$240x10^3$	$600x10^3$	$1.2x10^6$	$2.4x10^6$
1100 (÷13)	$13x10^3$	$26x10^3$	$65x10^3$	$130x10^3$	$260x10^3$	$650x10^3$	$1.3x10^6$	$2.6x10^6$
1101 (÷14)	$14x10^3$	$28x10^3$	$70x10^3$	$140x10^3$	$280x10^3$	$700x10^3$	$1.4x10^6$	$2.8x10^6$
1110 (÷15)	$15x10^3$	$30x10^3$	$75x10^3$	$150x10^3$	$300x10^3$	$750x10^3$	$1.5x10^6$	$3x10^6$
1111 (÷16)	$16x10^3$	$32x10^3$	$80x10^3$	$160x10^3$	$320x10^3$	$800x10^3$	$1.6x10^6$	$3.2x10^6$

Three control bits in the CPMUCOP register allow selection of seven COP time-out periods.

When COP is enabled, the program must write $55 and $AA (in this order) to the CPMUARMCOP register during the selected time-out period. Once this is done, the COP time-out period is restarted. If the program fails to do this and the COP times out, a COP reset is generated. Also, if any value other than $55 or $AA is written, a COP reset is generated.

Windowed COP operation is enabled by setting WCOP in the CPMUCOP register. In this mode, writes to the CPMUARMCOP register to clear the COP timer must occur in the last 25% of the selected time-out period. A premature write will immediately reset the part.

In MCU Normal Mode the COP time-out period (CR[2:0]) and COP window (WCOP) setting can be automatically pre-loaded at reset release from NVM memory (if values are defined in the NVM by the application). By default the COP is off and no window COP feature is enabled after reset release via NVM memory. The COP control register CPMUCOP can be written once in an application in MCU Normal Mode to update the COP time-out period (CR[2:0]) and COP window (WCOP) setting loaded from NVM memory at reset release. Any value for the new COP time-out period and COP window setting is allowed except COP off value if the COP was enabled during pre-load via NVM memory.
The COP clock source select bits can not be pre-loaded via NVM memory at reset release. The IRC clock is the default COP clock source out of reset.
The COP clock source select bits (COPOSCSEL0/1) and ACLK clock control bit in Stop Mode (CSAD) can be modified until the CPMUCOP register write once has taken place. Therefore these control bits should be modified before the final COP time-out period and window COP setting is written.
The CPMUCOP register access to modify the COP time-out period and window COP setting in MCU Normal Mode after reset release must be done with the WRTMASK bit cleared otherwise the update is ignored and this access does not count as the write once.

9.5.6 Power-On Reset (POR)

The on-chip POR circuitry detects when the internal supply VDD drops below an appropriate voltage level. The POR is deasserted, if the internal supply VDD exceeds an appropriate voltage level (voltage levels not specified, because the internal supply can not be monitored externally).The POR circuitry is always active. It acts as LVR in Stop Mode.

9.5.7 Low-Voltage Reset (LVR)

The on-chip LVR circuitry detects when one of the supply voltages VDD, VDDX and VDDF drops below an appropriate voltage level. If LVR is deasserted the MCU is fully operational at the specified maximum speed. The LVR assert and deassert levels for the supply voltage VDDX are V_{LVRXA} and V_{LVRXD} and are specified in the device Reference Manual.The LVR circuitry is active in Run- and Wait Mode.

Table 10-10. ADCFLWCTL Field Descriptions (continued)

Field	Description
5 RSTA	**Restart Event (Restart from Top of Command Sequence List)** — This bit indicates that a Restart Event is executed. The ADC loads the conversion command from top of the active Sequence Command List when no conversion or conversion sequence is ongoing. This bit is cleared when the first conversion command of the sequence from top of active Sequence Command List has been loaded into the ADCCMD register. This bit can only be set if bit ADC_EN is set. This bit is cleared if bit ADC_EN is clear. *Data Bus Control:* This bit can be controlled via the data bus if access control is configured accordingly via ACC_CFG[1:0]. Writing a value of 1'b0 does not clear the flag. Writing a one to this bit does not clear it but causes an overrun if the bit has already been set. See also Section 10.6.3.2.6, "Conversion flow control in case of conversion sequence control bit overrun scenarios for more details. *Internal Interface Control:* This bit can be controlled via the internal interface Signal "Restart" if access control is configured accordingly via ACC_CFG[1:0]. After being set an additional request via internal interface Signal "Restart" causes an overrun. See conversion flow control in case of overrun situations for more details. General: In conversion flow control mode "Trigger Mode" when bit RSTA gets set bit TRIG is set simultaneously if one of the following has been executed: - "End Of List" command type has been executed or is about to be executed - Sequence Abort Event 0 Continue with commands from active Sequence Command List. 1 Restart from top of active Sequence Command List.
4 LDOK	**Load OK for alternative Command Sequence List** — This bit indicates if the preparation of the alternative Sequence Command List is done and Command Sequence List must be swapped with the Restart Event. This bit is cleared when bit RSTA is set (Restart Event executed) and the Command Sequence List got swapped. This bit can only be set if bit ADC_EN is set. This bit is cleared if bit ADC_EN is clear. This bit is forced to zero if bit CSL_BMOD is clear. *Data Bus Control:* This bit can be controlled via the data bus if access control is configured accordingly via ACC_CFG[1:0]. Writing a value of 1'b0 does not clear the flag. To set bit LDOK the bits LDOK and RSTA must be written simultaneously. After being set this bit can not be cleared by writing a value of 1'b1. See also Section 10.6.3.2.6, "Conversion flow control in case of conversion sequence control bit overrun scenarios for more details. *Internal Interface Control:* This bit can be controlled via the internal interface Signal "LoadOK" and "Restart" if access control is configured accordingly via ACC_CFG[1:0]. With the assertion of Interface Signal "Restart" the interface Signal "LoadOK" is evaluated and bit LDOK set accordingly (bit LDOK set if Interface Signal "LoadOK" asserted when Interface Signal "Restart" asserts). General: Only in "Restart Mode" if a Restart Event occurs without bit LDOK being set the error flag LDOK_EIF is set except when the respective Restart Request occurred after or simultaneously with a Sequence Abort Request. The LDOK_EIF error flag is also not set in "Restart Mode" if the first Restart Event occurs after: - ADC got enabled - Exit from Stop Mode - ADC Soft-Reset 0 Load of alternative list done. 1 Load alternative list.

10.5.2.17 ADC Command Register 2 (ADCCMD_2)

A command which contains reserved bit settings causes the error flag CMD_EIF being set and ADC cease operation.

Module Base + 0x0016

	15	14	13	12	11	10	9	8
R	SMP[4:0]					0	0	Reserved
W								
R	SMP[4:0]					OPT[3:2][1]		Reserved
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 10-20. ADC Command Register 2 (ADCCMD_2)

[1] Only available on ADC12B_LBA V2 and V3 (see Table 10-2 for details)

Read: Anytime

Write: Only writable if bit SMOD_ACC is set
(see also Section 10.5.2.2, “ADC Control Register 1 (ADCCTL_1) bit SMOD_ACC description for more details)

Table 10-25. ADCCMD_2 Field Descriptions

Field	Description
15-11 SMP[4:0]	**Sample Time Select Bits** — These four bits select the length of the sample time in units of ADC conversion clock cycles. Note that the ADC conversion clock period is itself a function of the prescaler value (bits PRS[6:0]). Table 10-26 lists the available sample time lengths.
	ADC12B_LBA V2 and V3 (includes OPT[3:2])
10-9 OPT[3:2]	**Option Bits** — These two option bits can be used to control a SoC level feature/function. These bits are used together with Option bits OPT[1:0]. Please refer to the device reference manual for details of the feature/functionality controlled by these bits.

NOTE

If bit SMOD_ACC is set modifying this register must be done carefully - only when no conversion and conversion sequence is ongoing.

Table 10-26. Sample Time Select

SMP[4]	SMP[3]	SMP[2]	SMP[1]	SMP[0]	Sample Time in Number of ADC Clock Cycles
0	0	0	0	0	4
0	0	0	0	1	5
0	0	0	1	0	6
0	0	0	1	1	7

– *When finished:*
This bit is cleared when the first conversion command of the sequence from top of active Sequence Command List is loaded

– *Mandatory Requirement:*
- In all ADC conversion flow control modes a Restart Event causes bit RSTA to be set. Bit SEQA is set simultaneously by ADC hardware if:
* ADC not idle (a conversion or conversion sequence is ongoing and current CSL not finished) and no Sequence Abort Event in progress (bit SEQA not already set or set simultaneously via internal interface or data bus)
* ADC idle but RVL done condition not reached
The RVL done condition is reached by one of the following:
* A “End Of List” command type has been executed
* A Sequence Abort Event is in progress or has been executed (bit SEQA already set or set simultaneously via internal interface or data bus)
The ADC executes the Sequence Abort Event followed by the Restart Event for the conditions described before or only a Restart Event.
- In ADC conversion flow control mode “Trigger Mode” a Restart Event causes bit TRIG being set automatically. Bit TRIG is set when no conversion or conversion sequence is ongoing (ADC idle) and the RVL done condition is reached by one of the following:
* A “End Of List” command type has been executed
* A Sequence Abort Event is in progress or has been executed
The ADC executes the Restart Event followed by the Trigger Event.
- In ADC conversion flow control mode “Trigger Mode” a Restart Event and a simultaneous Trigger Event via internal interface or data bus causes the TRIG_EIF bit being set and ADC cease operation.

- **Restart Event + CSL Exchange (Swap)**
Internal Interface Signals: Restart + LoadOK
Corresponding Bit Names: RSTA + LDOK

– *Function:*
Go to top of active CSL (clear index register for CSL) and switch to other offset register for address calculation if configured for double buffer mode (exchange the CSL list)
Requested by:
- Internal interface with the assertion of Interface Signal Restart the interface Signal LoadOK is evaluated and bit LDOK is set accordingly (bit LDOK set if Interface Signal LoadOK asserted when Interface Signal Restart asserts).
- Write Access via data bus to set control bit RSTA simultaneously with bit LDOK.

– *When finished:*
Bit LDOK can only be cleared if it was set as described before and both bits (LDOK, RSTA) are cleared when the first conversion command from top of active Sequence Command List is loaded

– *Mandatory Requirement:*
No ongoing conversion or conversion sequence
Details if using the internal interface:

10.9.9 Triggered Conversion — Single CSL

Applications that require the conversion of one or more groups of different channels in a periodic and timed manner can make use of a configuration in “Trigger Mode” with a single CSL containing a list of sequences. This means the CSL consists of several sequences each separated by an “End of Sequence” command. The last command of the CSL uses the “End Of List” command with wrap to top of CSL and waiting for a Trigger (CMD_SEL[1:0] =2’b11). Hence after the initial Restart Event each sequence can be launched via a Trigger Event and repetition of the CSL can be launched via a Trigger after execution of the “End Of List” command.

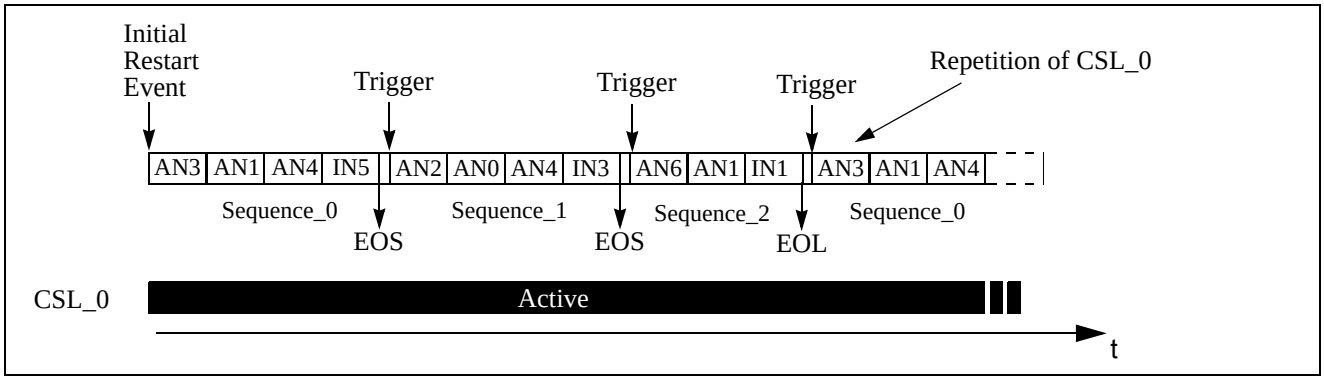


Figure 10-42. Conversion Flow Control Diagram — Triggered Conversion (CSL Repetition)

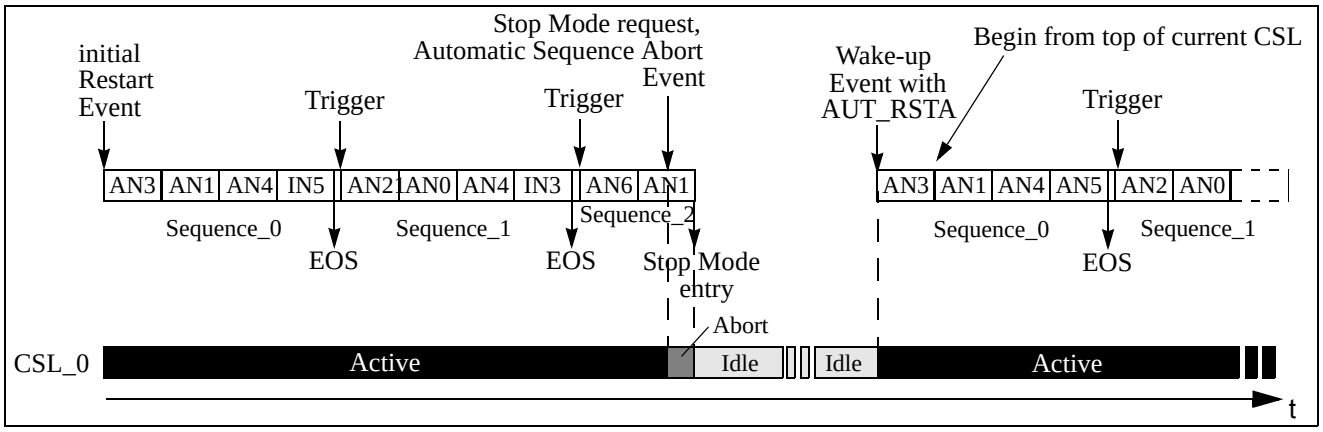


Figure 10-43. Conversion Flow Control Diagram — Triggered Conversion (with Stop Mode)

In case a Low Power Mode is used:
If bit AUT_RSTA is set before Low Power Mode is entered, the conversion continues automatically as soon as a low power mode (Stop Mode or Wait Mode with bit SWAI set) is exited.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0010–0x0013 CANIDAR0–3	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
	W								
0x0014–0x0017 CANIDMRx	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
	W								
0x0018–0x001B CANIDAR4–7	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
	W								
0x001C–0x001F CANIDMR4–7	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
	W								
0x0020–0x002F CANRXFG	R	See Section 13.3.3, “Programmer’s Model of Message Storage”							
	W								
0x0030–0x003F CANTXFG	R	See Section 13.3.3, “Programmer’s Model of Message Storage”							
	W								

= Unimplemented or Reserved

Figure 13-3. MSCAN Register Summary (continued)

13.3.2 Register Descriptions

This section describes in detail all the registers and register bits in the MSCAN module. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order. All bits of all registers in this module are completely synchronous to internal clocks during a register read.

13.3.2.1 MSCAN Control Register 0 (CANCTL0)

The CANCTL0 register provides various control bits of the MSCAN module as described below.

Module Base + 0x0000 — Access: User read/write[1]

	7	6	5	4	3	2	1	0
R	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
W								
Reset:	0	0	0	0	0	0	0	1

= Unimplemented

Figure 13-4. MSCAN Control Register 0 (CANCTL0)

[1] Read: Anytime
Write: Anytime when out of initialization mode; exceptions are read-only RXACT and SYNCH, RXFRM (which is set by the module only), and INITRQ (which is also writable in initialization mode)

NOTE

The CANCTL0 register, except WUPE, INITRQ, and SLPRQ, is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK = 1). This register is writable again as soon as the initialization mode is exited (INITRQ = 0 and INITAK = 0).

Table 13-3. CANCTL0 Register Field Descriptions

Field	Description
7 RXFRM	**Received Frame Flag** — This bit is read and clear only. It is set when a receiver has received a valid message correctly, independently of the filter configuration. After it is set, it remains set until cleared by software or reset. Clearing is done by writing a 1. Writing a 0 is ignored. This bit is not valid in loopback mode. 0 No valid message was received since last clearing this flag 1 A valid message was received since last clearing of this flag
6 RXACT	**Receiver Active Status** — This read-only flag indicates the MSCAN is receiving a message[1]. The flag is controlled by the receiver front end. This bit is not valid in loopback mode. 0 MSCAN is transmitting or idle 1 MSCAN is receiving a message (including when arbitration is lost)
5 CSWAI[2]	**CAN Stops in Wait Mode** — Enabling this bit allows for lower power consumption in wait mode by disabling all the clocks at the CPU bus interface to the MSCAN module. 0 The module is not affected during wait mode 1 The module ceases to be clocked during wait mode
4 SYNCH	**Synchronized Status** — This read-only flag indicates whether the MSCAN is synchronized to the CAN bus and able to participate in the communication process. It is set and cleared by the MSCAN. 0 MSCAN is not synchronized to the CAN bus 1 MSCAN is synchronized to the CAN bus
3 TIME	**Timer Enable** — This bit activates an internal 16-bit wide free running timer which is clocked by the bit clock rate. If the timer is enabled, a 16-bit time stamp will be assigned to each transmitted/received message within the active TX/RX buffer. Right after the EOF of a valid message on the CAN bus, the time stamp is written to the highest bytes (0x000E, 0x000F) in the appropriate buffer (see Section 13.3.3, “Programmer’s Model of Message Storage”). In loopback mode no receive timestamp is generated. The internal timer is reset (all bits set to 0) when disabled. This bit is held low in initialization mode. 0 Disable internal MSCAN timer 1 Enable internal MSCAN timer
2 WUPE[3]	**Wake-Up Enable** — This configuration bit allows the MSCAN to restart from sleep mode or from power down mode (entered from sleep) when traffic on CAN is detected (see Section 13.4.5.5, “MSCAN Sleep Mode”). This bit must be configured before sleep mode entry for the selected function to take effect. 0 Wake-up disabled — The MSCAN ignores traffic on CAN 1 Wake-up enabled — The MSCAN is able to restart

Table 13-23. CANIDMR0–CANIDMR3 Register Field Descriptions

Field	Description
7-0 AM[7:0]	**Acceptance Mask Bits** — If a particular bit in this register is cleared, this indicates that the corresponding bit in the identifier acceptance register must be the same as its identifier bit before a match is detected. The message is accepted if all such bits match. If a bit is set, it indicates that the state of the corresponding bit in the identifier acceptance register does not affect whether or not the message is accepted. 0 Match corresponding acceptance code register and identifier bits 1 Ignore corresponding acceptance code register bit

Module Base + 0x001C to Module Base + 0x001F — Access: User read/write[1]

	7	6	5	4	3	2	1	0
R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
Reset	0	0	0	0	0	0	0	0

Figure 13-22. MSCAN Identifier Mask Registers (Second Bank) — CANIDMR4–CANIDMR7

1 Read: Anytime
Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 13-24. CANIDMR4–CANIDMR7 Register Field Descriptions

Field	Description
7-0 AM[7:0]	**Acceptance Mask Bits** — If a particular bit in this register is cleared, this indicates that the corresponding bit in the identifier acceptance register must be the same as its identifier bit before a match is detected. The message is accepted if all such bits match. If a bit is set, it indicates that the state of the corresponding bit in the identifier acceptance register does not affect whether or not the message is accepted. 0 Match corresponding acceptance code register and identifier bits 1 Ignore corresponding acceptance code register bit

13.3.3 Programmer's Model of Message Storage

The following section details the organization of the receive and transmit message buffers and the associated control registers.

To simplify the programmer interface, the receive and transmit message buffers have the same outline. Each message buffer allocates 16 bytes in the memory map containing a 13 byte data structure.

An additional transmit buffer priority register (TBPR) is defined for the transmit buffers. Within the last two bytes of this memory map, the MSCAN stores a special 16-bit time stamp, which is sampled from an internal timer after successful transmission or reception of a message. This feature is only available for transmit and receiver buffers, if the TIME bit is set (see Section 13.3.2.1, "MSCAN Control Register 0 (CANCTL0)").

The time stamp register is written by the MSCAN. The CPU can only read these registers.

16.3.2.6 Timer Control Register 1/Timer Control Register 2 (TCTL1/TCTL2)

Module Base + 0x0008

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Reset	0	0	0	0	0	0	0	0

Figure 16-10. Timer Control Register 1 (TCTL1)

Module Base + 0x0009

	7	6	5	4	3	2	1	0
R W	RESERVED	RESERVED	RESERVED	RESERVED	OM1	OL1	OM0	OL0
Reset	0	0	0	0	0	0	0	0

Figure 16-11. Timer Control Register 2 (TCTL2)

Read: Anytime

Write: Anytime

Table 16-6. TCTL1/TCTL2 Field Descriptions

Note: Writing to unavailable bits has no effect. Reading from unavailable bits return a zero

Field	Description
1:0 OMx	**Output Mode** — These two pairs of control bits are encoded to specify the output action to be taken as a result of a successful OCx compare. When either OMx or OLx is 1, the pin associated with OCx becomes an output tied to OCx. **Note:** For an output line to be driven by an OCx the OCPDx must be cleared.
1:0 OLx	**Output Level** — These two pairs of control bits are encoded to specify the output action to be taken as a result of a successful OCx compare. When either OMx or OLx is 1, the pin associated with OCx becomes an output tied to OCx. **Note:** For an output line to be driven by an OCx the OCPDx must be cleared.

Table 16-7. Compare Result Output Action

OMx	OLx	Action
0	0	No output compare action on the timer output signal
0	1	Toggle OCx output line
1	0	Clear OCx output line to zero
1	1	Set OCx output line to one

- For channels 0, 1, 4, and 5 the clock choices are clock A.
- For channels 2, 3, 6, and 7 the clock choices are clock B.

17.6 Interrupts

The PWM module has no interrupt.

Table 18-6. SCIACR1 Field Descriptions (continued)

Field	Description
1 BERRIE	**Bit Error Interrupt Enable** — BERRIE enables the bit error interrupt flag, BERRIF, to generate interrupt requests. 0 BERRIF interrupt requests disabled 1 BERRIF interrupt requests enabled
0 BKDIE	**Break Detect Interrupt Enable** — BKDIE enables the break detect interrupt flag, BKDIF, to generate interrupt requests. 0 BKDIF interrupt requests disabled 1 BKDIF interrupt requests enabled

18.3.2.5 SCI Alternative Control Register 2 (SCIACR2)

Module Base + 0x0002

	7	6	5	4	3	2	1	0
R	IREN	TNP1	TNP0	0	0	BERRM1	BERRM0	BKDFE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 18-8. SCI Alternative Control Register 2 (SCIACR2)

Read: Anytime, if AMAP = 1

Write: Anytime, if AMAP = 1

Table 18-7. SCIACR2 Field Descriptions

Field	Description
7 IREN	**Infrared Enable Bit** — This bit enables/disables the infrared modulation/demodulation submodule. 0 IR disabled 1 IR enabled
6:5 TNP[1:0]	**Transmitter Narrow Pulse Bits** — These bits enable whether the SCI transmits a 1/16, 3/16, 1/32 or 1/4 narrow pulse. See Table 18-8.
2:1 BERRM[1:0]	**Bit Error Mode** — Those two bits determines the functionality of the bit error detect feature. See Table 18-9.
0 BKDFE	**Break Detect Feature Enable** — BKDFE enables the break detect circuitry. 0 Break detect circuit disabled 1 Break detect circuit enabled

Table 18-8. IRSCI Transmit Pulse Width

TNP[1:0]	Narrow Pulse Width
11	1/4
10	1/32
01	1/16

[5] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

A.1.7 I/O Characteristics

This section describes the characteristics of I/O pins.

Table A-10. 5V I/O Characteristics (Junction Temperature From –40°C To +175°C)

Conditions are: MC9S12ZVL(S)32\16\8: 4.5V ≤ V_{DDX} ≤ 5.5V, MC9S12ZVL(A)128\96\64: 4.85V ≤ V_{DDX} ≤ 5.15V, unless otherwise noted. I/O Characteristics for all GPIO pins (defined in A.1.1.1/A-671).						
Num	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1a	Input high voltage	V_{IH}	0.65*V_{DDX}	—	—	V
1b	Input high voltage BKGD pin, 3.15 V < V_{DDX} <5.5V	V_{IH}	0.65*V_{DDX}	—	—	V
2	Input high voltage	V_{IH}	—	—	V_{DDX}+0.3	V
3a	Input low voltage	V_{IL}	—	—	0.35*V_{DDX}	V
3b	Input low voltage BKGD pin, 3.15 V < V_{DDX} <5.5V	V_{IL}	—	—	0.35*V_{DDX}	V
4	Input low voltage	V_{IL}	V_{SSX}–0.3	—	—	V
5	Input hysteresis	V_{HYS}	—	250	—	mV
6	Input leakage current on all GPIO - except PP1, PP3, PP5 and PP7 - except PAD0 and PAD1 for 150°C < T_J < 175°C (Pins in high impedance input mode) [1] V_{in} = V_{DDX} or V_{SSX}	I_{in}	-1	—	1	µA
7	Input leakage current on PAD0 for 150°C < T_J < 175°C (Pin in high impedance input mode)[1] V_{in} = V_{DDX} or V_{SSX}	I_{in}	-1.5	—	1.5	µA
8	Input leakage current on PAD1 for 150°C < T_J < 175°C (Pin in high impedance input mode)[1] V_{in} = V_{DDX} or V_{SSX}	I_{in}	-3.5	—	3.5	µA
9	Input leakage current on PP1, PP3, PP5 and PP7 for -40°C < T_J < 150°C (Pins in high impedance input mode)[1] V_{in} = V_{DDX} or V_{SSX}	I_{in}	-2.5	—	2.5	µA
10	Input leakage current on PP1, PP3, PP5 and PP7 for 150°C < T_J < 175°C (Pins in high impedance input mode)[1] V_{in} = V_{DDX} or V_{SSX}	I_{in}	-3.5	—	7	µA
11	Output high voltage (All GPIO except PP1, PP3[2], PP5[2] and PP7) I_{OH} = -4 mA	V_{OH}	V_{DDX} – 0.8	—	—	V
12	Output low voltage (All GPIO except PP1, PP3[2], PP5[2] and PP7) I_{OL} = +4mA	V_{OL}	—	—	0.8	V

1. The values for thermal resistance are achieved by package simulations

I.3 Dynamic Electrical Characteristics

Table I-3. Dynamic Electrical Characteristics of the analog comparator - ACMP

Characteristics noted under conditions $3.20V \le V_{DDA} \le 5.15V$, $-40°C \le T_J \le 175°C$[1] unless otherwise noted. Typical values noted reflect the approximate parameter mean at $T_A = 25°C$[2] under nominal conditions unless otherwise noted.						
Num	**Ratings**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	Output uncertain time after module enable	$t_{ACMP\_dly\_en}$	-	1	2	µs
2	ACMP Propagation Delay of Inputs ACMP0 and ACMP1 for $-2*V_{hyst(typ)}$ to $+2*V_{hyst(typ)}$ input step (w/o synchronize delay) • ACDLY=0 Low speed mode • ACDLY=1 High speed mode ACMPP is crossing ACMPN in positive direction	t_{ACMP_delay}	130 20	300 70	750 400	ns ns
3	ACMP Propagation Delay of Inputs ACMP0 and ACMP1 for $-2*V_{hyst(typ)}$ to $+2*V_{hyst(typ)}$ input step (w/o synchronize delay) $150°C \le T_J \le 175°C$ • ACDLY=0 Low speed mode • ACDLY=1 High speed mode ACMPP is crossing ACMPN in positive direction	t_{ACMP_delay}	- -	- -	800 450	ns ns

1 T_J: Junction Temperature

2 T_A: Ambient Temperature